09/12/02
20020748 13

*162162*

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
13 December 2001 (13.12.2001)

PCT

(10) International Publication Number
WO 01/95377 A3

(51) International Patent Classification[7]: H01L 21/02

(21) International Application Number: PCT/US01/18583

(22) International Filing Date: 7 June 2001 (07.06.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/590,791 8 June 2000 (08.06.2000) US

(71) Applicant: MICRON TECHNOLOGY, INC. [US/US]; 8000 South Federal Way, Boise, ID 83706-9632 (US).

(72) Inventors: BASCERI, Cem; 314 E. Iowa Drive, Boise, ID 83706 (US). VISOKAY, Mark; 2705 Millwood Drive, Richardson, TX 75082 (US). GRAETTINGER, Thomas, M.; 1880 S. Leadville Avenue, Boise, ID 83706 (US). CUMMINGS, Steven, D.; 545 Robie Creek, Boise, ID 83716 (US).

(74) Agent: JONES, Michael, D.; Klarquist Sparkman LLP One World Trade Center, Suite 1600, 121 SW Salmon Street, Portland, OR 97204 (US).

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

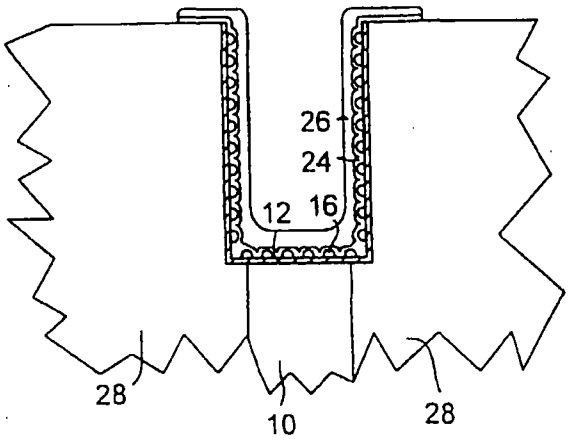
(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
--- with international search report

(88) Date of publication of the international search report:
30 May 2002

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

(54) Title: METHODS FOR FORMING AND INTEGRATED CIRCUIT STRUCTURES CONTAINING ENHANCED-SURFACE-AREA CONDUCTIVE LAYERS




(57) Abstract: An enhanced-surface-area conductive layer compatible with high-dielectric constant materials is created by forming a film or layer having at least two phases, at least one of which is electrically conductive. The film may be formed in any convenient manner, such as by chemical vapor deposition techniques, which may be followed by an anneal to better define and/or crystallize the at least two phases. The film may be formed over an underlying conductive layer. At least one of the least two phases is selectively removed from the film, such as by an etch process that preferentially etches at least one of the at least two phases so as to leave at least a portion of the electrically conductive phase. Ruthenium and ruthenium oxide, both conductive, may be used for the two or more phases. Iridium and its oxide, rhodium and its oxide, and platinum and platinum-rhodium may also be used. A wet etchant comprising ceric ammonium nitrate and acetic acid may be used. In the case of this etchant and a ruthenium/ruthenium oxide film, the etchant preferentially removes the ruthenium phase, leaving a pitted or "islanded" surface of ruthenium oxide physically and electrically connected by the underlying conductive layer. The remaining pitted or islanded layer, together with the underlying conductive layer, if any, constitutes an enhanced-surface-area conductive layer. The enhanced-surface-area conductive layer may be used to form a plate or a storage capacitor in an integrated circuit, such as in a memory cell of a DRAM or the like.

WO 01/95377 A3

*ACTION*