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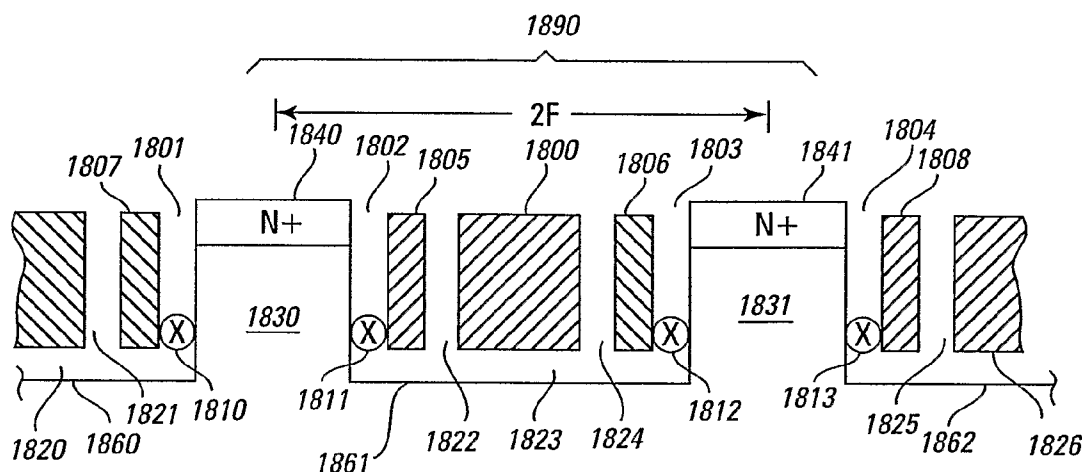
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(54) Title: APPARATUS AND METHOD FOR VERTICAL SPLIT-GATE NROM MEMORY



(57) Abstract: A split gate, vertical NROM memory cell (1890) is comprised of a plurality of oxide pillars (1830, 1831) that each has a source/drain region (1840, 1841) formed in the top of the pillar. A trench is formed between each pair of oxide pillars. A polysilicon control gate (1800) is formed in the trench between the pair of oxide pillars. A polysilicon program gate (1805, 1806) is formed between the control gate and each oxide pillar. The program gates extend along the sidewall of each oxide pillar. A gate insulator layer (1802, 1803) is formed between each program gate and the adjacent oxide pillar. Each gate insulator layer has a structure for trapping at least one charge. In one embodiment, the gate insulator structure is an oxide-nitride-oxide layer in which the charge is stored at the trench bottom end (1811, 1812) of the nitride layer. An interpoly insulator (1822, 1824) is formed between the program gates and the control gate. The charge can also be stored in the insulator layer between the bottom of the trench and the control and program gates.



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*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*