

DESCRIPTION

Title of Invention: DATA PROCESSING APPARATUS AND DATA
PROCESSING METHOD

Technical Field

[0001]

The present technology relates to data processing apparatuses and data processing methods, and more specifically to data processing apparatuses and data processing methods which enable provision of, for example, LDPC codes that achieve good error-rate performance.

Background Art

[0002]

In recent years, LDPC (Low Density Parity Check) codes, which have a high error-correcting capability, have been widely employed in transmission schemes including satellite digital broadcasting technologies, such as DVB (Digital Video Broadcasting) - S.2, which is used in Europe (see, for example, NPL 1). LDPC codes are also employed in next-generation terrestrial digital broadcasting technologies, such as DVB-T.2.

[0003]

Recent studies have found that, like turbo codes, LDPC codes have a performance closer to the Shannon limit for larger code lengths. In addition, because of their characteristic of having minimum distances proportional to

code lengths, LDPC codes have the feature of high block error probability performance, and have a further advantage in showing substantially no error floor phenomena, which is observed in the decoding characteristics of turbo codes and the like.

[0004]

LDPC codes will now be described in more detail. LDPC codes are linear codes, and may or may not be binary. The following description will be given in the context of binary LDPC codes.

[0005]

An LDPC code has the most striking feature that it is defined by a sparse parity check matrix. Here, the term "sparse matrix" refers to a matrix having a very small number of elements of 1 (or a matrix whose elements are almost zeros).

[0006]

Fig. 1 illustrates an example of a parity check matrix H of an LDPC code.

[0007]

In the parity check matrix H illustrated in Fig. 1, the weight of each column (column weight) (i.e., the number of 1s) is 3 and the weight of each row (row weight) is 6.

[0008]

In an encoding operation using an LDPC code (LDPC

encoding), for example, a generator matrix G is generated on the basis of a parity check matrix H . By multiplying the generator matrix G by binary information bits, a code word (i.e., an LDPC code) is generated.

[0009]

Specifically, an encoding device that performs LDPC encoding first calculates a generator matrix G , where the equation $GH^T = 0$ is established between the transpose H^T of the parity check matrix H and the generator matrix G . Here, if the generator matrix G is a $K \times N$ matrix, the encoding device multiplies the generator matrix G by a bit sequence (i.e., a vector u) of K information bits to generate a code word $c (= uG)$ having N bits. The code word (or LDPC code) generated by the encoding device is received on the receiver side via a certain communication path.

[0010]

An LDPC code can be decoded using the message passing algorithm, which is an algorithm called probabilistic decoding proposed by Gallager and which is based on belief propagation on a so-called Tanner graph with variable nodes (also referred to as "message nodes") and check nodes. Here, the variable nodes and the check nodes will also be hereinafter referred to simply as "nodes" as appropriate.

[0011]

Fig. 2 illustrates an LDPC code decoding procedure.

[0012]

Note that, in the following description, a real-number value representing the likelihood of the value "0" of the i -th bit of an LDPC code (i.e., a code word) received on the receiver side, which is expressed in log likelihood ratio (i.e., a reception LLR), is also referred to as a "reception value u_i ," as appropriate. Further, a message output from a check node is represented by u_i , and a message output from a variable node is represented by v_i .

[0013]

In an LDPC code decoding process, first, as illustrated in Fig. 2, in step S11, an LDPC code is received, and a message (check node message) u_i is initialized to "0". In addition, a variable k of a counter for repetitive processing, which takes an integer value, is initialized to "0". Then, the process proceeds to step S12. In step S12, a message (variable node message) v_i is determined by performing computation given by Expression (1) (variable node computation) on the basis of a reception value u_i , obtained through the reception of the LDPC code. A message u_i is further determined by performing computation given by Expression (2) (check node computation) on the basis of the message v_i .

[0014]

[Math. 1]

$$v_i = u_{0i} + \sum_{j=1}^{d_v-1} u_j \quad \dots (1)$$

[0015]

[Math. 2]

$$\tanh\left(\frac{u_j}{2}\right) = \prod_{i=1}^{d_c-1} \tanh\left(\frac{v_i}{2}\right) \quad \dots (2)$$

[0016]

Here, d_v and d_c in Expressions (1) and (2) are arbitrarily selectable parameters indicating the number of 1s in the vertical direction (columns) and the horizontal direction (rows) of the parity check matrix H , respectively. For example, for an LDPC code in a parity check matrix H with a column weight of 3 and a row weight of 6 (i.e., a (3,6) LDPC code) illustrated in Fig. 1, $d_v = 3$ and $d_c = 6$.

[0017]

Note that, in each of the variable node computation of Expression (1) and the check node computation of Expression (2), a message input from an edge (or a line connecting between a variable node and a check node) from which a message is output is not the target of the computation. Thus, the range of computation is 1 to $d_v - 1$ or 1 to $d_c - 1$. Furthermore, the check node computation of Expression (2) is actually performed by creating in advance a table of a

function $R(v_1, v_2)$ given by Expression (3), which is defined by one output for two inputs v_1 and v_2 , and sequentially (or recursively) using the table in the manner given by Expression (4).

[0018]

[Math. 3]

$$x = 2 \tanh^{-1} \{ \tanh(v_1/2) \tanh(v_2/2) \} = R(v_1, v_2) \quad \cdot \cdot \cdot (3)$$

[0019]

[Math. 4]

$$u_j = R(v_1, R(v_2, R(v_3, \dots R(v_{d_c-2}, v_{d_c-1})))) \quad \cdot \cdot \cdot (4)$$

[0020]

In step S12, furthermore, the variable k is incremented by "1". Then, the process proceeds to step S13. In step S13, it is determined whether the variable k is larger than a certain number of times of repetitive decoding C . If it is determined in step S13 that the variable k is not larger than C , the process returns to step S12, and subsequently, similar processing is repeatedly performed.

[0021]

If it is determined in step S13 that the variable k is larger than C , the process proceeds to step S14. In step

S14, a message v_i as a final output result of decoding is determined by performing computation given by Expression (5), and is output. Then, the LDPC code decoding process ends.

[0022]

[Math. 5]

$$v_i = u_{0i} + \sum_{j=1}^{d_v} u_j$$

... (5)

[0023]

Here, the computation of Expression (5) is performed using, unlike the variable node computation of Expression (1), the messages u_i from all the edges connected to a variable node.

[0024]

Fig. 3 illustrates an example of a parity check matrix H of a (3,6) LDPC code (with a code rate of 1/2 and a code length of 12).

[0025]

In the parity check matrix H illustrated in Fig. 3, similarly to Fig. 1, the column weight is 3 and the row weight is 6.

[0026]

Fig. 4 illustrates a Tanner graph of the parity check matrix H illustrated in Fig. 3.

[0027]

Here, in Fig. 4, a check node is represented by a plus "+" sign, and a variable node is represented by an equal "=" sign. A check node and a variable node correspond to each row and column of the parity check matrix H , respectively. A connection between a check node and a variable node is an edge, and corresponds to an element of "1" in the parity check matrix.

[0028]

More specifically, in a case where the element in the j -th row and the i -th column of the parity check matrix is 1, in Fig. 4, the i -th variable node ("=" node) from the top and the j -th check node ("+" node) from the top are connected by an edge. An edge indicates that a code bit corresponding to a variable node has a constraint corresponding to a check node.

[0029]

In the sum product algorithm, which is an LDPC code decoding method, variable node computation and check node computation are repeatedly performed.

[0030]

Fig. 5 illustrates variable node computation to be performed at a variable node.

[0031]

At a variable node, a message v_i corresponding to an edge for which calculation is to be performed is determined

through the variable node computation of Expression (1) using messages u_1 and u_2 from the remaining edges connected to the variable node and also using a reception value u_{01} . The messages corresponding to the other edges are also determined in a similar way.

[0032]

Fig. 6 illustrates check node computation to be performed at a check node.

[0033]

Here, the check node computation of Expression (2) can be rewritten as Expression (6) by using the relationship of the equation $a \times b = \exp\{\ln(|a|) + \ln(|b|)\} \times \text{sign}(a) \times \text{sign}(b)$, where $\text{sign}(x)$ is 1 for $x > 0$ and -1 for $x < 0$.

[0034]

[Math. 6]

$$\begin{aligned} u_j &= 2 \tanh^{-1} \left(\prod_{i=1}^{d_c-1} \tanh \left(\frac{v_i}{2} \right) \right) \\ &= 2 \tanh^{-1} \left[\exp \left\{ \sum_{i=1}^{d_c-1} \ln \left(\left| \tanh \left(\frac{v_i}{2} \right) \right| \right) \right\} \times \prod_{i=1}^{d_c-1} \text{sign} \left(\tanh \left(\frac{v_i}{2} \right) \right) \right] \\ &= 2 \tanh^{-1} \left[\exp \left\{ - \left(\sum_{i=1}^{d_c-1} - \ln \left(\tanh \left(\frac{|v_i|}{2} \right) \right) \right) \right\} \times \prod_{i=1}^{d_c-1} \text{sign}(v_i) \right] \\ &\quad \dots (6) \end{aligned}$$

[0035]

If the function $\phi(x)$ is defined as the equation $\phi(x) =$

$\ln(\tanh(x/2))$ for $x \geq 0$, the equation $\phi^{-1}(x) = 2 \tanh^{-1}(e^{-x})$ is established. Thus, Expression (6) can be transformed into Expression (7).

[0036]

[Math. 7]

$$u_j = \phi^{-1} \left(\sum_{i=1}^{d_c-1} \phi(|v_i|) \right) \times \prod_{i=1}^{d_c-1} \text{sign}(v_i) \quad \dots (7)$$

[0037]

At a check node, the check node computation of Expression (2) is performed in accordance with Expression (7).

[0038]

More specifically, at a check node, as illustrated in Fig. 6, a message u_j corresponding to an edge for which calculation is to be performed is determined through the check node computation of Expression (7) using messages v_1 , v_2 , v_3 , v_4 , and v_5 from the remaining edges connected to the check node. The messages corresponding to the other edges are also determined in a similar way.

[0039]

Note that the function $\phi(x)$ in Expression (7) can be represented by the equation $\phi(x) = \ln((e^x + 1)/(e^x - 1))$, where $\phi(x) = \phi(-x)$ for $x > 0$. The functions $\phi(x)$ and $\phi^{-1}(x)$

may be implemented in hardware by using an LUT (Look Up Table), where the same LUT is used for both functions.

Citation List

Non Patent Literature

[0040]

NPL 1: DVB-S.2 : ETSI EN 302 307 V1.2.1 (2009-08)

Summary of Invention

Technical Problem

[0041]

In the standards that employ LDPC codes, such as DVB-S.2, DVB-T.2, and DVB-C.2, an LDPC code is mapped to symbols (or is symbolized) of orthogonal modulation (digital modulation) such as QPSK (Quadrature Phase Shift Keying). The symbols are mapped to constellation points and are transmitted.

[0042]

Meanwhile, there has recently been a demand for efficient transmission of a large amount of data such as a three-dimensional (3D) image or a 4k image. A 4k image has a resolution of 3840 pixels horizontally and 2160 pixels vertically, providing approximately four times the pixel resolution of full high definition.

[0043]

However, prioritizing the efficiency of data transmission would increase an error rate.

[0044]

On the contrary, there may also be a demand that the efficiency of data transmission can be somewhat sacrificed for data transmission with good error-rate performance.

[0045]

In the future, demands for data transmission with various efficiency levels are expected to increase. For example, a plurality of LDPC codes having different code rates allow data transmission with various efficiency levels.

[0046]

In data transmission, therefore, it is desirable that LDPC codes having code rates which are easily set to a somewhat large number of code rates, the number of which is greater than or equal to, for example, the number of code rates demanded for data transmission, be employed.

[0047]

It is also desirable that LDPC codes have high resistance to errors (i.e., high robustness), that is, good error-rate performance, no matter which code rate of LDPC code is to be employed.

[0048]

Embodiments of the present invention are made in view of the foregoing situation, and are intended to provide LDPC codes having good error-rate performance.

Solution to Problem

[0049]

A data processing apparatus according to a first aspect or data processing method according to a second aspect of the present invention includes an encoding unit configured to encode or an encoding step of encoding information bits into an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 24/30 on the basis of a parity check matrix of the LDPC code, wherein the LDPC code includes information bits and parity bits, the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits, the information matrix portion is represented by a parity check matrix initial value table, and the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

1504 2103 2621 2840 3869 4594 5246 6314 7327 7364 10425
11934 12898 12954

27 1903 3923 4513 7812 8098 8428 9789 10519 11345 12032
12157 12573 12930

17 191 660 2451 2475 2976 3398 3616 5769 6724 8641
10046 11552 12842

13 1366 4993 6468 7689 8563 9131 10012 10914 11574
11837 12203 12715 12946

432 872 2603 3286 3306 3385 4137 5563 7540 9339 9948

12315 12656 12929

1113 1394 4104 4186 7240 8827 11522 11833 12359 12363
12629 12821 12904 12946

14 441 1432 1677 2432 8981 11478 11507 12599 12783
12793 12912 12922 12943

1579 1806 7971 8586 9845 10357 11600 12007 12020 12339
12576 12817 12830 12904

20 546 3672 5538 6944 8052 8781 9743 12269 12393 12418
12549 12555 12718

1 3540 4397 5013 6626 8617 9587 10360 10602 11402 11983
12068 12495 12838

30 1572 4908 7421 8041 8910 8963 11005 11930 12240
12340 12467 12892 12933

33 2060 3907 4215 5545 8306 8655 8743 8806 9315 9364
10685 11954 12959

1338 2596 4876 5207 9555 10421 10929 11648 11739 12375
12416 12643 12742 12754

9469 10544 10932 11250 11426 11582 11846 12139 12202
12210 12356 12378 12873 12929

2681 3337 3616 6113 7078 8167 8624 9697 10908 11781
11855 12095 12475 12659

28 4086 5432 6555 6848 7368 8794 11483 11572 12414
12816 12834 12936 12957

5 5044 5572 6023 9192 9589 9979 10009 10855 10991 11715
12314 12610 12945

17 272 602 5681 6530 9572 9886 11061 11495 12238 12265
12483 12885 12955
22 2245 4282 4469 5007 6650 6733 10151 10401 11571
12004 12261 12805 12844
23 3270 4468 8621 9662 11240 11934 12091 12444 12691
12717 12858 12888 12917
740 1519 4923 6191 7878 8350 9293 10779 11020 11287
11630 12792 12862 12920
12 28 3584 6072 7079 8075 10477 11130 11383 11780 12341
12667 12818 12927
14 118 5283 5382 8301 9097 9413 9664 10437 10701 11124
12685 12730 12734
32 1426 3678 4325 5353 7780 9042 9928 10077 10377 10679
11191 11750 12611
1 669 3831 3980 5381 5412 6552 8453 9435 10243 11546
11821 11987 12807
232 483 919 1232 2156 2396 2990 3774 8539 8704 8819
10810 11868 12634
2381 7309 9334
348 6494 12623
4872 6257 11090
7 11370 11985
6615 12788 12855
1173 5269 12647
1944 7738 8116

17 4828 9175
2329 6034 12642
1254 2366 5013
2984 5078 5664
7423 10265 11528
1656 8526 8716
22 287 2837
18 100 3079
299 2171 12169
33 5920 11144
1286 3650 9309
2283 8809 12583
3193 8242 9081
2507 6846 8113
5211 8722 12689
1064 2592 8659
6136 6925 12958
1256 12789 12932
4274 8945 8788
1824 3209 6926
11 8899 12669
6249 6338 8730
641 9679 12831
3459 9876 11185
3224 6148 8173

9078 12126 12771

10907 11278 12731

3392 4020 12838

2814 11588 12909

6063 9214 11519

6064 6827 12683

1610 2452 6582

903 6289 8074

4592 8138 12952

2587 6271 9945

2733 11844 11893

581 4601 10020

14 5597 6049

343 3582 5931

5263 6521 12846

1394 2457 5251

11 4627 12747

2650 10366 12390

6285 11893 12062

10143 12892 12956

8448 11917 12339

4209 11693 12356

1529 2369 9086

5389 8148 10224

66 4876 12362

9483 12659 12887

3587 6767 12478

3122 5245 9044

3267 10118 11466

1347 3857 6705

9384 9576 11971

1366 8708 10758

412 4249 12863

1676 10488 11850

17 1605 2455

14 111 6045

11368 12919 12953

10588 11530 12337

4549 5143 12218

3088 4185 11674

23 2554 7823

6615 9291 9863

2229 3629 10855

3818 5509 12764

2740 11525 12914

8297 8611 12948

3606 11104 12920

5097 10412 12759

6502 7266 12072

5425 5490 10728

22 72 8462
32 12439 12657
8483 9540 10430
7275 7377 7420
5748 9726 12356
5672 6150 9156
28 3527 5857
520 7099 11335
405 6173 12865
5847 12843 12934
4289 7679 10386
2950 8021 12938
8844 11214 12955
2130 10760 12665
734 4790 12940
8 6991 12772
19 3205 11289
12 1440 9077
8670 8837 12951
3531 9166 12937
15 8901 8929
838 10114 11740
2648 9959 10934
323 7499 12877
9505 5859 11395

6627 12709 12933
364 1976 12888
8213 9124 12793
9588 10088 11108
299 890 11634
7368 7598 11602
28 4669 12585
15 27 12474
1426 3614 4205
30 2087 11147
6226 6259 12941.

[0050]

A data processing apparatus according to a third aspect or data processing method according to a fourth aspect of the present invention includes a decoding unit configured to decode or a decoding step of decoding an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 24/30 on the basis of a parity check matrix of the LDPC code, wherein the LDPC code includes information bits and parity bits, the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits, the information matrix portion is represented by a parity check matrix initial value table, and the parity check matrix initial value table is a table showing positions of elements of 1 in the

information matrix portion in units of 360 columns,
including

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11934 12898 12954

27 1903 3923 4513 7812 8098 8428 9789 10519 11345 12032
12157 12573 12930

17 191 660 2451 2475 2976 3398 3616 5769 6724 8641
10046 11552 12842

13 1366 4993 6468 7689 8563 9131 10012 10914 11574
11837 12203 12715 12946

432 872 2603 3286 3306 3385 4137 5563 7540 9339 9948
12315 12656 12929

1113 1394 4104 4186 7240 8827 11522 11833 12359 12363
12629 12821 12904 12946

14 441 1432 1677 2432 8981 11478 11507 12599 12783
12793 12912 12922 12943

1579 1806 7971 8586 9845 10357 11600 12007 12920 12339
12576 12817 12830 12904

20 546 3672 5538 6944 8052 8781 9743 12269 12393 12418
12549 12555 12718

1 3540 4397 5911 6626 8617 9587 10360 10602 11402 11983
12068 12495 12838

30 1572 4908 7421 8041 8910 8963 11005 11930 12240
12340 12467 12892 12933

33 2060 1907 4213 5545 8306 8655 8743 8806 9315 9364

10685 11954 12959

1338 2596 4876 5207 9555 10421 10929 11648 11739 12375

12416 12643 12742 12754

9469 10544 10932 11250 11426 11582 11846 12139 12202

12210 12356 12378 12873 12929

2681 3337 3616 6113 7078 8167 8624 9697 10908 11781

11855 12095 12475 12659

28 4086 5432 6555 6848 7368 8794 11483 11572 12414

12816 12894 12936 12957

5 5044 5572 9023 9192 9589 9979 10009 10855 10991 11715

12314 12610 12945

17 272 602 5681 6530 9572 9886 11061 11495 12238 12265

12483 12885 12955

22 2245 4282 4469 5007 6650 6733 10151 10401 11571

12604 12261 12805 12844

23 3270 4468 8621 9662 11240 11934 12091 12444 12691

12717 12858 12888 12917

740 1519 4923 6191 7878 8350 9293 10779 11020 11287

11630 12792 12862 12920

12 28 3584 6072 7079 8075 10477 11130 11383 11780 12341

12667 12818 12927

14 118 5283 5392 8301 9097 9413 9664 10437 10701 11124

12685 12730 12734

32 1426 3078 4325 5353 7780 9042 9928 10077 10377 10679

11191 11750 12611

1 669 3831 3980 5381 5412 6552 8453 9435 10243 11546
11821 11987 12807
232 483 919 1232 2156 2396 2990 3774 8539 8704 8819
10810 11868 12634
2381 7309 9334
348 6494 12623
4872 6257 11090
7 11970 11985
6615 12788 12855
1173 5269 12647
1944 7738 8116
17 4828 9175
2329 6034 12642
1254 2366 5013
2984 5078 5664
7423 10265 11528
1656 3526 8116
22 287 2837
18 100 3079
299 3171 12169
33 5920 11144
1296 3650 9309
2283 8809 12558
3199 3242 9081
2507 6846 8112

5211 8722 12689
1064 2592 8659
6136 6925 12958
1256 12789 12932
4274 8045 8788
1824 3209 6926
11 8899 12669
6249 6338 8730
641 9679 12831
3459 9876 11185
3226 6148 8173
9678 12126 12771
16907 11278 12731
3392 4020 12838
2814 11588 12909
6063 9214 11519
6064 6827 12683
1610 2452 6582
903 6289 8074
4592 8138 12952
2587 6271 9945
2733 11844 11893
581 4601 10020
14 5597 6049
343 3582 5931

5263 6521 12846

1394 2457 5251

11 4627 12747

2650 10366 12390

6285 11893 12062

10143 12892 12956

8448 11917 12330

4209 11693 12356

1529 2360 9086

5389 8148 10224

64 4876 12862

9483 12659 12887

3587 6767 12478

3122 5245 9044

3267 10118 11466

1347 3857 6705

9384 9576 11971

1366 8708 10758

412 4249 12863

1676 10488 11850

17 1605 2455

14 111 6045

11368 12919 12953

10588 11530 12937

4549 5143 12213

3088 4135 11674
23 2554 7823
6615 9291 9863
2229 3629 10855
3818 5509 12764
2740 11525 12914
8297 8611 12948
3606 11104 12920
5997 10412 12759
6502 7266 12072
5425 5490 10728
22 73 8462
32 12439 12657
8483 9540 10430
7275 7377 7420
5748 9726 12356
5672 6150 9156
28 3527 5857
520 7099 11335
405 6173 12865
5847 12843 12934
4289 7679 10386
2950 8021 12938
8844 11214 12955
2110 10760 12885

734 4790 12940
8 6991 12772
19 8205 11289
12 1440 9077
8670 8837 12951
3531 9166 12937
15 8901 8929
838 10114 11740
2648 9959 10934
323 7499 12877
5505 5659 11395
6627 12709 12933
364 1976 12888
8213 9124 12793
9588 10088 11108
299 890 11634
7368 7598 11602
28 4669 12585
15 27 12474
1426 3614 4205
30 2087 11147
6226 6259 12941.

[0051]

A data processing apparatus according to a fifth aspect or data processing method according to a sixth aspect of the present invention includes an encoding unit

configured to encode or an encoding step of encoding information bits into an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 25/30 on the basis of a parity check matrix of the LDPC code, wherein the LDPC code includes information bits and parity bits, the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits, the information matrix portion is represented by a parity check matrix initial value table, and the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

1860 2354 3967 4292 4488 5243 5373 5766 8378 9111 10468
10505 10774

24 2266 2380 3282 4255 4779 8729 9140 9566 10102 10661
10711 10797

605 650 1108 1669 2251 3133 5847 6197 6902 7545 10521
10600 10773

1016 1428 1612 2335 3102 3810 4926 5953 9964 10246
10569 10734 10784

3195 6308 8029 9030 9397 9461 9833 10239 10499 10675
10736 10757 10773

2 27 3641 4566 7332 9318 9323 9916 10365 10438 10561
10581 10750

2405 2458 4820 6232 6254 6347 7139 7474 8623 8779 8798
10747 10794

3164 4736 6474 7162 7420 7517 7835 8238 8412 8489 9006
10113 10440

20 2372 5561 5649 6907 8393 8505 9181 9567 9595 10388
10483 10714

1071 2899 5135 5780 6616 7111 7773 8582 9015 9912 10139
10387 10768

292 2833 5490 6011 6136 6713 7517 9096 10128 10328
10407 10525 10736

1044 3711 4421 5140 5207 8118 8749 8884 9205 10359
10372 10746 10784

3241 5696 6440 7240 7419 8613 8878 9593 9959 9997 10401
10404 10754

3133 4647 5912 6065 6694 7208 7346 8227 9465 9739 10452
10516 10770

2254 6444 7449 8095 8120 8710 9030 9162 9643 9968 10101
10571 10678

918 1445 2217 4262 4623 5401 5745 7446 7907 9539 10125
10514 10726

6 1341 1788 3105 4359 5263 5470 7552 8249 8644 10609
10674 10733

1994 3000 3151 3173 7742 8335 8438 8741 9232 9296 9817
10022 10257

467 1674 3016 3950 4055 5399 6688 7113 7273 8658 8702

9642 10545

2007 2541 3125 7380 7550 8122 8501 8665 9882 10403

10519 10594 10696

334 587 709 1540 2023 2876 6216 8768 9328 9481 10424

10507 10779

2165 4185 4306 5019 6961 7386 8447 9082 9837 10091

10461 10559 10570

7 903 2948 6312 6654 7738 7980 8312 9104 9743 10070

10278 10406

3047 3154 4160 4373 5461 8711 8809 9040 9173 9252 9537

9995 10735

2018 2355 3828 3854 6201 6696 8312 8459 8550 8833 9586

10202 10224

1402 1908 4286 4669 6029 6115 6737 7538 9495 9517 10055

10509 10644

3442 3589 3868 5051 5322 5580 8725 9046 9170 10041

10613 10681 10689

2733 7826 10622

3597 4753 7086

1394 7297 10264

2848 7502 10304

1649 2405 10783

647 2911 9069

2572 4066 7508

1361 8887 10103

3681 4023 9090
1496 4962 6325
2016 5120 9747
3954 5260 8568
3364 8719 10035
4208 4806 9973
29 3361 3490
1835 2317 10436
7312 8177 9041
7728 8097 10761
2109 7902 9685
5424 8943 9436
4369 7643 9152
2240 10140 10528
3435 6124 10604
8962 9357 10040
26 1931 8629
9275 10455 10643
8 24 4952
3995 6456 10633
28 10300 10337
4894 9286 9429
5587 6721 9120
1859 9198 9762
6374 6453 7011

1319 4530 5442
1507 10711 10798
2115 3445 3641
6668 9139 10163
4038 8117 10295
1479 3403 8247
2522 2934 3562
1526 5073 9650
2136 9820 10636
4214 8464 9891
8018 10330 10610
8984 10299 10647
3414 7272 8599
4883 9077 9525
22 8173 8425
2941 6536 10126
29 6540 7361
5 3787 10468
4264 4818 6906
3903 7041 10412
6078 7661 10619
6522 9723 9890
5112 5416 6253
5925 9961 10447
9 10411 10598

8790 8814 10793

4768 5466 10664

10 10675 10766

6814 8705 10737

17 769 6692

1503 10696 10742

1285 4632 8976

4279 4973 7907

4650 4775 10785

28 729 10331

1914 5240 10723

3569 4921 9561

4 9442 10796

494 2328 9507

1717 8768 10750

9540 10599 10774

11 10075 10644

10246 10607 10753

5510 7088 9053

1347 3584 5523

7872 10596 10736

628 10592 10695

5632 5688 10627

2375 10009 10561

4169 4630 8871

2896 10038 10521

89 9695 9799

20 7563 9069

4534 10321 10697

8212 9868 10716

7485 9312 10327

234 536 6293

5515 7350 9251

283 3182 7167

2444 5378 6130

6183 8315 10726

43 4871 8347

2427 10219 10728

10 21 9448

1067 8312 8420

4793 9522 10105

4688 10536 10724

3825 7496 10709

682 8544 10449

2794 7110 10741

9279 10741 10767

2897 5442 8771

33 7957 10460

5 10393 10792

6225 10224 10798

23 9014 10786
7836 8339 8642
3476 5455 9788
1939 10251 10384
4008 7890 10450
926 2090 3804
1038 2497 10701
22 6220 8405
5153 5944 10367
7260 7726 9529
3039 8397 10665
7262 9644 10083
5531 6248 10795
7926 8248 8413
4649 8971 10182.

[0052]

A data processing apparatus according to a seventh aspect or data processing method according to an eighth aspect of the present invention includes a decoding unit configured to decode or a decoding step of decoding an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 25/30 on the basis of a parity check matrix of the LDPC code, wherein the LDPC code includes information bits and parity bits, the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion

corresponding to the parity bits, the information matrix portion is represented by a parity check matrix initial value table, and the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

1860 2354 3967 4292 4488 5243 5373 5766 8378 9111 10468
10505 10774

24 2266 2389 3232 4255 4779 8729 9140 9566 10102 10661
10711 10797

605 650 1108 1669 2251 3133 5847 6197 6902 7545 10521
10600 10773

1916 1428 1612 2335 3102 3810 4926 5953 9964 10246
10569 10734 10784

3195 6308 8029 9030 9397 9461 9833 10239 10499 10675
10736 10757 10773

2 27 3641 4566 7332 9318 9323 9916 10365 10438 10561
10581 10750

2405 2458 4820 6232 6254 6347 7139 7474 8623 8779 8798
10747 10794

3164 4736 6474 7162 7420 7517 7835 8238 8412 8489 9006
10113 10440

20 2372 5361 5649 6967 8393 8505 9181 9567 9595 10388
10483 10714

1071 2499 5115 5780 8616 7111 7778 8582 9015 9912 10139

10387 10768

292 2833 5490 6011 6136 6713 7517 9096 10128 10328

10407 10525 10736

1044 3711 4421 5140 5207 8118 8749 8884 9205 10359

10372 10746 10784

3241 5696 6440 7240 7419 8613 8878 9593 9959 9997 10401

10404 10754

3133 4647 5912 6065 6624 7208 7346 8227 9465 9739 10432

10516 10770

2254 6444 7449 8095 8120 8710 9030 9162 9643 9968 10101

10571 10678

918 1445 2217 4262 4623 5401 5749 7446 7907 9539 10125

10514 10726

6 1341 1788 3165 4359 5263 5470 7552 8249 8644 10609

10674 10733

1694 3060 3151 3173 7742 8335 8438 8741 9232 9296 9817

10023 10257

467 1674 3016 3950 4055 5399 6688 7113 7273 8658 8702

9642 10545

2007 2541 3123 7380 7550 8122 8501 8665 9882 10403

10519 10594 10696

334 587 709 1540 2023 2876 6216 8768 9328 9481 10424

10567 10779

2165 4185 4306 5019 6961 7386 8447 9082 9837 10091

10461 10559 10570

7 903 2948 6312 6654 7738 7980 8312 9104 9743 10070
10278 10406
3047 3154 4160 4378 5467 8711 8809 9040 9173 9252 9537
9995 10735
2018 2355 3828 3854 6201 6696 8313 8459 8550 8833 9586
10202 10224
1402 1908 4286 4660 6029 6115 6737 7538 9495 9517 10055
10509 10644
3442 3589 3868 5051 5322 5580 8725 9046 9170 10041
10613 10681 10689
2733 7826 10622
3597 4753 7086
1394 7297 10264
2848 7502 10304
1649 2405 10783
647 2911 9069
2572 4006 7508
1361 8887 10103
3681 4023 9090
1496 4962 6325
2016 5120 9747
3954 5260 8568
3364 8710 10035
4208 4806 9973
23 1361 3490

1835 2317 10436
7312 8177 9041
7728 8097 10761
2109 7902 9685
5424 8943 9436
4369 7643 9152
2240 10140 10528
3435 6124 10604
8962 9357 10040
26 1931 8629
8275 10455 10643
8 24 4952
3995 6456 10633
28 10300 10337
4894 9286 9429
5587 6721 9120
1859 9198 9762
6374 6453 7011
1319 4530 5442
1507 10711 10798
2115 2445 3641
6668 9139 10163
4038 8117 10295
1479 2403 8247
2522 2936 3562

1526 5073 9650
2136 9820 10636
4214 8464 9391
8018 10330 10610
8984 10209 10647
3414 7272 8599
4883 9077 9525
22 8173 8425
2941 6536 10126
29 6540 7361
5 3787 10468
4264 4818 6906
3903 7041 10412
6078 7661 10619
6922 9723 9890
5132 5416 6253
5925 9961 10447
9 10311 10598
8790 8814 10793
4768 5466 10664
19 10675 10766
6814 8705 10737
17 769 6692
1503 10696 10742
1285 4632 8976

4273 4973 7907
4650 4775 10785
28 729 10331
1914 5240 10723
3569 4921 9561
4 9442 10796
494 2328 9507
1717 8768 10750
9540 10599 10774
11 10075 10644
10246 10607 10753
5510 7088 9053
1347 3584 5523
7872 10596 10736
628 10592 10695
5632 5688 10627
2375 10009 10561
4169 4630 8871
2896 10038 10521
89 9695 9799
20 7563 9069
4534 10421 10697
9212 9868 10716
7485 9312 10327
234 536 6293

5515 7350 9251
283 3182 7167
2444 5378 6130
6183 8315 10726
43 4871 8347
2427 10219 10728
10 21 9448
1067 8312 8420
4793 9522 10105
4688 10536 10724
3825 7496 10709
682 8544 10449
2794 7110 10741
9279 10741 10767
2897 5442 8771
33 7957 10460
5 10393 10792
6225 10224 10798
23 9014 10786
7836 8339 8642
3476 5455 9788
1939 10251 10384
4008 7890 10450
926 2090 3804
1038 2497 10701

22 6220 8405
5153 5944 10367
7260 7726 9529
3039 8397 10665
7262 9644 10083
5531 6248 10795
7926 8248 8413
4649 8971 10182.

[0053]

A data processing apparatus according to a ninth aspect or data processing method according to a tenth aspect of the present invention includes an encoding unit configured to encode or an encoding step of encoding information bits into an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 26/30 on the basis of a parity check matrix of the LDPC code, wherein the LDPC code includes information bits and parity bits, the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits, the information matrix portion is represented by a parity check matrix initial value table, and the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

142 2307 2598 2650 4028 4434 5781 5881 6016 6323 6681

6698 8125

2932 4928 5248 5256 5983 6773 6828 7789 8426 8494 8534

8539 8583

899 3295 3833 5399 6820 7400 7753 7890 8109 8451 8529

8564 8602

21 3060 4720 5429 5636 5927 6966 8110 8170 8247 8355

8365 8616

20 1745 2838 3799 4380 4418 4646 5059 7343 8161 8302

8456 8631

9 6274 6725 6792 7195 7333 8027 8186 8209 8273 8442

8548 8632

494 1365 2405 3799 5188 5291 7644 7926 8139 8458 8504

8594 8625

192 574 1179 4387 4695 5089 5831 7673 7789 8298 8301

8612 8632

11 20 1406 6111 6176 6256 6708 6834 7828 8232 8457 8495

8602

6 2654 3554 4483 4966 5866 6795 8063 8249 8301 8497

8509 8623

21 1144 2355 3124 6773 6805 6987 7742 7994 8358 8374

8580 8611

335 4473 4823 5528 6096 7543 7586 7921 8197 8319 8394

8489 8636

2919 4531 4419 4735 6366 6393 6844 7193 8165 8205 8544

8586 8617

12 19 742 930 3009 4330 6213 6224 7292 7430 7792 7922
8137
710 1439 1588 2434 3516 5239 6248 6827 8230 8448 8515
8581 8619
200 1075 1868 5581 7349 7642 7698 8037 8201 8210 8320
8391 8526
3 2501 4252 5256 5292 5567 6136 6321 6430 6486 7571
8521 8636
3062 4599 5885 6529 6616 7314 7319 7567 8024 8153 8302
8372 8598
105 381 1574 4351 5452 5603 5943 7467 7788 7933 9362
8513 8587
787 1857 3396 3659 6550 7131 7965 8015 8040 8312 8484
8525 8537
15 1113 4226 5197 5575 5761 6762 7038 8260 8338 8444
8512 8568
36 5216 5368 5616 6029 6591 8038 8067 8299 8351 8565
8578 8585
1 23 4300 4530 5426 5532 5817 6967 7124 7979 9022 9270
8417
629 2133 4828 5475 5875 5890 7124 8042 8345 8385 8518
8598 8612
11 1065 3782 4227 4993 7104 7863 7904 8104 8228 8321
8383 8565
2131 2274 3168 3215 3220 5597 8347 7812 8238 8354 8527

8557 8614

5600 6591 7491 7696

1766 8281 8626

1725 2280 5120

1650 3445 7652

4312 6911 8626

15 1013 5892

2263 2546 2979

1545 5873 7406

67 726 3697

2860 6443 8542

17 911 2820

1561 4580 6052

79 5269 7134

22 2410 2424

3501 5642 8627

808 6250 8571

4099 6389 7482

4023 5000 7833

5476 5765 7917

1009 3194 7207

20 495 5411

1703 8388 8635

6 4395 4921

200 2053 8206

1089 5126 5562

10 4193 7720

1967 2151 4608

22 738 3513

3385 5066 8152

440 1118 8537

3429 6058 7716

5213 7519 8382

5564 8365 8620

43 3219 8603

4 5409 5815

5 6376 7654

4091 5724 5953

5348 6754 8613

1634 6398 6632

72 2058 8605

3497 5811 7579

3846 6743 8559

15 5933 8629

2133 5859 7068

4151 4617 8566

2960 8270 8410

2055 3617 8210

544 1441 6835

4043 7482 8592

294 2180 8524
3058 8227 8373
364 5756 8617
5383 8555 8619
1704 2480 4181
7338 7929 7990
2615 3905 7981
4298 4548 8296
8262 8319 8630
892 1893 8028
5694 7237 8595
1487 5012 5810
4335 8593 8624
3509 4531 5273
10 22 830
4161 5208 6280
275 7063 8634
4 2725 3113
2279 7403 8174
1637 3328 3930
2810 4939 5624
3 1234 7687
2799 7740 8616
22 7701 8636
4302 7857 7991

7477 7794 8592

9 6111 8591

5 8606 8628

347 3497 4033

1747 2613 8636

1827 5600 7042

580 1822 6842

232 7134 7783

4629 5000 7231

951 2806 4947

571 3474 8577

2437 2496 7945

23 5873 8162

12 1168 7686

8315 8540 8596

1766 2506 4733

929 1516 3338

21 1216 6355

782 1452 8617

8 6083 6087

667 3240 4583

4030 4661 5790

559 7122 8553

3292 4388 4909

2532 3673 8594

1991 3954 6206
6835 7900 7980
139 5722 8573
2680 4928 4998
243 2579 7735
4281 8132 8566
7656 7671 8609
1116 2291 4166
21 388 8021
6 1123 8369
311 4919 8511
0 3248 6290
13 6762 7172
4209 5632 7563
49 127 8074
581 1735 4075
0 2235 5470
2178 5820 6179
16 3575 6054
1095 4564 6458
9 1581 5953
2537 6469 8532
14 3874 4844
0 4269 3551
2114 7272 7926

1875 2388 4057

3232 4042 6663

9 401 583

13 4100 6584

2299 4190 4410

21 3670 4979.

[0054]

A data processing apparatus according to an eleventh aspect or data processing method according to a twelfth aspect of the present invention includes a decoding unit configured to decode or a decoding step of decoding an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 26/30 on the basis of a parity check matrix of the LDPC code, wherein the LDPC code includes information bits and parity bits, the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits, the information matrix portion is represented by a parity check matrix initial value table, and the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

142 2307 2598 2650 4028 4434 5781 5881 6016 6323 6681
6698 8125

2932 4928 5248 5256 5983 6773 6828 7789 8426 8494 8534

8539 8583

899 3295 3833 5399 6820 7400 7753 7890 8109 8451 8529

8564 8602

21 3060 4720 5429 5636 5927 6966 8110 8170 8247 8355

8365 8616

20 1745 2838 3799 4380 4418 4646 5059 7343 8161 8302

8456 8631

9 6274 6725 6792 7195 7333 8027 8186 8209 8273 8442

8548 8632

494 1365 2405 3799 5188 5291 7644 7926 8139 8458 8504

8594 8625

192 574 1179 4387 4695 5089 5831 7673 7789 8298 8301

8612 8632

11 20 1406 6111 6176 6256 6708 6834 7828 8232 8457 8495

8602

5 2654 3554 4483 4966 5866 6795 8059 8249 8301 8497

8509 8625

21 1144 2355 3124 6773 6805 6887 7742 7994 8358 8374

8580 8611

335 4475 4883 5528 6096 7543 7525 7921 8197 8319 8394

8489 8636

2919 4331 4419 4735 6366 6393 6844 7193 8165 8205 8544

8386 8617

12 19 742 930 3009 4330 6213 6224 7292 7430 7792 7922

8137

710 1439 1588 2434 3516 5239 6248 6827 8230 8448 8515
8581 8619
200 1075 1868 5581 7349 7642 7698 8037 8201 8210 8320
8391 8526
3 2501 4252 5256 5292 5567 6136 6321 6430 6486 7571
8521 8636
3062 4599 5885 6529 6616 7314 7319 7567 8024 8153 8302
8372 8598
105 381 1574 4351 5452 5603 5943 7467 7788 7933 8362
8513 8587
787 1857 3386 3659 6550 7131 7965 8015 8040 8312 8484
8525 8537
15 1118 4226 5197 5575 5761 6762 7038 8260 8338 8444
8512 8568
36 5216 5368 5616 6029 6591 8038 8067 8299 8351 8565
8578 8585
1 23 4300 4530 5426 5532 5817 6967 7124 7979 8022 8270
8437
629 2133 4828 5475 5875 5890 7194 8042 8345 8385 8518
8598 8612
11 1065 3782 4237 4993 7104 7863 7904 8104 8228 8321
8383 8565
2131 2274 3168 3215 3220 5597 6347 7812 8238 8354 8527
8557 8614
5600 6591 7491 7696

1766 8281 8626

1725 2280 5120

1650 3445 7652

4312 6911 8626

15 1013 5892

2263 2546 2979

1545 5873 7406

67 726 3697

2860 6443 8542

27 911 2820

1561 4580 6052

79 5269 7134

22 2410 2424

3501 5642 8627

808 6950 8571

4099 6389 7482

4023 5000 7833

5476 5765 7917

1008 3194 7207

20 495 5411

1703 8388 8635

6 4395 4421

200 2053 8206

1089 5126 5562

10 4193 7720

1967 2151 4608

22 738 3513

3385 5066 8152

440 1118 8537

3429 6058 7716

5213 7519 8382

5564 8365 8620

43 3219 8603

4 5409 5815

5 6376 7654

4091 5724 5953

5348 6754 8613

1634 6398 6632

72 2058 8605

3497 5811 7579

3846 6743 8559

15 5933 8629

2133 5859 7068

4151 4617 8566

2960 8270 8410

2059 3617 8210

544 1441 6895

4943 7482 8592

294 2180 8524

8658 8227 8373

364 5756 8617
5383 8555 8619
1704 2480 4181
7338 7929 7990
2615 3905 7981
4298 4548 8296
8262 3319 8630
892 1893 8028
5694 7237 8595
1487 5012 5810
4335 8593 8624
3509 4531 5273
10 22 830
4151 5208 6280
275 7063 8634
4 2725 3113
2279 7403 8174
1637 3328 3930
2810 4939 5624
3 1234 7687
2799 7740 8616
22 7701 8636
4302 7857 7993
7477 7794 8392
9 6111 8591

5 8606 8628
347 3497 4033
1747 2613 8636
1827 5600 7042
580 1822 6842
232 7134 7783
4629 5000 7231
951 2806 4947
571 3474 8577
2437 2496 7945
23 5873 8162
12 1168 7686
8315 8540 8596
1766 2506 4733
929 1516 3338
21 1216 6555
782 1452 8617
8 6083 6087
667 3240 4583
4030 4661 5790
559 7122 8553
3202 4388 4909
2533 3673 8594
1991 3954 6206
6835 7300 7980

189 5722 8573
2680 4928 4998
243 2579 7735
4281 8132 8566
7656 7671 8609
1116 2291 4166
21 388 8021
6 1123 8369
311 4918 8511
0 3248 6290
13 6762 7172
4209 5632 7563
49 127 8074
581 1735 4075
0 2235 5470
2178 5820 6179
16 3575 6054
1093 4564 6458
9 1581 5953
2537 6469 8552
14 2874 4844
0 3269 3551
2114 7372 7926
1875 2388 4057
3232 4042 6463

9 401 583
13 4100 6584
2299 4190 4410
21 3670 4979.

[0055]

A data processing apparatus according to a thirteenth aspect or data processing method according to a fourteenth aspect of the present invention includes an encoding unit configured to encode or an encoding step of encoding information bits into an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 27/30 on the basis of a parity check matrix of the LDPC code, wherein the LDPC code includes information bits and parity bits, the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits, the information matrix portion is represented by a parity check matrix initial value table, and the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

658 706 898 1149 2577 2622 2772 3266 3329 5243 6079
6271
289 784 1682 3584 3995 4821 4856 5063 5974 6168 6437
6453
658 1426 2043 2065 2986 4118 4284 5394 5444 5477 5727

6018

641 928 1225 2841 4052 4840 4992 5268 5533 6249 6461

6475

2312 2917 3713 3849 4059 4241 4610 5440 5727 6101 6397

6144

1165 1592 1891 2154 3981 4817 5181 5748 5788 6012 6266

6350

13 2758 3069 4233 4697 5100 5279 5677 5919 5969 6280

6422

818 1500 2125 2340 3774 4707 4901 5170 5744 6008 6316

6353

857 3054 3409 3496 3704 4368 5326 6211 6292 6256 6367

6381

0 7 12 1709 2166 3418 3723 4887 5770 6043 6069 6431

2481 3379 4650 4900 4919 5060 5410 5423 6056 6173 6283

6386

15 814 854 1871 2934 3387 3915 5180 5393 5442 5581 5663

146 1882 3076 4458 4848 5252 5602 5778 5821 6213 6251

6401

2 947 1419 1566 3437 3646 4615 4634 4735 5819 5943 6280

1731 2309 2920 4158 4185 4298 4711 5082 5757 5762 6204

6269

257 297 337 2733 3230 4134 4430 4749 5295 5689 5921

6262

1436 2151 2629 3217 3930 4078 5386 5739 5906 6146 6225

6366

133 530 2448 4745 5000 5020 5224 5273 6211 6266 6431

6453

13 2644 3895 3898 4485 4722 5142 5462 5951 6031 6084

6351

6 3000 3873 3995 4680 5158 5504 5692 5755 6255 6338

6359

166 465 1658 2549 2941 4244 5071 5149 5452 5874 5939

6038

2309 2937 4282 4628 5113 5454 5731 5825 6021 6171 6402

6472

3 1077 2116 2426 2830 4853 5066 5571 5850 5910 6389

6421

817 1608 2220 2925 3281 4393 5042 5058 5377 5464 5588

6148

1848 3871 4381 4776 5366 5578 5648 6143 6389 6434 6465

6473

1263 1616 3150 3497 3759 4078 5530 5665 5694 5913 6397

6420

11 813 2185 2795 3349 4652 4678 5078 5504 6011 6286

6387

3060 3161 4584 4996 5143 5542 5697 5937 6141 6155 6242

6445

1638 2333 2632 3450 3505 3911 4399 4454 5499 5860 6044

6360

650 1744 4517
5772 6071 6471
3582 3622 5776
6153 6380 6446
3977 5932 6447
2071 4597 4891
11 1428 3776
1111 3874 5048
1410 2144 4445
4681 5481 6462
4044 5037 5497
2716 2891 6411
3299 4384 6224
1843 6087 6400
4664 5009 5856
1548 4383 5055
5172 4190 6373
5899 6443 6470
2572 3647 6240
1295 2158 6466
5604 6269 6368
3 5551 6434
3325 5737 6261
666 1397 5538
3069 4274 6410

4042 5992 6437

743 3075 3447

1344 2725 6386

283 2808 6303

2 4627 4632

26 1565 4000

4012 4946 6472

1629 6158 6467

6300 6351 6376

2969 4344 4440

2317 3115 4832

2099 5263 6285

2409 5868 5997

3752 4200 6350

3125 5841 6142

1 2242 6328

16 2525 6379

3198 5269 5960

4 1705 2069

990 4948 5520

1664 3836 4521

1765 4110 6454

9 1373 6387

1969 2405 6368

623 1428 3946

3111 6380 6436

1861 5611 5934

9 2444 3081

5 5508 6317

3184 4988 5995

1060 4803 6400

5021 5826 6289

1608 4754 5648

4702 6391 6421

3899 4811 6128

927 2286 5313

4123 6181 6453

2893 4150 5261

605 4332 5094

17 3518 6358

2858 6126 6478

15 1316 6465

2 2032 2983

5249 6340 6427

3 5003 6200

4478 6315 6420

5158 6390 6447

2598 3229 5399

3747 6424 6446

1412 2453 6332

5256 5715 6455

2137 3421 4368

15 3880 5245

17 3156 5638

3227 3798 6230

2094 3129 6456

1412 5573 5932

175 1182 6304

3555 6407 6463

583 1654 6339

14 6261 6449

3553 5383 5679

2092 2744 4153

0 4465 6472

11 3840 4354

17 5457 6222

1467 6083 6220

3449 3858 6337

3782 5318 6426

417 5038 5790

3571 5638 5873

6117 6241 6476

1898 5680 6219

3235 3817 6429

2095 4194 6224

2 4092 6448
5 6330 6383
285 5075 6334
10 505 2867
1183 5956 6466
839 4716 6471
984 3254 6432
1501 4790 6465
8 1457 1707
1660 1969 6438
4349 6182 6305
1423 3848 5490
1651 2969 6345
344 4164 6298
2397 6027 6274
2233 2778 6161
13 1778 2977
9 1916 3377
0 3 6190
395 4893 6394
3512 4098 6400
3490 6281 6473
12 1359 6465
4202 5179 6412
3007 3542 4271

2400 3350 6351

7 5490 5716

4695 5231 6266

777 6292 6402

919 4851 6367

6 644 3893

5386 6190 6434

17 169 4896.

[0056]

A data processing apparatus according to a fifteenth aspect or data processing method according to a sixteenth aspect of the present invention includes a decoding unit configured to decode or a decoding step of decoding an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 27/30 on the basis of a parity check matrix of the LDPC code, wherein the LDPC code includes information bits and parity bits, the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits, the information matrix portion is represented by a parity check matrix initial value table, and the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

658 706 898 1149 2577 2622 2772 3266 3329 5243 6079

6271

289 784 1682 3584 3995 4821 4856 5063 5974 6168 6437

6453

658 1426 2043 2065 2986 4118 4284 5394 5444 5477 5727

6018

641 928 1225 2841 4052 4840 4992 5268 5533 6249 6461

6475

2312 2917 3713 3849 4059 4241 4610 5440 5727 6101 6397

6444

1165 1592 1891 2154 3981 4817 5181 5748 5788 6012 6266

6350

13 2758 3069 4233 4697 5100 5279 5677 5919 5969 6280

6422

818 1500 2125 2340 3774 4707 4901 5170 5744 6008 6316

6353

857 3054 3409 3496 3704 4868 5326 6211 6292 6356 6367

6381

0 7 12 1709 2166 3418 3723 4887 5770 6043 6069 6431

2481 3379 4650 4900 4919 5060 5410 5425 6056 6173 6283

6386

15 814 854 1271 2934 3387 3915 5180 5303 5442 5581 5665

146 1882 3076 4458 4848 5252 5602 5778 5821 6213 6251

5401

2 947 1419 1566 3437 3646 4615 4634 4735 5819 5943 6280

1231 2309 2920 4158 4185 4298 4711 5082 5757 5782 6204

6209

257 297 337 2783 3230 4134 4480 4749 5295 5680 5921

6202

1436 2151 2629 3217 3930 4078 5386 5799 5906 6146 6226

6366

133 530 2448 4745 5000 5020 5224 5273 6211 6266 6431

6453

13 2644 3895 3898 4485 4722 5142 5462 5951 6031 6084

6351

6 3000 3873 3995 4680 5158 5504 5692 5755 6255 6338

6359

166 465 1658 2549 2941 4244 5071 5149 5452 5874 5939

6038

2309 2937 4282 4628 5113 5454 5731 5825 6021 6171 6402

6472

3 1077 2116 2426 2830 4853 5066 5571 5850 5916 6389

6421

817 1608 2229 2925 3281 4393 5042 5058 5377 5464 5588

6443

1842 3871 4381 4776 5366 5578 5648 6143 6389 6434 6465

6473

1263 1616 3150 3497 3759 4078 5530 5669 5694 5913 6397

6420

11 813 2185 2795 3349 4652 4678 5078 5564 6011 6286

6387

3060 3161 4584 4996 5143 5542 5697 5937 6141 6155 6342
6445
1638 2333 2632 3450 3505 3911 4399 4454 5499 5860 6044
6360
650 1744 4517
5772 6071 6471
3582 3622 5776
6153 6380 6446
3977 5932 6447
2071 4597 4891
11 1428 3776
1111 3874 5048
1410 2144 4445
4681 5481 6462
4044 5037 5437
2716 2891 6411
3209 4384 6224
1843 6087 6460
4664 5009 5856
1548 4383 5055
3172 4190 6373
5899 6443 6470
2572 3647 6240
1295 2158 6466
5604 6269 6368

3 5551 6454
3325 5797 6261
666 1397 5538
3069 4274 6410
4042 5992 6437
743 3075 3447
1344 2725 6386
263 2808 6303
2 4627 4632
26 1565 4000
4012 4946 6472
1629 6158 6467
6300 6351 6376
2969 4344 4440
2317 3115 4832
2099 5263 6285
2409 5868 5997
3752 4200 6350
3125 5841 6142
1 2249 6328
16 2526 6379
3198 5269 5960
4 1705 2069
990 4948 5520
1664 3836 4521

1765 4110 6454

9 1373 6387

1969 2405 6368

623 1428 3946

3111 6380 6436

1861 5611 5934

9 2444 3091

5 5508 6317

3184 4988 5995

1060 4803 6400

5021 5826 6289

1608 4754 5648

4702 6391 6421

3899 4811 6128

927 2286 5213

4123 6181 6453

2893 4150 5261

605 4332 5094

17 3518 6358

2858 6128 6473

15 1316 6465

2 2032 2983

5249 6340 6427

5 6003 6200

4478 6315 6420

5158 6390 6447

2598 3229 5399

3747 6424 6446

1412 2453 6332

5256 5715 6455

2137 3421 4368

15 3880 5245

17 3156 5638

3227 3798 6230

2094 3129 6458

1412 5573 5932

175 1182 6304

3555 6407 6463

583 1654 6339

14 6261 6449

3553 5383 5679

2092 2744 4153

0 4466 6472

11 3840 4354

17 5457 6222

1467 6083 6220

3449 3858 6337

3782 5318 6426

417 5038 5790

3571 5638 5873

6217 6241 6476

1898 5680 6219

3235 3817 6429

2095 4194 6224

2 4092 6448

5 6330 6383

285 5075 6334

10 505 2867

5183 5956 6466

839 4716 6471

984 3254 6432

1501 4790 6465

8 1457 1707

1660 1969 6438

4349 6182 6305

1423 3848 5490

1651 2969 6345

344 4164 6298

2397 6027 6274

2233 2778 6161

13 1778 2977

9 1916 3377

0 2 6190

395 4893 6394

3512 4398 6406

3490 6281 6473
12 1359 6465
4202 5179 6412
3007 3542 4271
2400 3350 6351
7 5490 5716
4695 5231 6266
777 6292 6402
919 4851 6367
6 644 3893
5386 6190 6434
17 169 4896.

[0057]

A data processing apparatus according to a seventeenth aspect or data processing method according to an eighteenth aspect of the present invention includes an encoding unit configured to encode or an encoding step of encoding information bits into an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 28/30 on the basis of a parity check matrix of the LDPC code, wherein the LDPC code includes information bits and parity bits, the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits, the information matrix portion is represented by a parity check matrix initial value table, and the parity check matrix

initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

85	314	1602	1728	1929	2295	2729	2924	3779	4054	4276
918	1378	1838	1903	2399	2524	2937	3615	3740	4140	4213
1361	1430	2639	2648	2910	3418	3511	3543	4177	4209	4248
472	1143	1318	1545	1830	2228	2249	2256	3626	3839	3991
226	1401	2154	2318	2851	3317	3468	3944	3983	4047	4093
490	1145	1247	1851	2671	2776	3152	3229	3345	3758	3786
522	1393	1473	2196	2707	3052	3398	3814	3827	4148	4301
417	1982	2176	2336	2459	2806	3005	3771	3870	4080	4243
112	1040	1596	1621	1685	2118	2571	3359	3945	4034	4171
646	1705	2181	2439	2808	2851	2987	3044	3494	4049	4312
6	11	115	245	663	1773	2624	3444	3601	3952	4246
11	541	1020	1326	2259	2347	2750	2861	3328	3428	4126
515	941	1233	1804	2295	2528	3265	3826	4002	4022	4224
46	484	679	1949	2342	2929	3555	3860	3918	4068	4113
1832	2023	2279	2376	2965	3276	3318	3549	3640	3843	3910
241	943	1222	1583	1637	2745	3338	4080	4086	4203	4306
11	1419	1841	2398	2920	3409	3703	3768	3878	4052	4254
878	2049	2123	2431	2657	2704	3135	3342	3726	4141	4162
16	837	1267	1410	2100	2026	3099	3107	4042	4129	4157
133	646	1367	1394	2118	2311	2676	2956	3195	3536	3657
696	1444	2129	2432	2494	2793	2947	3852	3985	4254	4319
11	1076	1618	1925	2332	2743	2934	3009	3163	4169	4188

14 20 808 2629 2681 3090 3491 3835 4017 4068 4083
433 1386 2416 2570 2950 3611 3869 3969 4248 4251 4316
384 1292 1534 2610 2617 3559 3638 3964 4131 4293 4313
271 564 1719 2288 2597 2674 3429 3455 3793 4074 4286
133 190 815 955 1485 2000 2860 3000 3734 4013 4287
559 771 1762 2537 2764 2816 3186 3806 3933 4224 4271
11 733 1198 1735 1856 2668 2754 3216 4070 4113 4311
4 806 1832 2047 2058 2724 3387 3793 3833 4005 4319
506 1456 2339 3069 3343 3442 3889 3939 4013 4212 4278
2038 3980 4313
64 2373 4080
800 1535 4166
1030 3759 4002
1687 3269 4225
1213 2632 3878
719 2916 4277
1261 1930 3459
777 1568 1914
4 397 3290
10 3451 4115
3629 3985 4155
2652 3668 4026
135 3172 4319
1426 1970 3657
199 1268 2064

570 845 2761
41 1067 3498
1588 2482 2750
1615 2013 2715
121 1812 2588
10 992 1082
1929 4225 4279
6 1967 3760
593 1812 4107
891 2146 4158
924 2282 3585
592 2971 4235
260 3493 4313
2423 3180 3449
2042 3118 3625
2877 3064 3882
7 2139 4316
4 7 2954
1398 3947 4272
3675 4253 4318
1561 1977 2432
2531 4192 4209
1032 1102 4268
75 1718 3438
925 1073 4171

2124 2762 4148

4 3455 4069

3 1279 3382

1277 1746 3969

2727 3127 4230

584 1108 3454

9 2057 3061

1608 4193 4310

2673 3164 3713

1379 4072 4318

959 3447 4146

2509 4255 4296

819 1352 3371

3562 3865 4041

940 1217 3607

114 2544 4310

4 2178 4213

2035 4246 4251

272 1236 2733

953 2762 4115

1853 3496 4309

1119 3740 4318

2051 4058 4317

0 3162 4207

2389 4034 4111

4 3395 4301
3716 4089 4198
6 4272 4311
1 4 1854
4238 4299 4305
7 10 3737
11 3764 4296
297 1912 4117
1087 1796 4056
2153 3882 4030
962 4043 4203
243 3841 4306
2183 3886 4216
943 1974 2897
278 3224 3933
3 4196 4245
3409 4301 4315
2 2176 3214
462 3293 4008
478 2178 4202
3593 3825 4216
115 2796 4225
3827 4196 4251
1375 4301 4306
296 407 2955

688 3913 4281
3446 3840 4314
1073 3444 4146
1556 2761 3391
2 3543 4264
1378 3347 4305
847 1952 2745
1 1743 4042
2087 3048 4254
1010 4073 4132
2610 4129 4152
4106 4120 4312
7 4282 4304
3885 4227 4219
1235 4105 4195
1700 2332 4224
9 3750 4282
1539 4013 4310
3734 3834 4011
1397 2758 3645
7 1000 2984
11 3433 4068
1139 1800 3352
8 546 2561
1 4209 4239

2366 4063 4282
279 2524 2533
657 1913 4006
2322 2623 2960
758 803 2304
9 13 4241
3887 4299 4318
2612 3830 4230
1300 1596 2155
3622 3671 4230
2491 3722 3977
735 3812 4201
3204 3796 4317
2727 4292 4305
1062 2676 4255
2777 3131 4286
2518 3352 3937
4225 4255 4317
3644 3822 4311
1853 3754 4094
599 2608 3276.

[0058]

A data processing apparatus according to a nineteenth aspect or data processing method according to a twentieth aspect of the present invention includes a decoding unit configured to decode or a decoding step of decoding an LDPC

(Low Density Parity Check) code having a code length of 64800 bits and a code rate of 28/30 on the basis of a parity check matrix of the LDPC code, wherein the LDPC code includes information bits and parity bits, the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits, the information matrix portion is represented by a parity check matrix initial value table, and the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

85	314	1602	1728	1929	2295	2729	2924	3779	4054	4276
918	1378	1938	1903	2399	2524	2937	3615	3740	4140	4213
1361	1430	2639	2648	2910	3418	3511	3543	4177	4209	4248
472	1143	1318	1545	1830	2228	2249	2256	3626	3839	3991
226	1401	2154	2318	2851	3317	3468	3944	3983	4047	4093
490	1145	1247	1851	2671	2776	3152	3229	3345	3759	3786
522	1393	1473	2196	2707	3052	3398	3814	3827	4148	4301
417	1982	2176	2336	2459	2806	3005	3771	3870	4080	4243
112	1040	1596	1621	1685	2113	2571	3359	3945	4034	4171
546	1705	2181	2439	2808	2851	2987	3044	3494	4049	4312
6	11	115	245	663	1773	2624	3444	3601	3952	4246
11	541	1020	1326	2259	2347	2750	2861	3328	3428	4126
515	941	1232	1804	2295	2528	3265	3826	4002	4022	4224

46 484 679 1949 2342 2929 3555 3860 3918 4068 4113
1832 2023 2279 2376 2965 3278 3318 3549 3640 3843 3910
241 943 1222 1583 1637 2745 3338 4080 4086 4202 4300
11 1419 1841 2398 2920 3409 3703 3768 3878 4052 4254
878 2049 2123 2431 2657 2704 3135 3342 3728 4141 4162
16 837 1267 1410 2100 3026 3099 3107 4042 4129 4157
133 646 1367 1394 2118 2311 2676 2956 3195 3536 3657
698 1444 2129 2432 2494 2793 2947 3852 3985 4254 4319
11 1076 1618 1995 2332 2743 2934 3009 3565 4169 4188
14 20 808 2629 2681 3090 3491 3835 4017 4068 4083
433 1386 2416 2570 2950 3611 3869 3969 4248 4251 4316
384 1292 1534 2610 2617 3559 3638 3964 4131 4293 4313
271 564 1719 2388 2597 2674 3429 3455 3793 4074 4286
133 190 815 955 1485 2000 2860 3000 3734 4013 4287
559 771 1762 2537 2764 2816 3186 3806 3933 4224 4271
11 733 1198 1735 1856 2668 2754 3216 4070 4113 4311
4 806 1832 2047 2058 2724 3387 3793 3833 4005 4319
506 1456 2339 3069 3343 3442 3889 3939 4013 4212 4278
2038 3980 4313
64 2373 4080
800 1535 4166
1030 3759 4002
1687 3269 4225
1219 2632 3878
119 2916 4277

1261 1930 3459

777 1568 1914

4 397 3290

10 3451 4115

3629 3885 4155

2652 3668 4026

135 3172 4319

1426 1970 3657

199 1268 2064

570 845 2761

41 1067 3498

1588 2482 2750

1615 2013 2715

121 1812 2588

10 992 1082

1929 4225 4279

6 1957 3760

593 1812 4107

891 2146 4158

324 2282 3585

592 2971 4235

260 3493 4313

2423 3180 3449

2042 3118 3625

2877 3064 3892

7 2139 4316
4 7 2954
1398 3947 4272
3675 4253 4318
1561 1977 2432
2531 4192 4209
1032 1102 4268
75 1718 3438
925 3073 4171
2124 2782 4148
4 3455 4069
3 1279 3382
1277 1746 3969
2727 3127 4230
584 1108 3454
9 2057 3061
1698 4103 4310
2673 3164 3713
1379 4072 4318
950 3447 4146
2509 4255 4296
819 1352 3371
3562 3865 4041
940 1217 3607
114 2544 4310

4 2178 4213
2035 4246 4251
272 1236 2733
953 2762 4115
1853 3496 4309
1119 3740 4318
2051 4058 4317
0 3162 4207
2389 4034 4111
4 3395 4301
3716 4089 4198
6 4272 4311
1 4 1854
4238 4299 4305
7 10 3737
11 3764 4296
297 1912 4117
1987 1796 4056
2153 3882 4030
962 4043 4203
243 3841 4308
2183 3886 4216
943 1974 2897
278 3224 3933
3 4196 4245

3409 4301 4315

2 2176 3214

462 3203 4008

478 2178 4202

3593 3825 4216

115 2796 4225

3827 4196 4251

1375 4301 4306

296 407 2055

688 3913 4281

3446 3840 4314

1073 3444 4146

1556 2761 3391

2 3543 4264

1378 3347 4305

847 1952 2745

1 1743 4042

2087 3048 4254

1010 4073 4132

2610 4129 4152

4106 4120 4313

7 4282 4304

3885 4227 4319

1235 4105 4195

1700 2332 4224

9 3750 4282
1539 4013 4310
3734 3834 4011
1397 2758 3645
7 1000 2984
11 3433 4068
1139 1800 3352
8 546 2561
1 4209 4239
2366 4063 4282
279 2524 2533
657 1913 4006
2322 2623 2960
758 303 2304
9 13 4241
3887 4299 4318
2612 3830 4230
1300 1596 2155
3622 3671 4230
2491 3722 3977
735 3812 4201
3204 3796 4317
2727 4292 4305
1062 2676 4255
2777 3131 4286

2518 3352 3937

4225 4255 4317

3644 3822 4311

1853 3754 4094

599 2608 3276.

[0059]

An data processing apparatus according to a twenty-first aspect or data processing method according to a twenty-second aspect of the present invention includes an encoding unit configured to encode or an encoding step of encoding information bits into an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 29/30 on the basis of a parity check matrix of the LDPC code, wherein the LDPC code includes information bits and parity bits, the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits, the information matrix portion is represented by a parity check matrix initial value table, and the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

212 499 911 940 1392

316 563 1527 2006 2077

2 1906 2043 2112 2123

537 901 1582 1812 1955

5 978 1280 1933 2145
5 2035 2044 2108 2121
5 939 1874 1974
4 1069 1758
694 2096 2106
1129 1511 1659
1564 2089 2159
2 1605 2004
474 1341 2003
103 2128 2150
1656 1993 2153
1881 2122 2138
1088 1968 2141
1 298 2073
1042 1724 2137
1253 1758 2145
1209 1566 2123
1466 2116 2155
43 2006 2049
592 1806 1865
3 143 2149
1158 1443 2002
1422 2152 2157
485 2119 2150
571 1831 2086

204 2042 2151

174 544 974

1469 1795 1995

13 708 1683

5 1144 2030

486 1309 1576

165 2030 2147

504 2073 2126

263 565 1798

239 861 1861

862 1610 1716

1346 1971 2128

5 804 1399

2139 2144 2155

4 2136 2159

1485 2059 2158

50 1091 1332

373 1730 2092

59 1086 1401

1166 1781 2065

213 2080 2154

492 1905 2110

1 1517 2126

122 1427 2146

885 991 1842

3 278 1806
967 1354 1907
1697 2047 2156
684 1924 2151
2077 2122 2157
978 2054 2135
435 2034 2150
136 1997 2125
1504 1850 2153
1404 1989 2119
109 1001 2152
780 1473 2150
198 1723 2062
927 2087 2138
1 666 2018
1293 1960 2141
1648 2033 2144
681 1578 1999
1342 2022 2157
949 1907 1994
138 1261 2135
3 608 982
1211 1501 2150
201 328 1186
1295 2089 2132

267 556 2142
801 2052 2122
1382 2135 2155
572 1503 1704
346 1183 2129
1926 2090 2149
1337 2133 2140
5 1806 2125
1383 1628 2068
1193 1626 2138
1999 2115 2146
217 274 2021
3 816 2024
1380 2138 2157
607 1385 2110
184 1195 2063
0 1767 2108
0 2081 2097
1135 2036 2128
1748 2091 2125
797 1552 1926
1046 1890 2128
291 1359 2131
1075 1214 1762
60 149 1943

581 1197 1232
1009 2026 2136
884 2002 2117
1 576 1449
519 1968 2114
5 1489 1630
1926 2037 2158
2 1249 2159
0 811 2114
2055 2152 2159
802 1911 2120
204 1033 2033
1840 2012 2037
1746 2111 2155
1098 1835 2157
2 1492 1831
353 1637 1830
375 1264 2036
2 1638 2035
1096 1971 2021
950 1809 1884
253 467 1600
5 379 1833
4 1698 1970
37 1637 2136

1174 1460 2157

612 1827 2134

1783 1802 1949

2029 2118 2151

1984 2030 2141

2 347 462

862 1693 2121

2 895 1401

4 1901 2100

1183 1674 2069

1575 1940 2158

5 1904 2097

1044 2029 2092

1441 1943 2150

0 3 1300

2 516 1735

503 1342 2019

1421 1914 2131

28 986 1467

1270 1851 1988

481 1265 2016

530 546 909

653 1909 2138

1865 2002 2149

2 1359 1518

1640 2104 2129
1656 2109 2155
1307 1762 2114
565 1647 2118
1690 2081 2156
1 300 1995
5 1681 2151
1602 2050 2156
1 1960 2153
2061 2070 2138
1581 1673 2142
1048 1142 2101
1867 1991 2055
856 1640 1878
251 561 966
343 1816 2114
3 966 2045
1885 1922 2158
57 556 2059
732 1724 2147.

[0060]

A data processing apparatus according to a twenty-third aspect or data processing method according to a twenty-fourth aspect of the present invention includes a decoding unit configured to decode or a decoding step of decoding an LDPC (Low Density Parity Check) code having a code length of

64800 bits and a code rate of 29/30 on the basis of a parity check matrix of the LDPC code, wherein the LDPC code includes information bits and parity bits, the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits, the information matrix portion is represented by a parity check matrix initial value table, and the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

212	499	911	946	1392
316	563	1527	2006	2077
2	1906	2043	2112	2123
537	901	1582	1812	1955
5	978	1280	1933	2145
5	2035	2044	2108	2121
5	939	1874	1974	
4	1069	1758		
694	2096	2106		
1129	1511	1659		
1564	2089	2159		
2	1605	2094		
474	1341	2063		
193	2128	2150		

1656 1993 2153

1881 2122 2138

1088 1968 2141

1 298 2073

1042 1724 2137

1253 1758 2145

1209 1566 2123

1466 2116 2155

43 2006 2049

592 1806 1865

3 143 2149

1158 1448 2002

1422 2152 2157

485 2119 2150

371 1831 2086

204 2042 2151

174 514 974

1469 1795 1993

13 708 1683

5 1144 2030

486 1309 1576

165 2030 2147

504 2073 2126

263 565 1798

222 851 1861

862 1610 1716
1346 1971 2128
5 804 1399
2139 2144 2155
4 2136 2159
1485 2059 2158
50 1091 1332
373 1730 2092
39 1086 1401
1166 1781 2065
213 2080 2154
492 1905 2110
1 1517 2126
722 1427 2146
885 991 1842
3 278 1806
967 1354 1907
1697 2047 2156
684 1924 2151
2077 2122 2157
978 2034 2135
435 2034 2150
136 1997 2125
1504 1850 2153
1404 1989 2119

109 1001 2152

780 1473 2150

198 1723 2062

927 2087 2138

1 666 2018

1293 1960 2141

1648 2033 2144

681 1578 1999

1342 2022 2157

949 1907 1994

138 1261 2135

3 608 982

1211 1501 2150

201 228 1186

1295 2089 2132

267 556 2142

801 2052 2122

1382 2135 2155

572 1503 1704

346 1182 2129

1926 2090 2149

1337 2133 2140

5 1606 2125

1383 1628 2068

1193 1626 2138

1999 2115 2146

217 274 2021

3 816 2024

1380 2138 2157

607 1385 2110

184 1195 2063

0 1767 2108

0 2081 2097

1135 2036 2128

1748 2001 2125

797 1552 1926

1046 1890 2128

291 1859 2131

1073 1214 1762

60 549 1943

581 1197 1232

1009 2026 2136

884 2002 2117

1 576 1449

519 1968 2114

5 1489 1630

1926 2037 2158

2 1249 2159

0 811 2114

2055 2112 2150

802 1911 2120
204 1033 2033
1840 2012 2037
1746 2111 2155
1098 1835 2157
2 1492 1831
353 1537 1830
375 1264 2036
2 1638 2035
1096 1971 2021
950 1809 1884
253 467 1600
5 379 1833
4 1698 1970
37 1637 2136
1174 1460 2157
612 1827 2134
1783 1802 1949
2029 2118 2151
1984 2030 2141
2 347 462
862 1693 2121
2 895 1461
4 1901 2100
1183 1674 2066

1575 1940 2158

5 1904 2097

1044 2029 2092

1441 1943 2150

0 3 1300

2 516 1735

503 1342 2019

1421 1914 2131

28 986 1467

1270 1851 1988

481 1265 2016

530 546 909

653 1909 2158

1805 2002 2149

2 1359 1518

1640 2104 2129

1656 2109 2155

1307 1752 2114

565 1647 2118

1690 2081 2136

1 300 1995

5 1681 2151

1602 2050 2156

1 1960 2153

2061 2070 2132

1581 1673 2142

1048 1142 2101

1867 1991 2055

856 1640 1878

251 561 966

343 1816 2114

3 966 2045

1885 1922 2158

57 556 2059

732 1724 2147.

[0061]

In embodiments of the present invention, information bits are encoded into an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of $24/30$, $25/30$, $26/30$, $27/30$, $28/30$, or $29/30$ on the basis of a parity check matrix of the LDPC code.

[0062]

In embodiments of the present invention, furthermore, an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of $24/30$, $25/30$, $26/30$, $27/30$, $28/30$, or $29/30$ is decoded on the basis of the parity check matrix of an LDPC code.

[0063]

The LDPC code includes information bits and parity bits, the parity check matrix includes an information matrix

portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits, the information matrix portion is represented by a parity check matrix initial value table, and the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns.

[0064]

A parity check matrix initial value table with a code rate of 24/30 includes

1504 2103 2621 2840 3869 4594 5246 6314 7327 7364 10425
11934 12898 12954

27 1903 3923 4513 7812 8098 8428 9789 10519 11345 12032
12157 12573 12930

17 191 660 2451 2475 2976 3398 3616 5769 6724 8641
10046 11552 12842

13 1366 4993 6468 7689 8563 9131 10012 10914 11574
11837 12203 12715 12946

432 872 2603 3286 3306 3385 4137 5563 7540 9339 9948
12315 12656 12929

1113 1394 4104 4186 7240 8827 11522 11833 12359 12363
12629 12821 12964 12946

14 441 1432 1677 2422 8981 11478 11507 12599 12783
12793 12912 12922 12943

1579 1806 7971 8586 9845 10357 11600 12007 12020 12339

12576 12817 12830 12904

20 546 3672 5538 6944 8052 8781 9743 12269 12393 12418
12549 12555 12718

1 3540 4397 5011 6626 8617 9587 10360 10602 11402 11983
12068 12495 12838

30 1572 4908 7421 8041 8910 8963 11005 11930 12240
12340 12467 12892 12933

33 2060 3907 4215 5545 8306 8655 8743 8806 9315 9364
10685 11954 12959

1338 2596 4876 5207 9555 10421 10929 11648 11739 12375
12416 12643 12742 12754

9469 10344 10932 11250 11426 11582 11846 12139 12202
12210 12356 12378 12873 12929

2681 3337 3616 6113 7078 8167 8624 9697 10908 11781
11955 12035 12475 12659

28 4086 5432 6555 6848 7368 8794 11483 11572 12414
12816 12894 12936 12957

5 5044 5572 9023 9192 9589 9979 10009 10855 10991 11715
12314 12610 12945

17 272 602 5681 6530 9572 9886 11061 11495 12238 12265
12483 12685 12955

22 2245 4282 4469 5007 6650 6733 10151 10401 11571
12004 12261 12805 12844

23 3270 4468 5621 9662 11240 11934 12091 12444 12691
12717 12858 12888 12917

740 1519 4923 6191 7878 8350 9293 10779 11020 11287
11630 12792 12862 12920
12 28 3584 6072 7079 8075 10477 11130 11383 11780 12341
12667 12818 12927
14 118 5283 5382 8301 9097 9413 9664 10437 10701 11124
12685 12730 12734
32 1426 3078 4325 5353 7780 9042 9928 10077 10377 10679
11191 11750 12611
1 669 3831 3930 5381 5412 6552 8453 9435 10243 11546
11821 11987 12807
232 483 919 1232 2156 2396 2990 3774 8539 8704 8819
10810 11868 12634
2381 7309 9334
348 6494 12623
4872 6257 11090
7 11970 11985
6615 12789 12855
1173 5269 12647
1944 7738 8116
17 4828 9175
2329 6034 12642
1254 2366 5013
2984 5078 5664
7423 10265 11528
1656 8526 8716

22 287 2837

18 100 3079

299 3171 12169

33 5920 11144

1286 3650 9309

2283 8809 12588

3199 8242 9081

2507 6846 8113

5211 8722 12689

1064 2592 8659

6136 6925 12958

1256 12789 12932

4274 8045 8788

1824 3209 6926

11 8899 12669

6249 6338 8730

641 9679 12831

3459 9876 11165

3226 6148 8173

9078 12126 12771

10907 11278 12732

3392 4020 12838

2814 11588 12909

6063 9214 11519

6064 6827 12683

1610 2452 6582
903 6239 3074
4592 8138 12952
2587 6271 9945
2733 11844 11893
581 4601 10020
14 5597 6049
343 3582 5931
5263 6521 12846
1394 2457 5251
11 4627 12747
2650 10366 12390
6285 11093 12062
10143 12892 12956
3448 11917 12330
4209 11693 12356
1529 2360 9086
5389 8148 10224
64 4876 12862
9483 12659 12887
3587 6767 12478
3122 5245 9044
3267 10118 11466
1347 3857 6705
9384 9576 11977

1366 8708 10758

412 4249 12863

1676 10488 11850

17 1605 2455

14 111 6045

11368 12919 12953

10588 11530 12937

4549 5143 12218

3088 4185 11674

23 2854 7823

6615 9291 9863

2229 3629 10855

3918 5509 12761

2740 11525 12914

8297 8611 12948

3606 11104 12920

5097 10412 12759

6502 7266 12072

5425 5490 10728

22 73 8462

32 12439 12657

8483 9540 10430

7275 7377 7420

5748 9726 12356

5672 6150 5156

28 3527 5857

520 7099 11335

405 6173 12865

5847 12843 12934

4289 7679 10386

2950 8021 12938

8844 11214 12955

2130 10760 12665

734 4790 12940

8 6991 12772

19 8205 11289

12 1440 9077

8670 8837 12951

3531 9166 12937

15 8901 8929

838 10114 11740

2648 9959 10934

323 7499 12877

5505 5659 11295

6627 12709 12933

364 1376 12888

8213 9124 12793

9568 10088 11168

299 890 11634

7368 7508 11602

28 4669 12583

15 27 12474

1426 3614 4205

30 2087 11147

6226 6259 12941.

[0065]

A parity check matrix initial value table with a code rate of 25/30 includes

1860 2354 3967 4292 4488 5243 5373 5766 8378 9111 10468
10505 10774

24 2266 2380 3282 4255 4779 8729 9140 9566 10102 10661
10711 10797

605 650 1108 1669 2251 3133 5847 6197 6902 7545 10521
10600 10773

1016 1428 1612 2335 3102 3810 4926 5953 9964 10246
10569 10734 10784

3195 6308 8029 9030 9397 9461 9833 10239 10499 10675
10736 10757 10773

2 27 3641 4566 7332 9318 9323 9916 10365 10438 10561
10581 10750

2405 2458 4820 6232 6254 6347 7139 7474 8623 8779 8798
10747 10794

3164 4736 6474 7162 7420 7517 7835 8238 8412 8489 9006
10113 10440

20 7372 5561 5649 6907 8393 8505 9181 9567 9595 10388

10483 10714

1071 2899 5135 5780 6616 7111 7773 8582 9015 9912 10139

10387 10768

292 2833 5490 6011 6136 6713 7517 9096 10128 10328

10407 10525 10736

1044 3711 4421 5140 5207 8118 8749 8884 9205 10359

10372 10746 10784

3241 5696 6440 7240 7419 8613 8878 9593 9959 9997 10401

10404 10754

3133 4647 5912 6065 6694 7208 7346 8227 9465 9739 10452

10516 10770

2254 6444 7449 8095 8120 8710 9030 9162 9643 9968 10101

10571 10678

918 1445 2217 4262 4623 5401 5749 7446 7907 9539 10125

10514 10726

6 1341 1788 3105 4355 5263 5470 7552 8249 8644 10609

10674 10733

1994 3000 3131 3173 7742 8335 8438 8741 9232 9296 9817

10023 10257

467 1674 3016 3950 4055 5399 6638 7113 7273 8658 8702

9642 10545

2007 2541 3125 7380 7550 8122 8501 8665 9882 10403

10519 10594 10696

334 537 709 1540 2023 2876 6216 8768 9328 9481 10424

10507 10779

2165 4185 4306 5019 6961 7386 8447 9082 9837 10091
10461 10559 10570
7 903 2948 6312 6654 7738 7980 8312 9104 9743 10070
10278 10406
3047 3154 4160 4378 5461 8711 8809 9040 9173 9252 9537
9995 10735
2018 2355 3828 3854 6201 6696 8313 8459 8550 8833 9586
10202 10224
1402 1908 4286 4660 6029 6115 6737 7538 9495 9517 10055
10509 10644
3442 3589 3863 5051 5322 5580 8725 9046 9170 10041
10613 10681 10689
2733 7826 10622
3597 4753 7086
1394 7297 10264
2848 7502 10304
1649 2405 10783
647 2911 9069
2572 4006 7508
1361 8887 10103
3681 4023 9090
1496 4962 6325
2016 5120 9747
3954 5260 8568
3364 8719 10035

4208 4806 9973
29 3361 3490
1835 2317 10436
7312 8177 9041
7728 8097 10761
2109 7902 9685
5424 8943 9436
4369 7643 9152
2240 10140 10528
3435 6124 10604
8962 9357 10040
26 1931 8629
5275 10456 10643
8 24 4952
3995 6456 10633
28 10300 10337
4894 9286 9429
5587 6721 9120
1859 9198 9762
6374 6453 7011
1319 4330 5442
1507 10711 10798
2115 3445 3641
6668 9139 10163
4038 3117 10295

1479 3403 8247
2522 2934 3562
1526 5073 9650
2136 9820 10636
4214 8464 9891
8019 10330 10610
8984 10209 10647
3414 7272 8599
4883 9077 9525
22 8173 3425
2341 6526 10126
29 6546 7361
5 3787 10468
4264 4818 6906
3903 7041 10412
6078 7661 10619
6922 9723 9890
5112 5416 6253
5923 9961 10447
9 10311 10598
8790 8814 10793
4768 5466 10664
10 10675 10766
6814 8705 10737
17 969 6692

1503 10696 10742

1285 4632 8976

4279 4973 7907

4650 4775 10785

28 729 10331

1914 5240 10723

3569 4921 9561

4 9442 10796

494 2328 9507

1717 8768 10750

9540 10599 10774

11 10075 10644

10246 10607 10753

5510 7088 9053

1347 3584 5523

7872 10596 10736

628 10592 10695

5632 5688 10627

2375 10009 10561

4169 4630 8871

2896 10038 10521

89 3695 9799

20 7563 9069

4534 10321 10697

8212 9868 10716

7485 9312 10327

234 536 6293

5515 7350 9251

283 3182 7167

2444 5378 6130

6183 8315 10726

43 4871 8347

2427 10219 10728

10 21 9448

1067 8312 8420

4793 9522 10105

4688 10536 10724

3825 7496 10709

682 8544 10449

2794 7110 10741

9279 10741 10767

2897 5442 8771

33 7957 10460

5 10393 10792

6225 10224 10798

23 9014 10786

7836 8339 8642

3476 5455 9788

1939 10251 10384

4608 7890 10450

926 2090 3804
1038 2497 10701
22 6220 8405
5153 5944 10367
7260 7726 9529
3039 8397 10665
7262 9644 10083
5531 6248 10795
7926 8248 8413
4649 8971 10182.

[0066]

A parity check matrix initial value table with a code rate of 26/30 includes

142 2307 2598 2650 4028 4434 5781 5881 6016 6323 6681
6698 8125
2932 4928 5248 5256 5383 6773 6828 7789 8426 8494 8534
8539 8583
899 3295 3833 5399 6820 7400 7753 7890 8109 8451 8529
8564 8602
21 3060 4720 5429 5636 5927 6966 8110 8170 8247 8355
8365 8616
20 1745 2838 3799 4380 4438 4646 5059 7343 8161 8302
8456 8631
9 6274 6725 6792 7195 7333 8021 8186 8209 8273 8442
8548 8632

494 1365 2405 3799 5188 5291 7644 7926 8139 8458 8504
8594 8625
192 574 1179 4387 4695 5089 5831 7673 7789 8298 8301
8612 8632
11 20 1406 6111 6176 6256 6708 6834 7828 8232 8457 8495
8602
6 2654 3554 4483 4966 5866 6795 8069 8249 8301 8497
8509 8623
21 1144 2355 3124 6773 6905 6887 7742 7994 8358 8374
8580 8611
335 4473 4883 5528 6096 7543 7586 7921 8197 8319 8394
8489 8636
2919 4331 4419 4735 6366 6393 6844 7193 8165 8205 8544
8586 8617
12 19 742 930 3009 4330 6213 6224 7292 7430 7792 7922
8137
710 1439 1588 2434 3516 5239 6248 6827 8230 8448 8515
8581 8619
200 1075 1868 5581 7349 7642 7698 8037 8201 8210 8320
8391 8526
3 2501 4252 5256 5292 5567 6136 6321 6430 6486 7571
8521 8636
3062 4599 5885 6529 6616 7314 7319 7567 8024 8153 8302
8372 8598
105 381 1574 4351 5452 5603 5943 7467 7788 7933 8362

8513 8587

787 1857 3386 3659 6550 7131 7965 8015 8040 8312 8484

8525 8537

15 1118 4226 5197 5575 5761 6762 7038 8260 8338 8444

8512 8568

36 5216 5368 5616 6029 6591 8038 8067 8299 8351 8565

8578 8585

1 23 4300 4530 5426 5532 5817 6967 7124 7979 8022 8270

8437

629 2133 4828 5475 5875 5890 7194 8042 8345 8385 8518

8598 8612

11 1065 3782 4237 4993 7104 7863 7904 8104 8228 8321

8383 8565

2131 2274 3168 3215 3220 5597 6347 7812 8238 8354 8527

8557 8614

5600 6591 7491 7696

1766 8281 8626

1725 2280 5120

1650 3445 7652

4312 6911 8626

15 1013 5892

2263 2546 2979

1545 5873 7406

67 126 3697

2860 6443 8542

17 911 2820
1561 4580 6052
79 5269 7134
22 2410 2424
3501 5642 8627
808 6950 8571
4099 6389 7482
4023 5090 7833
5476 5765 7917
1008 3194 7207
20 495 5411
1703 8388 8635
6 4395 4921
200 2053 8206
1089 5126 5562
10 4193 7720
1967 2151 4608
22 738 3513
3385 5066 8152
440 1118 8537
3429 6058 7716
5213 7519 8382
5564 8345 8620
43 3219 8603
4 5409 5815

5 6376 7654
4091 5724 5953
5348 6754 8613
1634 6398 6632
72 2058 8605
3497 5811 7579
3846 6743 8559
15 5933 8629
2133 5859 7068
4151 4617 8566
2960 8270 8410
2059 3617 8210
544 1441 6895
4043 7482 8592
294 2180 8524
3058 8227 8373
364 5756 8617
5383 8555 8619
1704 2480 4181
7338 7923 7990
2615 3905 7981
4298 4543 8296
8262 8319 8630
892 1893 8028
5694 7237 8595

1487 5012 5810

4335 8593 8624

3509 4531 5273

10 22 830

4161 5208 6280

275 7063 8634

4 2725 3113

2279 7403 8174

1637 3328 3930

2810 4939 5624

3 1234 7687

2799 7740 8616

22 7701 8636

4302 7857 7993

7477 7794 8592

3 6111 8591

5 8606 8628

347 3497 4033

1747 2613 8636

1827 5600 7042

580 1822 6842

232 7134 7783

4629 5000 7231

951 2806 4947

571 3474 8537

2437 2496 7945

23 5873 8162

12 1168 7686

8315 8540 8596

1766 2506 4733

929 1516 3338

21 1216 6555

782 1452 8617

8 6083 6087

667 3240 4533

4030 4661 5790

559 7122 8553

3202 4388 4909

2533 3673 8594

1931 3954 6206

6835 7900 7980

189 5722 8573

2680 4928 4998

243 2579 7735

4281 8122 8566

7656 7671 8609

1116 2291 4166

21 388 8021

6 1123 8369

311 4918 8511

0 3248 6290
13 6762 7172
4209 5632 7563
49 127 8074
581 1735 4075
0 2235 5470
2178 5820 6179
16 3575 6054
1095 4564 6458
9 1581 5953
2537 6469 8552
14 3874 4844
0 3269 3551
2114 7372 7926
1875 2388 4057
3232 4042 6663
9 401 583
13 4100 6584
2299 4190 4410
21 3670 4979.

[0067]

A parity check matrix initial value table with a code
rate of 27/30 includes

658 706 898 1149 2577 2622 2772 3266 3329 5243 6079
6271

289 784 1682 3584 3995 4821 4856 5063 5974 6168 6437
6453
658 1426 2043 2065 2986 4118 4284 5394 5444 5477 5727
6018
641 928 1225 2841 4052 4840 4992 5268 5533 6249 6461
6475
2312 2917 3713 3849 4059 4241 4610 5440 5727 6101 6397
6444
1165 1592 1891 2154 3981 4817 5181 5748 5788 6012 6266
6350
13 2758 3069 4233 4697 5100 5279 5677 5919 5969 6280
6422
818 1500 2125 2340 3774 4707 4901 5170 5744 6008 6316
6353
857 3054 3409 3496 3704 4868 5326 6211 6292 6356 6367
6381
0 7 12 1709 2166 3418 3723 4887 5770 6043 6069 6431
2481 3379 4650 4900 4913 5060 5410 5425 6056 6173 6283
6386
15 814 854 1871 2934 3387 3915 5180 5303 5442 5581 5665
146 1882 3076 4458 4848 5252 5602 5778 5821 6213 6251
6401
2 947 1413 1566 3437 3846 4615 4634 4735 5819 5943 6280
1231 2309 2920 4158 4185 4298 4711 5082 5757 5762 6204
6269

257 297 337 2783 3230 4134 4480 4749 5295 5689 5921
6202
1436 2151 2629 3217 3930 4078 5386 5799 5906 6146 6226
6366
133 530 2448 4745 5000 5020 5224 5273 6211 6266 6431
6453
13 2644 3895 3898 4485 4722 5142 5462 5951 6031 6084
6351
6 3000 3873 3995 4680 5158 5504 5692 5755 6255 6338
6359
166 465 1658 2549 2941 4244 5071 5149 5452 5874 5939
6038
2309 2937 4282 4628 5113 5454 5731 5825 6021 6171 6402
6472
3 1077 2116 2426 2830 4853 5066 5571 5850 5916 6289
6421
817 1608 2229 2925 3281 4393 5042 5058 5377 5464 5588
6448
3848 3871 4381 4776 5366 5578 5648 6143 6389 6434 6465
6473
1263 1616 3150 3497 3759 4078 5530 5665 5694 5913 6397
6420
11 813 2185 2795 3349 4652 4678 5078 5594 6011 6286
6387
3060 3161 4584 4996 5143 5542 5697 5937 6141 6155 6342

6445

1638 2333 2632 3450 3505 3911 4399 4454 5499 5860 6044

6360

650 1744 4517

5772 6071 6471

3582 3622 5776

6153 6380 6446

3977 5932 6447

2071 4597 4893

11 1428 3776

1111 3874 5048

1410 2144 4445

4681 5481 6462

4044 5037 5497

2716 2891 6411

3299 4384 6224

1843 6087 6400

4664 5009 5856

1548 4383 5055

3172 4190 6373

5899 6443 6470

2572 3647 6240

1295 2158 6466

5604 6269 6368

3 5551 6454

3325 5797 6261

666 1397 5538

3069 4274 6410

4042 5992 6437

743 3075 3447

1344 2725 6386

283 2808 6393

2 4627 4632

26 1565 4000

4012 4946 6472

1629 6158 6467

6300 6351 6376

2969 4444 4440

2317 3115 4932

2099 5263 6285

2409 5868 5997

3752 4200 6350

3125 5841 6142

1 2249 6322

16 2525 6379

3198 5269 5960

4 1705 2569

990 4948 5520

1664 3836 4521

1785 4110 6454

9 1373 6387
1969 2405 6368
623 1428 3946
3111 6380 6436
1861 5611 5934
9 2444 3081
5 5508 6317
3184 4988 5995
1060 4803 6400
5021 5826 6289
1608 4754 5648
4702 6391 6421
3899 4811 6128
927 2286 5313
4123 6181 6453
2893 4150 5261
605 4332 5094
17 5518 6358
2858 6126 6478
15 1316 6465
2 2032 2983
5249 6340 6427
5 6003 6200
4478 6315 6420
5158 6390 6447

2598 3229 5399

3747 6424 6446

1412 2453 6332

5256 5715 6455

2137 3421 4368

15 3880 5245

17 3156 5638

3227 3798 6230

2094 3129 6458

1412 5573 5932

175 1182 6304

3555 6407 6463

583 1654 6339

14 6261 6449

3553 5383 5679

2092 2744 4153

0 4466 6472

11 3840 4354

17 5457 6222

1467 6093 6220

3449 3858 6337

3782 5318 6426

417 5038 5790

3571 5638 5873

6117 6241 6476

1898 5680 6219

3235 3817 6429

2095 4194 6224

2 4092 6446

5 6330 6383

285 5075 6334

10 505 2867

1183 5956 6466

839 4716 6471

984 3234 6432

1501 4790 6465

8 1457 1707

1660 1969 6438

4349 6182 6305

1423 3848 5490

1651 2969 6345

344 4164 6298

2397 6027 6274

2233 2778 6161

13 1778 2977

9 1916 3377

0 3 6190

395 4993 6394

3512 4098 6400

3490 5281 6473

12 1359 6465
4202 5179 6412
3007 3542 4271
2400 3350 6351
7 5490 5716
4695 5231 6266
777 6292 6402
919 4851 6367
6 644 3893
5386 6190 6434
17 169 4896.

[0068]

A parity check matrix initial value table with a code rate of 20/30 includes

85 314 1602 1728 1929 2295 2729 2924 3779 4054 4276
918 1378 1838 1903 2399 2524 2937 3615 3740 4140 4213
1361 1430 2639 2648 2910 3418 3511 3543 4177 4209 4248
472 1143 1318 1545 1830 2228 2249 2256 3626 3839 3991
226 1401 2154 2318 2851 3317 3468 3944 3983 4047 4093
490 1143 1247 1851 2671 2776 3152 3229 3345 2738 3786
522 1393 1473 2196 2707 3052 3398 5814 3827 4148 4301
417 1982 2176 2336 2459 2806 3005 3771 3870 4080 4243
112 1040 1596 1621 1685 2118 2571 3359 3945 4034 4171
646 1705 2181 2439 2808 2851 2987 3044 3494 4049 4312
6 11 115 245 663 1773 2624 3444 3601 3352 4246

11 541 1020 1326 2259 2347 2750 2861 3328 3428 4126
515 941 1233 1804 2295 2528 3265 3826 4002 4022 4224
46 484 679 1949 2342 2929 3555 3860 3918 4068 4113
1832 2023 2279 2376 2965 3278 3318 3549 3640 3843 3910
241 943 1222 1583 1637 2745 3338 4080 4086 4203 4300
11 1419 1841 2398 2920 3409 3703 3768 3878 4052 4254
878 2049 2123 2431 2657 2704 3135 3342 3728 4141 4162
16 837 1267 1410 2100 3026 3099 3107 4042 4129 4157
133 646 1367 1394 2118 2311 2676 2956 3195 3536 3657
698 1444 2129 2432 2494 2793 2947 3852 3985 4254 4319
11 1076 1618 1995 2332 2743 2934 3009 3565 4169 4188
14 20 808 2629 2681 3099 3491 3835 4017 4068 4083
433 1386 2416 2570 2959 3611 3869 3969 4248 4251 4316
384 1292 1534 2610 2617 3559 3638 3964 4131 4293 4313
271 564 1719 2288 2597 2674 3429 3455 3793 4074 4286
133 190 815 955 1485 2000 2860 3000 3734 4013 4287
559 771 1762 2537 2764 2816 3186 3806 3933 4224 4271
11 733 1198 1735 1856 2668 2754 3216 4070 4113 4311
4 806 1832 2047 2058 2724 3387 3792 3933 4005 4319
506 1456 2339 3069 3347 3442 3889 3933 4013 4212 4278
2028 3989 4313
64 2373 4089
800 1535 4166
1030 3759 4002
1667 3269 4225

1219 2632 3878

719 2516 4277

1261 1930 3459

777 1568 1914

4 397 3290

10 3451 4115

3629 3885 4155

2652 3668 4026

135 3172 4319

1426 1970 3657

199 1268 2064

570 845 2761

41 1067 3498

1588 2482 2750

1615 2013 2715

121 1812 2588

10 992 1682

1929 4225 4279

6 1967 3760

593 1812 4107

891 2146 4158

924 2282 3585

592 2971 4235

260 3493 4313

2423 3186 3449

2042 3118 3625

2877 3064 3882

7 2139 4316

4 7 2954

1398 3947 4272

3675 4253 4318

1561 1977 2432

2531 4192 4209

1032 1102 4268

75 1718 3438

925 1073 4171

2124 2762 4148

4 3455 4069

3 1279 3382

1277 1746 3969

2727 3127 4230

584 1108 3454

9 2057 3061

1608 4103 4310

2673 3164 3713

1379 4072 4318

950 3447 4146

2509 4235 4296

813 1352 3371

3562 3865 4041

940 1217 3607
114 2544 4310
4 2178 4213
2035 4246 4251
272 1236 2733
953 2762 4115
1853 3496 4309
1119 3740 4318
2051 4058 4317
6 3162 4207
2389 4034 4111
4 3395 4301
3716 4089 4198
6 4272 4311
1 4 1854
4238 4299 4305
7 10 3737
11 3764 4296
237 1912 4117
1087 1796 4056
2153 3882 4330
962 4043 4263
243 3841 4303
2133 3886 4216
943 1974 2837

278 3224 3933
3 4196 4245
3409 4301 4315
2 2176 3214
462 3203 4008
478 2178 4202
3593 3825 4216
115 2796 4225
3827 4196 4251
1375 4301 4306
296 407 2055
688 3913 4231
3446 3840 4314
1073 3444 4146
1556 2761 3391
2 3543 4264
1378 3347 4305
847 1952 2745
1 1743 4042
2087 3048 4254
1919 4073 4132
2610 4129 4152
4106 4120 4313
7 4282 4304
3885 4227 4319

1235 4105 4135

1700 2332 4224

9 3750 4282

1539 4013 4310

3734 3834 4011

1397 2758 3645

7 1000 2984

11 3433 4068

1139 1800 3352

8 546 2561

1 4209 4239

2366 4063 4282

279 2524 2533

657 1913 4006

2322 2623 2960

758 803 2304

9 13 4241

3887 4299 4318

2612 3830 4230

1300 1596 2155

3622 3671 4239

2491 3722 3977

735 3812 4201

3204 3796 4317

2727 4292 4305

1962 2676 4255
2777 3131 4286
2518 3352 3937
4225 4255 4317
3644 3822 4311
1853 3754 4094
599 2608 3275.

[0069]

A parity check matrix initial value table with a code rate of 29/30 includes

212 499 911 940 1392
316 563 1527 2006 2077
2 1906 2043 2112 2123
537 901 1582 1812 1955
5 978 1280 1932 2145
5 2035 2044 2108 2121
5 939 1874 1974
4 1069 1758
694 2096 2106
1129 1511 1659
1564 2089 2159
2 1605 2094
474 1341 2003
103 2128 2150
1656 1993 2153

1881 2122 2138

1088 1968 2141

1 298 2073

1042 1724 2137

1253 1758 2145

1209 1966 2123

1466 2116 2155

43 2006 2049

592 1806 1865

3 143 2149

1158 1448 2002

1422 2152 2157

435 2119 2150

371 1831 2086

204 2042 2151

174 544 974

1469 1795 1995

13 708 1683

5 1144 2030

436 1309 1576

165 2030 2147

504 2073 2126

263 565 1798

229 861 1861

862 1619 1716

1346 1971 2128

5 804 1399

2139 2144 2155

4 2136 2159

1485 2059 2158

50 1091 1332

373 1730 2092

59 1086 1401

1166 1781 2065

213 2080 2154

492 1995 2110

1 1517 2126

722 1427 2146

885 991 1842

3 278 1806

967 1354 1907

1697 2047 2156

684 1924 2151

2077 2122 2157

978 2054 2135

435 2034 2150

136 1997 2125

1504 1950 2153

1404 1989 2119

199 1601 2152

780 1473 2150
198 1723 2062
927 2087 2138
1 666 2018
1293 1960 2141
1648 2033 2144
681 1578 1999
1342 2022 2157
949 1907 1994
138 1251 2135
3 608 982
1211 1501 2150
201 228 1186
1295 2089 2132
267 556 2142
801 2052 2122
1382 2135 2155
572 1503 1704
346 1183 2129
1926 2090 2149
1337 2133 2140
5 1306 2125
1383 1628 2063
1193 1626 2138
1999 2115 2146

217 274 2021

3 816 2024

1380 2138 2157

607 1385 2110

184 1195 2063

0 1767 2108

0 2081 2097

1135 2036 2128

1748 2001 2125

797 1552 1926

1046 1890 2128

291 1859 2131

1075 1214 1762

60 549 1943

581 1197 1232

1009 2026 2136

884 2002 2117

1 576 1449

519 1968 2114

5 1489 1630

1926 2037 2158

2 1249 2159

0 811 2114

2053 2152 2159

802 1911 2120

204 1033 2033
1840 2012 2037
1746 2111 2155
1098 1835 2157
2 1492 1831
353 1537 1830
375 1264 2036
2 1638 2035
1096 1971 2021
950 1809 1884
253 467 1600
5 379 1833
4 1698 1970
27 1637 2136
1174 1460 2157
612 1827 2134
1783 1802 1949
2029 2118 2151
1984 2036 2141
2 347 462
862 1693 2121
2 895 1401
4 1901 2100
1183 1674 2069
1575 1940 2158

5 1904 2097
1044 2029 2092
1441 1943 2150
0 3 1300
2 516 1735
503 1342 2019
1421 1914 2131
28 986 1467
1270 1851 1988
481 1265 2016
530 546 909
653 1309 2158
1805 2002 2149
2 1359 1518
1640 2104 2129
1656 2109 2155
1307 1762 2114
565 1647 2118
1690 2021 2156
1 300 1995
5 1681 2151
1602 2050 2156
1 1960 2153
2061 2070 2138
1581 1673 2142

1048 1142 2101

1867 1991 2055

856 1640 1878

251 561 966

343 1816 2114

3 966 2045

1885 1922 2158

57 556 2059

732 1724 2147.

[0070]

Note that each data processing apparatus may be an independent apparatus, or may be an internal block in a single apparatus.

Advantageous Effects of Invention

[0071]

According to embodiments of the present invention, it is possible to provide LDPC codes having good error-rate performance.

Brief Description of Drawings

[0072]

[Fig. 1] Fig. 1 is a diagram depicting a parity check matrix H of an LDPC code.

[Fig. 2] Fig. 2 is a flowchart depicting an LDPC code decoding procedure.

[Fig. 3] Fig. 3 is a diagram illustrating an example of a parity check matrix of an LDPC code.

[Fig. 4] Fig. 4 is a diagram illustrating a Tanner graph of a parity check matrix.

[Fig. 5] Fig. 5 is a diagram illustrating a variable node.

[Fig. 6] Fig. 6 is a diagram illustrating a check node.

[Fig. 7] Fig. 7 is a diagram illustrating an example configuration of an embodiment of a transmission system to which the present technology applies.

[Fig. 8] Fig. 8 is a block diagram illustrating an example configuration of a transmitting device 11.

[Fig. 9] Fig. 9 is a block diagram illustrating an example configuration of a bit interleaver 116.

[Fig. 10] Fig. 10 is a diagram illustrating a parity check matrix.

[Fig. 11] Fig. 11 is a diagram illustrating a parity matrix.

[Fig. 12] Fig. 12 is a diagram depicting a parity check matrix of an LDPC code defined in the DVB-S.2 standard.

[Fig. 13] Fig. 13 is a diagram depicting a parity check matrix of an LDPC code defined in the DVB-S.2 standard.

[Fig. 14] Fig. 14 includes diagrams illustrating an arrangement of constellation points of 16QAM.

[Fig. 15] Fig. 15 is a diagram illustrating arrangements of constellation points of 64QAM.

[Fig. 16] Fig. 16 is a diagram illustrating

arrangements of constellation points of 64QAM.

[Fig. 17] Fig. 17 is a diagram illustrating arrangements of constellation points of 64QAM.

[Fig. 18] Fig. 18 is a diagram illustrating an arrangement of constellation points defined in the DVB-S.2 standard.

[Fig. 19] Fig. 19 is a diagram illustrating an arrangement of constellation points defined in the DVB-S.2 standard.

[Fig. 20] Fig. 20 includes diagrams illustrating an arrangement of constellation points defined in the DVB-S.2 standard.

[Fig. 21] Fig. 21 includes diagrams illustrating an arrangement of constellation points defined in the DVB-S.2 standard.

[Fig. 22] Fig. 22 includes diagrams depicting the processing of a demultiplexer 25.

[Fig. 23] Fig. 23 includes diagrams depicting the processing of the demultiplexer 25.

[Fig. 24] Fig. 24 is a diagram illustrating a Tanner graph for LDPC code decoding.

[Fig. 25] Fig. 25 includes diagrams illustrating a parity matrix H_7 having a stepwise structure, and a Tanner graph corresponding to the parity matrix H_7 .

[Fig. 26] Fig. 26 is a diagram illustrating a parity

matrix H_p of a parity check matrix H corresponding to an LDPC code that has been subjected to parity interleaving.

[Fig. 27] Fig. 27 includes diagrams illustrating a transformed parity check matrix.

[Fig. 28] Fig. 28 is a diagram depicting the processing of a column twist interleaver 24.

[Fig. 29] Fig. 29 is a diagram illustrating the numbers of columns of a memory 31 which are necessary for column twist interleaving, and the addresses of write start positions.

[Fig. 30] Fig. 30 is a diagram illustrating the numbers of columns of the memory 31 which are necessary for column twist interleaving, and the addresses of write start positions.

[Fig. 31] Fig. 31 is a flowchart depicting a process performed by the bit interleaver 116 and a QAM encoder 117.

[Fig. 32] Fig. 32 includes diagrams illustrating a model of a communication path used in simulations.

[Fig. 33] Fig. 33 is a diagram illustrating relationships between Doppler frequencies f_d of flutters and error rates obtained in simulations.

[Fig. 34] Fig. 34 is a diagram illustrating relationships between Doppler frequencies f_d of flutters and error rates obtained in the simulations.

[Fig. 35] Fig. 35 is a block diagram illustrating an

example configuration of an LDPC encoder 115.

[Fig. 36] Fig. 36 is a flowchart depicting a process of the LDPC encoder 115.

[Fig. 37] Fig. 37 is a diagram illustrating an example of a parity check matrix initial value table with the code rate $1/4$ and the code length 16200.

[Fig. 38] Fig. 38 is a diagram depicting a method for determining a parity check matrix H from a parity check matrix initial value table.

[Fig. 39] Fig. 39 is a diagram illustrating the BER/FER characteristics of an LDPC code having a code length of 64800 bits, which is defined in the DVB-S.2 standard.

[Fig. 40] Fig. 40 is a diagram illustrating an example of a parity check matrix initial value table with the code rate $2/30$ and the code length 64800.

[Fig. 41] Fig. 41 is a diagram illustrating an example of a parity check matrix initial value table with the code rate $3/30$ and the code length 64800.

[Fig. 42] Fig. 42 is a diagram illustrating an example of a parity check matrix initial value table with the code rate $4/30$ and the code length 64800.

[Fig. 43] Fig. 43 is a diagram illustrating an example of a parity check matrix initial value table with the code rate $5/30$ and the code length 64800.

[Fig. 44] Fig. 44 is a diagram illustrating an example

of a parity check matrix initial value table with the code rate $6/30$ and the code length 64800.

[Fig. 45] Fig. 45 is a diagram illustrating an example of a parity check matrix initial value table with the code rate $7/30$ and the code length 64800.

[Fig. 46] Fig. 46 is a diagram illustrating an example of a parity check matrix initial value table with the code rate $8/30$ and the code length 64800.

[Fig. 47] Fig. 47 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $8/30$ and the code length 64800.

[Fig. 48] Fig. 48 is a diagram illustrating an example of a parity check matrix initial value table with the code rate $9/30$ and the code length 64800.

[Fig. 49] Fig. 49 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $9/30$ and the code length 64800.

[Fig. 50] Fig. 50 is a diagram illustrating an example of a parity check matrix initial value table with the code rate $10/30$ and the code length 64800.

[Fig. 51] Fig. 51 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $10/30$ and the code length 64800.

[Fig. 52] Fig. 52 is a diagram illustrating an example of a parity check matrix initial value table with the code

rate 11/30 and the code length 64800.

[Fig. 53] Fig. 53 is a diagram illustrating the example of the parity check matrix initial value table with the code rate 11/30 and the code length 64800.

[Fig. 54] Fig. 54 is a diagram illustrating an example of a parity check matrix initial value table with the code rate 12/30 and the code length 64800.

[Fig. 55] Fig. 55 is a diagram illustrating the example of the parity check matrix initial value table with the code rate 12/30 and the code length 64800.

[Fig. 56] Fig. 56 is a diagram illustrating an example of a parity check matrix initial value table with the code rate 13/30 and the code length 64800.

[Fig. 57] Fig. 57 is a diagram illustrating the example of the parity check matrix initial value table with the code rate 13/30 and the code length 64800.

[Fig. 58] Fig. 58 is a diagram illustrating an example of a parity check matrix initial value table with the code rate 14/30 and the code length 64800.

[Fig. 59] Fig. 59 is a diagram illustrating the example of the parity check matrix initial value table with the code rate 14/30 and the code length 64800.

[Fig. 60] Fig. 60 is a diagram illustrating an example of a parity check matrix initial value table with the code rate 15/30 and the code length 64800.

[Fig. 61] Fig. 61 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $15/30$ and the code length 64800.

[Fig. 62] Fig. 62 is a diagram illustrating an example of a parity check matrix initial value table with the code rate $16/30$ and the code length 64800.

[Fig. 63] Fig. 63 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $16/30$ and the code length 64800.

[Fig. 64] Fig. 64 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $16/30$ and the code length 64800.

[Fig. 65] Fig. 65 is a diagram illustrating an example of a parity check matrix initial value table with the code rate $17/30$ and the code length 64800.

[Fig. 66] Fig. 66 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $17/30$ and the code length 64800.

[Fig. 67] Fig. 67 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $17/30$ and the code length 64800.

[Fig. 68] Fig. 68 is a diagram illustrating an example of a parity check matrix initial value table with the code rate $18/30$ and the code length 64800.

[Fig. 69] Fig. 69 is a diagram illustrating the example

of the parity check matrix initial value table with the code rate 18/30 and the code length 64800.

[Fig. 70] Fig. 70 is a diagram illustrating the example of the parity check matrix initial value table with the code rate 18/30 and the code length 64800.

[Fig. 71] Fig. 71 is a diagram illustrating an example of a parity check matrix initial value table with the code rate 19/30 and the code length 64800.

[Fig. 72] Fig. 72 is a diagram illustrating the example of the parity check matrix initial value table with the code rate 19/30 and the code length 64800.

[Fig. 73] Fig. 73 is a diagram illustrating the example of the parity check matrix initial value table with the code rate 19/30 and the code length 64800.

[Fig. 74] Fig. 74 is a diagram illustrating an example of a parity check matrix initial value table with the code rate 20/30 and the code length 64800.

[Fig. 75] Fig. 75 is a diagram illustrating the example of the parity check matrix initial value table with the code rate 20/30 and the code length 64800.

[Fig. 76] Fig. 76 is a diagram illustrating the example of the parity check matrix initial value table with the code rate 20/30 and the code length 64800.

[Fig. 77] Fig. 77 is a diagram illustrating an example of a parity check matrix initial value table with the code

rate $21/30$ and the code length 64800.

[Fig. 78] Fig. 78 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $21/30$ and the code length 64800.

[Fig. 79] Fig. 79 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $21/30$ and the code length 64800.

[Fig. 80] Fig. 80 is a diagram illustrating an example of a parity check matrix initial value table with the code rate $22/30$ and the code length 64800.

[Fig. 81] Fig. 81 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $22/30$ and the code length 64800.

[Fig. 82] Fig. 82 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $22/30$ and the code length 64800.

[Fig. 83] Fig. 83 is a diagram illustrating an example of a parity check matrix initial value table with the code rate $23/30$ and the code length 64800.

[Fig. 84] Fig. 84 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $23/30$ and the code length 64800.

[Fig. 85] Fig. 85 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $23/30$ and the code length 64800.

[Fig. 86] Fig. 86 is a diagram illustrating an example of a parity check matrix initial value table with the code rate $24/30$ and the code length 64800.

[Fig. 87] Fig. 87 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $24/30$ and the code length 64800.

[Fig. 88] Fig. 88 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $24/30$ and the code length 64800.

[Fig. 89] Fig. 89 is a diagram illustrating an example of a parity check matrix initial value table with the code rate $25/30$ and the code length 64800.

[Fig. 90] Fig. 90 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $25/30$ and the code length 64800.

[Fig. 91] Fig. 91 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $25/30$ and the code length 64800.

[Fig. 92] Fig. 92 is a diagram illustrating an example of a parity check matrix initial value table with the code rate $26/30$ and the code length 64800.

[Fig. 93] Fig. 93 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $26/30$ and the code length 64800.

[Fig. 94] Fig. 94 is a diagram illustrating the example

of the parity check matrix initial value table with the code rate $26/30$ and the code length 64800.

[Fig. 95] Fig. 95 is a diagram illustrating an example of a parity check matrix initial value table with the code rate $27/30$ and the code length 64800.

[Fig. 96] Fig. 96 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $27/30$ and the code length 64800.

[Fig. 97] Fig. 97 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $27/30$ and the code length 64800.

[Fig. 98] Fig. 98 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $27/30$ and the code length 64800.

[Fig. 99] Fig. 99 is a diagram illustrating an example of a parity check matrix initial value table with the code rate $28/30$ and the code length 64800.

[Fig. 100] Fig. 100 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $28/30$ and the code length 64800.

[Fig. 101] Fig. 101 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $28/30$ and the code length 64800.

[Fig. 102] Fig. 102 is a diagram illustrating the example of the parity check matrix initial value table with

the code rate $28/30$ and the code length 64800.

[Fig. 103] Fig. 103 is a diagram illustrating an example of a parity check matrix initial value table with the code rate $29/30$ and the code length 64800.

[Fig. 104] Fig. 104 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $29/30$ and the code length 64800.

[Fig. 105] Fig. 105 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $29/30$ and the code length 64800.

[Fig. 106] Fig. 106 is a diagram illustrating the example of the parity check matrix initial value table with the code rate $29/30$ and the code length 64800.

[Fig. 107] Fig. 107 is a diagram illustrating an example of a Tanner graph of an ensemble defined by a degree sequence indicating a column weight of 3 and a row weight of 6.

[Fig. 108] Fig. 108 is a diagram illustrating an example of a Tanner graph of a multi-edge type ensemble.

[Fig. 109] Fig. 109 is a diagram illustrating minimum cycle lengths and performance thresholds for parity check matrices of LDPC codes with the code length 64800.

[Fig. 110] Fig. 110 is a diagram depicting a parity check matrix of an LDPC code with the code length 64800.

[Fig. 111] Fig. 111 is a diagram depicting parity check

matrices of LDPC codes with the code length 64800.

[Fig. 112] Fig. 112 is a diagram illustrating simulated BERs/FERs of LDPC codes with the code length 64800.

[Fig. 113] Fig. 113 is a diagram illustrating simulated BERs/FERs of LDPC codes with the code length 64800.

[Fig. 114] Fig. 114 is a diagram illustrating simulated BERs/FERs of LDPC codes with the code length 64800.

[Fig. 115] Fig. 115 includes diagrams illustrating BCH codes used in simulations of BERs/FERs of LDPC codes with the code length 64800.

[Fig. 116] Fig. 116 is a block diagram illustrating an example configuration of a receiving device 12.

[Fig. 117] Fig. 117 is a block diagram illustrating an example configuration of a bit deinterleaver 165.

[Fig. 118] Fig. 118 is a flowchart depicting a process performed by a QAM decoder 164, the bit deinterleaver 165, and an LDPC decoder 166.

[Fig. 119] Fig. 119 is a diagram illustrating an example of a parity check matrix of an LDPC code.

[Fig. 120] Fig. 120 is a diagram illustrating a matrix (transformed parity check matrix) obtained by performing row permutation and column permutation on a parity check matrix.

[Fig. 121] Fig. 121 is a diagram illustrating a transformed parity check matrix that is divided into 5×5 units.

[Fig. 122] Fig. 122 is a block diagram illustrating an example configuration of a decoding device that collectively performs node computation for P nodes.

[Fig. 123] Fig. 123 is a block diagram illustrating an example configuration of the LDPC decoder 166.

[Fig. 124] Fig. 124 includes diagrams depicting a process of a multiplexer 54 included in the bit deinterleaver 165.

[Fig. 125] Fig. 125 is a diagram depicting the processing of a column twist deinterleaver 55.

[Fig. 126] Fig. 126 is a block diagram illustrating another example configuration of the bit deinterleaver 165.

[Fig. 127] Fig. 127 is a block diagram illustrating a first example configuration of a receiving system in which the receiving device 12 can be used.

[Fig. 128] Fig. 128 is a block diagram illustrating a second example configuration of the receiving system in which the receiving device 12 can be used.

[Fig. 129] Fig. 129 is a block diagram illustrating a third example configuration of the receiving system in which the receiving device 12 can be used.

[Fig. 130] Fig. 130 is a block diagram illustrating an example configuration of an embodiment of a computer to which the present technology applies.

Description of Embodiments

[0073]

[Example Configuration of Transmission System to which Present Technology Applies]

[0074]

Fig. 7 illustrates an example configuration of an embodiment of a transmission system (the term "system" refers to a logical set of devices or apparatuses, and the devices or apparatuses may or may not be accommodated in the same housing) to which the present technology applies.

[0075]

Referring to Fig. 7, the transmission system includes a transmitting device 11 and a receiving device 12.

[0076]

The transmitting device 11 is configured to transmit (or broadcast) data such as a television broadcast program. More specifically, the transmitting device 11 encodes the target data to be transmitted, such as image data and audio data of a program, into an LDPC code, and transmits the LDPC code via a communication path 13 such as a satellite link, a terrestrial link, or a cable (wired line).

[0077]

The receiving device 12 receives an LDPC code transmitted from the transmitting device 11 via the communication path 13, decodes the LDPC code into target data, and outputs the target data.

[0078]

Here, it is well established that an LDPC code used in the transmission system illustrated in Fig. 7 exhibits very high performance on an AWGN (Additive White Gaussian Noise) communication path.

[0079]

However, burst errors or erasures may occur in the communication path 13. For example, notably in a case where the communication path 13 is a terrestrial link, in an OFDM (Orthogonal Frequency Division Multiplexing) system, a specific symbol may drop to zero in power (or be erased) in accordance with the delay of an echo (which is a path other than the main path) in a multi-path environment where a D/U (Desired to Undesired Ratio) is 0 dB (i.e., the power of the echo as the undesired power is equal to the power of the main path as the desired power).

[0080]

Further, if the D/U is 0 dB, all OFDM symbols at a specific point in time may also drop to zero in power (or be erased) due to a Doppler (doppler) frequency in a flutter (which is a communication path to which an echo with a Doppler frequency applied and having a delay of 0 is added).

[0081]

In addition, burst errors may occur due to unstable power of the receiving device 12 or undesired wiring

conditions from a receiver (not illustrated) that receives a signal from the transmitting device 11, such as an antenna, on the receiving device 12 side to the receiving device 12.
[0082]

In the LDPC code decoding process, on the other hand, as described above with reference to Fig. 5, the variable node computation of Expression (1), which involves addition of (the reception values y_{0k} of) the code bits of the LDPC code, is performed at the respective columns of the parity check matrix H , that is, the variable nodes corresponding to the code bits of the LDPC code. Thus, an error occurring in a code bit used for variable node computation would reduce the accuracy of a determined message.

[0083]

In the LDPC code decoding process, furthermore, the check node computation of Expression (7) is performed at a check node, by using messages determined at the variable nodes connected to the check node. Thus, an increase in the number of check nodes for which errors (including erasures) simultaneously occur in (code bits of an LDPC code corresponding to) a plurality of connected variable nodes would reduce decoding performance.

[0084]

More specifically, for example, if two or more of variable nodes connected to a check node simultaneously

become erasures, the check node returns a message with the probability of the value 0 being equal to the probability of the value 1 to all the variable nodes. In this case, the check node that returns the message with equal probabilities does not contribute to single decoding processing (one set of variable node computation and check node computation), resulting in a larger number of repetitions of decoding processing. Thus, decoding performance may deteriorate, and, additionally, the power consumption of the receiving device 12 that decodes the LDPC code may increase.

[0085]

To address the inconveniences described above, the transmission system illustrated in Fig. 7 is capable of increasing the resistance to burst errors or erasures while maintaining performance in an AWGN communication path.

[0086]

[Example Configuration of Transmitting Device 11]

[0087]

Fig. 8 is a block diagram illustrating an example configuration of the transmitting device 11 illustrated in Fig. 7.

[0088]

In the transmitting device 11, one or more input streams as target data are supplied to a node adaptation/multiplexer 111.

[0089]

The mode adaptation/multiplexer 111 performs processing such as mode selection and multiplexing the supplied one or more input streams, if necessary, and supplies the resulting data to a padder 112.

[0090]

The padder 112 pads zeros (or adds null) to the data supplied from the mode adaptation/multiplexer 111, as necessary, and supplies the resulting data to a BB scrambler 113.

[0091]

The BB scrambler 113 applies BB scrambling (Base-Band Scrambling) to the data supplied from the padder 112, and supplies the resulting data to a BCH encoder 114.

[0092]

The BCH encoder 114 performs BCH encoding on the data supplied from the BB scrambler 113, and supplies the resulting data to an LDPC encoder 115 as LDPC target data to be subjected to LDPC encoding.

[0093]

The LDPC encoder 115 performs LDPC encoding on the LDPC target data supplied from the BCH encoder 114 in accordance with a parity check matrix of an LDPC code, in which a parity matrix that is a portion of parity bits of the LDPC code has a stepwise structure, to obtain an LDPC code having

information bits corresponding to the LDPC target data. The LDPC encoder 115 outputs the LDPC code.

[0094]

More specifically, the LDPC encoder 115 performs LDPC encoding to encode the LDPC target data into, for example, an LDPC code defined in a certain standard such as DVB-S.2, DVB-T.2, or DVB-C.2 (corresponding to a parity check matrix) or a predetermined LDPC code (corresponding to a parity check matrix), and outputs the resulting LDPC code.

[0095]

Here, an LDPC code defined in the DVB-S.2, DVB-T.2, or DVB-C.2 standard is an IRA (Irregular Repeat Accumulate) code, and a parity matrix in a parity check matrix of the LDPC code has a stepwise structure. The parity matrix and the stepwise structure will be described below. An example of the IRA code is described in, for example, "Irregular Repeat-Accumulate Codes," H. Jin, A. Khandekar, and R. J. McEliece, in Proceedings of 2nd International Symposium on Turbo Codes and Related Topics, pp. 1-8, Sept. 2000.

[0096]

The LDPC code output from the LDPC encoder 115 is supplied to a bit interleaver 116.

[0097]

The bit interleaver 116 performs bit interleaving, described below, on the LDPC code supplied from the LDPC

encoder 115, and supplies the LDPC code that has been subjected to bit interleaving to a QAM encoder 117.

[0098]

The QAM encoder 117 maps the LDPC code supplied from the bit interleaver 116 to constellation points each representing one symbol of orthogonal modulation in units of one or more code bits of the LDPC code (or in units of symbols), and performs orthogonal modulation (multi-level modulation).

[0099]

More specifically, the QAM encoder 117 maps the LDPC code supplied from the bit interleaver 116 to constellation points defined by the modulation scheme on which orthogonal modulation of the LDPC code is based, in an IQ plane (IQ constellation) defined by an I axis representing an I component that is in the same phase as that of the carrier and a Q axis representing a Q component orthogonal to the carrier, and performs orthogonal modulation.

[0100]

Here, examples of the modulation scheme on which the orthogonal modulation performed by the QAM encoder 117 is based include modulation schemes defined in the DVB-S.2, DVB-T.2, DVB-C.2, and similar standards, and other modulation schemes, examples of which include BPSK (Binary Phase Shift Keying), QPSK (Quadrature Phase Shift Keying),

16APSK (Amplitude Phase-Shift Keying), 32APSK, 16QAM (Quadrature Amplitude Modulation), 64QAM, 256QAM, 1024QAM, 4096QAM, and 4PAM (Pulse Amplitude Modulation). Which of the modulation schemes the QAM encoder 117 uses to perform orthogonal modulation is set in advance through, for example, operation or the like by an operator of the transmitting device 11.

[0101]

The data obtained by the processing of the QAM encoder 117 (i.e., the symbols mapped to the constellation points) is supplied to a time interleaver 118.

[0102]

The time interleaver 118 performs time interleaving (which is interleaving in the time domain) on the data (i.e., symbols) supplied from the QAM encoder 117 in units of symbols, and supplies the resulting data to a MISO/MIMO encoder 119.

[0103]

The MISO/MIMO encoder 119 performs space-time encoding on the data (i.e., symbols) supplied from the time interleaver 118, and supplies the resulting data to a frequency interleaver 120.

[0104]

The frequency interleaver 120 performs frequency interleaving (which is interleaving in the frequency domain)

on the data (i.e., symbols) supplied from the MISO/MIMO encoder 119 in units of symbols, and supplies the resulting data to a frame builder & resource allocation unit 131.

[0105]

On the other hand, control data (signalling) for transmission control, such as BB signalling (Base Band Signalling) (BB Header), is supplied to a BCH encoder 121.

[0106]

The BCH encoder 121 performs BCH encoding on the control data supplied thereto in a manner similar to that for the BCH encoder 114, and supplies the resulting data to an LDPC encoder 122.

[0107]

The LDPC encoder 122 performs LDPC encoding on the data supplied from the BCH encoder 121, as LDPC target data, in a manner similar to that for the LDPC encoder 115, and supplies the resulting LDPC code to a QAM encoder 123.

[0108]

The QAM encoder 123 maps the LDPC code supplied from the LDPC encoder 122 to constellation points each representing one symbol of orthogonal modulation, in units of one or more code bits of the LDPC code (i.e., in units of symbols) in a manner similar to that for the QAM encoder 117, and performs orthogonal modulation. The QAM encoder 123 supplies the resulting data (i.e., symbols) to a frequency

interleaver 124.

[0109]

The frequency interleaver 124 performs frequency interleaving on the data (i.e., symbols) supplied from the QAM encoder 123 in units of symbols in a manner similar to that for the frequency interleaver 120, and supplies the resulting data to the frame builder & resource allocation unit 131.

[0110]

The frame builder & resource allocation unit 131 adds pilot symbols at desired positions of the data (i.e., symbols) supplied from the frequency interleavers 120 and 124, and configures a frame including a certain number of symbols (for example, a PL (Physical Layer) frame, a T2 frame, a C2 frame, etc.) from the resulting data (i.e., symbols). The frame builder & resource allocation unit 131 supplies the frame to an OFDM generation unit 132.

[0111]

The OFDM generation unit 132 generates an OFDM signal from the frame supplied from the frame builder & resource allocation unit 131, corresponding to the frame, and transmits the OFDM signal via the communication path 13 (Fig. 7).

[0112]

Note that the transmitting device 11 may be configured

without including some of the blocks illustrated in Fig. 8, such as the time interleaver 118, the MISO/MIMO encoder 119, the frequency interleaver 120, and the frequency interleaver 124.

[0113]

Fig. 9 illustrates an example configuration of the bit interleaver 116 illustrated in Fig. 8.

[0114]

The bit interleaver 116 is a data processing device for interleaving data, and includes a parity interleaver 23, a column twist interleaver 24, and a demultiplexer (DEMUX) 25. Note that the bit interleaver 116 may be configured without including one or both of the parity interleaver 23 and the column twist interleaver 24.

[0115]

The parity interleaver 23 performs parity interleaving on the LDPC code supplied from the LDPC encoder 115 to interleave parity bits of the LDPC code to different parity bit positions, and supplies the LDPC code that has been subjected to parity interleaving to the column twist interleaver 24.

[0116]

The column twist interleaver 24 performs column twist interleaving on the LDPC code supplied from the parity interleaver 23, and supplies the LDPC code that has been

subjected to column twist interleaving to the demultiplexer 25.

[0117]

More specifically, the LDPC code is transmitted after one or more code bits of the LDPC code are mapped to a constellation point representing one symbol of orthogonal modulation using the QAM encoder 117 illustrated in Fig. 8.

[0118]

The column twist interleaver 24 performs reordering processing, for example, column twist interleaving, described below, to reorder the code bits of the LDPC code supplied from the parity interleaver 23 so that a plurality of code bits of the LDPC code corresponding to 1s in an arbitrary row of the parity check matrix used in the LDPC encoder 115 are not included in one symbol.

[0119]

The demultiplexer 25 performs permutation processing on the LDPC code supplied from the column twist interleaver 24 to permute the positions of two or more code bits of the LDPC code to be mapped to symbols, thereby obtaining an LDPC code with increased resistance to AWGN. The demultiplexer 25 then supplies the two or more code bits of the LDPC code, which are obtained through the permutation processing, to the QAM encoder 117 (Fig. 8) as a symbol.

[0120]

Next, Fig. 10 illustrates the parity check matrix H that the LDPC encoder 115 illustrated in Fig. 8 uses for LDPC encoding.

[0121]

The parity check matrix H has an LDGM (Low-Density Generation Matrix) structure, and can be expressed by the equation $H = [H_A | H_T]$ (which is a matrix whose left elements are the elements of an information matrix H_A and right elements are the elements of a parity matrix H_T), where the information matrix H_A is a portion corresponding to information bits and the parity matrix H_T is a portion corresponding to parity bits among the code bits of the LDPC code.

[0122]

Here, the number of information bits and the number of parity bits among the code bits of one LDPC code (i.e., one code word) are represented by an information length K and a parity length M , respectively. In addition, the number of code bits of one LDPC code is represented by a code length N ($= K + M$).

[0123]

The information length K and the parity length M of an LDPC code having a certain code length N are determined in accordance with the code rate. In addition, the parity check matrix H is a matrix having M rows and N columns.

Thus, the information matrix H_A is an $M \times K$ matrix, and the parity matrix H_T is an $M \times M$ matrix.

[0124]

Fig. 11 illustrates a parity matrix H_T of a parity check matrix H of an LDPC code defined in the DVB-S.2, DVB-T.2, and DVB-C.2 standards.

[0125]

As illustrated in Fig. 11, the parity matrix H_T of the parity check matrix H of the LDPC code defined in DVB-T.2 and similar standards is a matrix having a stepwise structure (i.e., a lower bidiagonal matrix) in which elements of 1 are arranged in a stepwise manner. The parity matrix H_T has a row weight of 1 for the first row and a row weight of 2 for all the remaining rows. The parity matrix H_T further has a column weight of 1 for the last column and a column weight of 2 for all the remaining columns.

[0126]

In the manner described above, an LDPC code of a parity check matrix H including a parity matrix H_T having a stepwise structure can be easily generated using the parity check matrix H .

[0127]

More specifically, an LDPC code (i.e., a code word) is represented by a row vector c , and a column vector obtained by transposing the row vector is represented by c^T . In the

row vector c , which is the LDPC code, furthermore, an information bit portion is represented by a row vector A , and a parity bit portion is represented by a row vector T .
[0128]

In this case, the row vector c can be expressed by the equation $c = [A|T]$ (which is a row vector whose left elements are the elements of a row vector A and right elements are the elements of a row vector T), where the row vector A corresponds to information bits and the row vector T corresponds to parity bits.
[0129]

It is necessary for the parity check matrix H and the row vector $c = [A|T]$, which serves as the LDPC code, to satisfy the equation $Hc^T = 0$. Thus, the values of the elements of the row vector T corresponding to parity bits in the row vector $c = [A|T]$ satisfying the equation $Hc^T = 0$ can be sequentially (or successively) determined by setting the elements in the respective rows of the column vector Hc^T in the equation $Hc^T = 0$ to zero in order, starting from the element in the first row, in a case where the parity matrix H_p in the parity check matrix $H = [H_A|H_p]$ has the stepwise structure illustrated in Fig. 11.
[0130]

Fig. 12 is a diagram depicting a parity check matrix H of an LDPC code defined in DVB-T.2 and similar standards.

[0131]

The parity check matrix H of the LDPC code defined in DVB-T.2 and similar standards has a column weight X for KX columns, starting with the first column, a column weight of 3 for the subsequent $K3$ columns, a column weight of 2 for the subsequent $(M-1)$ columns, and a column weight of 1 for the last column.

[0132]

Here, the sum of columns given by $KX+K3+M-1+1$ equals the code length N .

[0133]

Fig. 13 is a diagram illustrating the numbers of columns KX , $K3$, and M and the column weight X for the respective code rates r of LDPC codes defined in DVB-T.2 and similar standards.

[0134]

In DVB-T.2 and similar standards, LDPC codes having code lengths N of 64800 bits and 16200 bits are defined.

[0135]

In addition, 11 code rates (nominal rates), $1/4$, $1/3$, $2/5$, $1/2$, $3/5$, $2/3$, $3/4$, $4/5$, $5/6$, $8/9$, and $9/10$, are defined for an LDPC code with a code length N of 64800 bits, and 10 code rates, $1/4$, $1/3$, $2/5$, $1/2$, $3/5$, $2/3$, $3/4$, $4/5$, $5/6$, and $8/9$, are defined for an LDPC code with a code length N of 16200 bits.

[0136]

Hereinafter, the code length N of 64800 bits will also be referred to as "64k bits", and the code length N of 16200 bits will also be referred to as "16k bits".

[0137]

It is well established that a code bit of an LDPC code corresponding to a column with a higher column weight in a parity check matrix H has a lower error rate.

[0138]

In a parity check matrix H defined in DVB-T.2 and similar standards illustrated in Figs. 12 and 13, the column weight tends to increase as the ordinal number of the columns of the parity check matrix H decreases (i.e., as the column comes closer to the left end of the parity check matrix H). Accordingly, robustness to errors (or resistance to errors) tends to increase as the ordinal number of the code bits of an LDPC code corresponding to the parity check matrix H decreases (i.e., the first code bit tends to be the most robust to errors), and tends to decrease as the ordinal number of the code bits increases (i.e., the last code bit tends to be the least robust to errors).

[0139]

Next, Fig. 14 illustrates example arrangements of (constellation points corresponding to) 16 symbols in an IQ plane in a case where the QAM encoder 117 illustrated in Fig.

8 performs 16QAM operation.

[0140]

More specifically, part A of Fig. 14 illustrates symbols of DVB-T.2 16QAM.

[0141]

In 16QAM, one symbol is represented as 4 bits, and 16 ($= 2^4$) symbols are provided. Further, the 16 symbols are arranged in a square of 4 symbols in the I direction and 4 symbols in the Q direction, centered on the origin of the IQ plane.

[0142]

Assuming now that the $(i+1)$ -th bit from the most significant bit of a bit sequence represented by one symbol is represented by bit y_i , then 4 bits represented by one symbol of 16QAM can be represented by bits y_0 , y_1 , y_2 , and y_3 in order, starting from the most significant bit. In a case where the modulation scheme is 16QAM, 4 code bits of an LDPC code are (symbolized) to a symbol (symbol values) of 4 bits y_0 to y_3 .

[0143]

Part B of Fig. 14 illustrates bit boundaries of 4 bits (hereinafter also referred to as "symbol bits") y_0 to y_3 represented by a 16QAM symbol.

[0144]

Here, a bit boundary of symbol bits y_i (in Fig. 14, $i =$

0, 1, 2, 3) is a boundary between a symbol having a symbol bit y_i of 0 and a symbol having a symbol bit y_i of 1.

[0145]

As illustrated in part B of Fig. 14, for the most significant symbol bit y_0 among the 4 symbol bits y_0 to y_3 represented by the 16QAM symbol, the only one bit boundary extends along the Q axis in the IQ plane. For the second symbol bit y_1 (the second most significant bit), the only one bit boundary extends along the I axis in the IQ plane.

[0146]

In addition, two bit boundaries are provided for the third symbol bit y_2 , one between the first and second columns of the 4×4 square of symbols, counting from the left, and the other between the third and fourth columns.

[0147]

In addition, two bit boundaries are provided for the fourth symbol bit y_3 , one between the first and second rows of the 4×4 square of symbols, counting from the top, and the other between the third and fourth rows.

[0148]

Symbol bits y_i represented by symbols are less erroneous (i.e., lower error probability) as the number of symbols spaced away from a bit boundary increases, and are more erroneous (i.e., higher error probability) as the number of symbols close to a bit boundary increases.

[0149]

It is assumed now that a less erroneous bit (robust to errors) is referred to as a "strong bit" and a more erroneous bit (sensitive to errors) is referred to as a "weak bit". In the 4 symbol bits y_0 to y_3 of the 16QAM symbol, the most significant symbol bit y_0 and the second symbol bit y_1 are strong bits, and the third symbol bit y_2 and the fourth symbol bit y_3 are weak bits.

[0150]

Figs. 15 to 17 illustrate example arrangements of (constellation points corresponding to) 64 symbols in an IQ plane in a case where the QAM encoder 117 illustrated in Fig. 8 performs 64QAM operation, that is, symbols of DVB-S.2 16QAM.

[0151]

In 64QAM, one symbol represents 6 bits, and 64 ($= 2^6$) symbols are provided. Further, the 64 symbols are arranged in a square of 8 symbols in the I direction and 8 symbols in the Q direction, centered on the origin of the IQ plane.

[0152]

Symbol bits of one 64QAM symbol can be represented by bits y_0 , y_1 , y_2 , y_3 , y_4 , and y_5 in order, starting from the most significant bit. In a case where the modulation scheme is 64QAM, 6 code bits of an LDPC code are mapped to a symbol of 6-bit symbol bits y_0 to y_5 .

[0153]

Here, Fig. 15 illustrates bit boundaries of the most significant symbol bit y_0 and the second symbol bit y_1 among the symbol bits y_0 to y_5 of the 64QAM symbol, Fig. 16 illustrates bit boundaries of the third symbol bit y_2 and the fourth symbol bit y_3 , and Fig. 17 illustrates bit boundaries of the fifth symbol bit y_4 and the sixth symbol bit y_5 .

[0154]

As illustrated in Fig. 15, one bit boundary is provided for each of the most significant symbol bit y_0 and the second symbol bit y_1 . Further, as illustrated in Fig. 16, two bit boundaries are provided for each of the third symbol bit y_2 and the fourth symbol bit y_3 . As illustrated in Fig. 17, four bit boundaries are provided for each of the fifth symbol bit y_4 and the sixth symbol bit y_5 .

[0155]

Accordingly, among the symbol bits y_0 to y_5 of the 64QAM symbol, the most significant symbol bit y_0 and the second symbol bit y_1 are the strongest bits, and the third symbol bit y_2 and the fourth symbol bit y_3 are the second strongest bits. Then, the fifth symbol bit y_4 and the sixth symbol bit y_5 are weak bits.

[0156]

It can be found from Fig. 14 and, furthermore, Figs. 15

to 17 that symbol bits of an orthogonal modulation symbol have a tendency that more significant bits are stronger bits and less significant bits are weaker bits.

[0157]

Fig. 18 is a diagram illustrating an example arrangement of (constellation points corresponding to) 4 symbols in an IQ plane in a case where a satellite link is used as the communication path 13 (Fig. 7) and the QAM encoder 117 illustrated in Fig. 8 performs QPSK operation, that is, a diagram of, for example, DVB-S.2 QPSK symbols.

[0158]

In DVB-S.2 QPSK, each symbol is mapped to one of four constellation points on the circumference of a circle having a radius ρ of 1, centered on the origin of the IQ plane.

[0159]

Fig. 19 is a diagram illustrating an example arrangement of 8 symbols in an IQ plane in a case where a satellite link is used as the communication path 13 (Fig. 7) and the QAM encoder 117 illustrated in Fig. 8 performs 8PSK operation, that is, a diagram of, for example, DVB-S.2 8PSK symbols.

[0160]

In DVB-S.2 8PSK, each symbol is mapped to one of eight constellation points on the circumference of a circle having a radius ρ of 1, centered on the origin of the IQ plane.

[0161]

Fig. 20 includes diagrams illustrating an example arrangement of 16 symbols in an IQ plane in a case where a satellite link is used as the communication path 13 (Fig. 7) and the QAM encoder 117 illustrated in Fig. 8 performs 16APSK operation, that is, diagrams of, for example, DVB-S.2 16APSK symbols.

[0162]

Part A of Fig. 20 illustrates an arrangement of constellation points of DVB-S.2 16APSK.

[0163]

In DVB-S.2 16APSK, each symbol is mapped to one of 16 constellation points in total, namely, 4 constellation points on the circumference of a circle having a radius R_1 and 12 constellation points on the circumference of a circle having a radius R_2 ($> R_1$), centered on the origin of the IQ plane.

[0164]

Part B of Fig. 20 illustrates the ratio $\gamma = R_2/R_1$, which is the ratio of the radii R_2 and R_1 in the arrangement of constellation points of DVB-S.2 16APSK.

[0165]

In the arrangement of constellation points of DVB-S.2 16APSK, the ratio γ of the radii R_2 and R_1 differs depending on the code rate.

[0166]

Fig. 21 includes diagrams illustrating an example arrangement of 32 symbols in an IQ plane in a case where a satellite link is used as the communication path 13 (Fig. 7) and the QAM encoder 117 illustrated in Fig. 8 performs 32APSK operation, that is, diagrams of, for example, DVB-S.2 32APSK symbols.

[0167]

Part A of Fig. 21 illustrates an arrangement of constellation points of DVB-S.2 32APSK.

[0168]

In DVB-S.2 32APSK, each symbol is mapped to one of 32 constellation points in total, namely, 4 constellation points on the circumference of a circle having a radius R_1 , 12 constellation points on the circumference of a circle having a radius R_2 ($> R_1$), and 16 constellation points on the circumference of a circle having a radius R_3 ($> R_2$), centered on the origin of the IQ plane.

[0169]

Part B of Fig. 21 illustrates the ratio $\gamma_1 = R_2/R_1$, which is the ratio of the radii R_2 and R_1 , and the ratio $\gamma_2 = R_3/R_1$, which is the ratio of the radii R_3 and R_1 , in the arrangement of constellation points of DVB-S.2 32APSK.

[0170]

In the arrangement of constellation points of DVB-S.2

32APSK, the ratio γ_1 of the radii R_2 and R_1 and the ratio γ_2 of the radii R_3 and R_1 each differ depending on the code rate.
[0171]

The symbol bits of the symbols of the respective DVB-S.2 orthogonal modulation types (QPSK, 8PSK, 16APSK, and 32APSK) having the arrangements of constellation points illustrated in Figs. 18 to 21 also include strong bits and weak bits similarly to those illustrated in Figs. 14 to 17.
[0172]

Here, as described above with reference to Figs. 12 and 13, the LDPC code output from the LDPC encoder 115 (Fig. 8) includes code bits robust to errors and code bits sensitive to errors.
[0173]

Furthermore, as described above with reference to Figs. 14 to 21, the symbol bits of a symbol of orthogonal modulation performed by the QAM encoder 117 include strong bits and weak bits.
[0174]

Thus, assigning code bits of an LDPC code which are sensitive to errors to symbol bits of an orthogonal modulation symbol which are sensitive to errors would reduce the resistance to errors as a whole.
[0175]

Accordingly, an interleaver has been proposed that is

configured to interleave code bits of an LDPC code such that a code bit of the LDPC code which is sensitive to errors is allocated to a strong bit (symbol bit) of an orthogonal modulation symbol.

[0176]

The demultiplexer 25 illustrated in Fig. 9 is capable of performing the processing of the above-described interleaver.

[0177]

Fig. 22 includes diagrams depicting the processing of the demultiplexer 25 illustrated in Fig. 9.

[0178]

More specifically, part A of Fig. 22 illustrates an example functional configuration of the demultiplexer 25.

[0179]

The demultiplexer 25 includes a memory 31 and a permutation unit 32.

[0180]

An LDPC code is supplied to the memory 31 from the LDPC encoder 115.

[0181]

The memory 31 has a storage capacity to store mb bits in its row (horizontal) direction and $N/(mb)$ bits in its column (vertical) direction. Code bits of the LDPC code supplied to the memory 31 are written in the column

direction, and are read in the row direction. The read code bits are supplied to the permutation unit 32.

[0182]

Here, as described above, N (= information length K + parity length M) represents the code length of the LDPC code.

[0183]

In addition, m represents the number of code bits of the LDPC code which are mapped to one symbol, and b is a certain positive integer and denotes a multiple used to obtain integer multiples of m . As described above, the demultiplexer 25 maps (or symbolizes) code bits of an LDPC code to a symbol, where the multiple b represents the number of symbols obtained by the demultiplexer 25 through single symbolization.

[0184]

Part A of Fig. 22 illustrates an example configuration of the demultiplexer 25 in a case where the modulation scheme is 64QAM in which each symbol is mapped to one of 64 constellation points, or any other suitable modulation scheme. The number of code bits m of an LDPC code to be mapped to one symbol is therefore 6.

[0185]

In part A of Fig. 22, furthermore, the multiple b is 1. Therefore, the memory 31 has a storage capacity of $N/(6 \times 1)$ bits in the column direction and (6×1) bits in the row

direction.

[0186]

Here, in the following, a storage area of the memory 31, which has one bit in the row direction and extends in the column direction, is referred to as a "column" as appropriate. In part A of Fig. 22, the memory 31 includes 6 (= 6×1) columns.

[0187]

The demultiplexer 23 writes code bits of the LDPC code to the memory 31 (in the column direction) from the top to the bottom of each column of the memory 31, where the writing operation moves toward the right, starting from the leftmost column.

[0188]

Further, when the writing of code bits up to the bottom of the rightmost column is completed, code bits are read from the memory 31 in the row direction, starting from the first row of all the columns of the memory 31, in units of 6 bits (i.e., mb bits). The read code bits are supplied to the permutation unit 32.

[0189]

The permutation unit 32 performs permutation processing to permute the positions of 6 code bits supplied from the memory 31, and outputs the resulting 6 bits as 6 symbol bits y_0, y_1, y_2, y_3, y_4 , and y_5 representing one 64QAM symbol.

[0130]

More specifically, mb (here, 6) code bits are read from the memory 31 in the row direction. If the i -th bit from the most significant bit of the mb code bits read from the memory 31 is represented by bit b_i (where $i = 0, 1, \dots, mb-1$), the 6 code bits read from the memory 31 in the row direction can be represented by bits b_0, b_1, b_2, b_3, b_4 , and b_5 in order, starting from the most significant bit.

[0131]

In terms of the column weights described with reference to Figs. 12 and 13, the code bits in the bit b_0 direction are code bits robust to errors, and the code bits in the bit b_5 direction are code bits sensitive to errors.

[0132]

The permutation unit 32 is configured to perform permutation processing to permute the positions of the 6 code bit b_0 to b_5 read from the memory 31 so that the code bits sensitive to errors among the 6 code bits b_0 to b_5 read from the memory 31 may be allocated to strong bits among the symbol bits y_0 to y_5 representing one 64QAM symbol.

[0133]

Here, various methods for permuting the 6 code bits b_0 to b_5 read from the memory 31 and allocating them to the 6 symbol bits y_0 to y_5 representing one 64QAM symbol have been proposed by many companies.

[0194]

Part B of Fig. 22 illustrates a first permutation method, part C of Fig. 22 illustrates a second permutation method, and part D of Fig. 22 illustrates a third permutation method.

[0195]

In part B of Fig. 22 to part D of Fig. 22 (also in Fig. 23, described below), a line connecting bits b_i and y_j indicates that the code bit b_i is allocated to the symbol bit y_j of the symbol (i.e., the position of the code bit b_i is replaced with that of the symbol bit y_j).

[0196]

In the first permutation method illustrated in part B of Fig. 22, the use of one of three permutation types is proposed. In the second permutation method illustrated in part C of Fig. 22, the use of one of two permutation types is proposed.

[0197]

In the third permutation method illustrated in part D of Fig. 22, the sequential selection and use of six permutation types are proposed.

[0198]

Fig. 23 illustrates an example configuration of the demultiplexer 25 in a case where the modulation scheme is 64QAM in which each symbol is mapped to one of 64

constellation points, or any other suitable modulation scheme (and therefore, the number of code bits m of an LDPC code to be mapped to one symbol is 6, similarly to the case in Fig. 22) and in a case where the multiple b is 2, and also illustrates a fourth permutation method.

[0199]

In a case where the multiple b is 2, the memory 31 has a storage capacity of $N/(6 \times 2)$ bits in the column direction and (6×2) bits in the row direction, and includes 12 ($= 6 \times 2$) columns.

[0200]

Part A of Fig. 23 illustrates the order in which code bits of an LDPC code are written to the memory 31.

[0201]

As described with reference to Fig. 22, the demultiplexer 25 writes code bits of the LDPC code to the memory 31 (in the column direction) from the top to the bottom of each column of the memory 31, where the writing operation moves toward the right, starting from the leftmost column.

[0202]

Further, when the writing of code bits up to the bottom of the rightmost column is completed, code bits are read from the memory 31 in the row direction, starting from the first row of all the columns of the memory 31, in units of

12 bits (i.e., mb bits). The read code bits are supplied to the permutation unit 32.

[0203]

The permutation unit 32 performs permutation processing to permute the positions of 12 code bits supplied from the memory 31, by using the fourth permutation method, and outputs the resulting 12 bits as 12 bits representing two symbols of 64QAM (i.e., b symbols), that is, 6 symbol bits $y_0, y_1, y_2, y_3, y_4,$ and y_5 representing one 64QAM symbol and 6 symbol bits $y_6, y_7, y_8, y_9, y_{10},$ and y_{11} representing the subsequent one symbol.

[0204]

Here, part B of Fig. 23 illustrates a fourth permutation method that is a method for performing permutation processing by the permutation unit 32 illustrated in part A of Fig. 23.

[0205]

Note that, in the permutation processing, in a case where the multiple b is 2 (also in a case where the multiple b is 3 or more), mb code bits are allocated to mb symbol bits of consecutive b symbols. In the following, including Fig. 23, the (i+1)-th bit from the most significant bit of mb symbol bits of consecutive b symbols is represented by bit (or symbol bit) y_i , for convenience of illustration.

[0206]

The optimum permutation type of code bits, which increases the error-rate performance in an AWGN communication path, depends on the code rate or code length of an LDPC code, the modulation scheme, and so forth.

[0207]

[Parity Interleaving]

[0208]

Next, parity interleaving performed by the parity interleaver 23 illustrated in Fig. 9 will be described with reference to Figs. 24 to 26.

[0209]

Fig. 24 illustrates (part of) a Tanner graph of a parity check matrix of an LDPC code.

[0210]

As illustrated in Fig. 24, if errors such as erasures simultaneously occur in multiple, such as two, (code bits corresponding to) variable nodes connected to a check node, the check node returns a message with the probability of the value 0 being equal to the probability of the value 1 to all the variable nodes connected to the check node. Hence, the decoding performance deteriorates if a plurality of variable nodes connected to the same check node simultaneously become erasures or the like.

[0211]

Meanwhile, the LDPC code output from the LDPC encoder

115 illustrated in Fig. 8, which is defined in the DVB-S.2 and similar standards, is an IRA code, and a parity matrix H_T of the parity check matrix H has a stepwise structure, as illustrated in Fig. 11.

[0212]

Fig. 25 illustrates a parity matrix H_T having a stepwise structure, and a Tanner graph corresponding to the parity matrix H_T .

[0213]

More specifically, part A of Fig. 25 illustrates a parity matrix H_T having a stepwise structure, and part B of Fig. 25 illustrates a Tanner graph corresponding to the parity matrix H_T illustrated in part A of Fig. 25.

[0214]

In the parity matrix H_T having a stepwise structure, elements of 1 are adjacent in each row (except the first row). Thus, in the Tanner graph of the parity matrix H_T , two adjacent variable nodes corresponding to two adjacent elements having the value 1 in the parity matrix H_T are connected to the same check node.

[0215]

Accordingly, if errors simultaneously occur in parity bits corresponding two adjacent variable nodes as described above due to burst errors, erasures, and the like, a check node connected to the two variable nodes (i.e., variable

nodes whose messages are determined using the parity bits) corresponding to the two erroneous parity bits returns a message with the probability of the value 0 being equal to the probability of the value 1 to the variable nodes connected to the check node. The decoding performance thus deteriorates. Then, if the burst length (which is the number of consecutive erroneous parity bits) increases, the number of check nodes that return the message with equal probabilities increases, resulting in further deterioration of decoding performance.

[0216]

Accordingly, the parity interleaver 23 (Fig. 9) performs parity interleaving on the LDPC code supplied from the LDPC encoder 115 to interleave parity bits to different parity bit positions in order to prevent the deterioration of decoding performance described above.

[0217]

Fig. 26 illustrates a parity matrix H_T of a parity check matrix H corresponding to an LDPC code which has been subjected to parity interleaving by the parity interleaver 23 illustrated in Fig. 9.

[0218]

Here, the information matrix H_A of the parity check matrix H corresponding to the LDPC code defined in the DVB-3.2 and similar standards, which is output from the LDPC

encoder 115, has a cyclic structure.

[0219]

The term "cyclic structure" refers to a structure in which a certain column matches another column that is cyclically shifted. Examples of the cyclic structure include a structure in which the position of "1" in each row of every P columns corresponds to the position to which the position of the first column out of the P columns has been cyclically shifted in a column direction by a value proportional to the value q obtained by dividing the parity length M. In the following, the number of columns P in the cyclic structure will be referred to as the "number of unit columns of the cyclic structure" as appropriate.

[0220]

As described with reference to Figs. 12 and 13, examples of the LDPC codes defined in the DVB-S.2 and similar standards include two types of LDPC codes having code lengths N of 64800 bits and 16200 bits. For either of the two types of LDPC codes, the number of unit columns P of the cyclic structure is defined to be 360, which is one of the divisors, excluding 1 and M, of the parity length M.

[0221]

In addition, the parity length M has a value other than the prime number represented by the equation $M = q \times P = q \times 360$, by using a value q which differs depending on the code

rate. Therefore, similarly to the number of unit columns P of the cyclic structure, the value q is also one of the divisors, excluding 1 and M , of the parity length M , and is given by dividing the parity length M by the number of unit columns P of the cyclic structure (i.e., the parity length M is the product of the divisors P and q of the parity length M).

[0222]

As described above, the parity interleaver 23 performs parity interleaving on an N -bit LDPC code to interleave the $(K+qx+y+1)$ -th code bit among the code bits of the N -bit LDPC code to the $(K+Py+x+1)$ -th code bit position, where K denotes the information length, x is an integer greater than or equal to 0 and less than P , and y is an integer greater than or equal to 0 and less than q .

[0223]

The $(K+qx+y+1)$ -th code bit and the $(K+Py+x+1)$ -th code bit are code bits positioned after the $(K+1)$ -th code bit, and are therefore parity bits. Accordingly, the position of a parity bit of an LDPC code is shifted by parity interleaving.

[0224]

In this parity interleaving operation, (parity bits corresponding to) variable nodes connected to the check node are spaced away from each other by the number of unit

columns P of the cyclic structure, i.e., in the illustrated example, 360 bits, thereby preventing simultaneous occurrence of errors in a plurality of variable nodes connected to the same check node for a burst length less than 360 bits. The resistance to burst errors can therefore be improved.

[0225]

Note that the LDPC code, which has undergone parity interleaving such that the $(K+qx+y+1)$ -th code bit is interleaved to the $(K+Py+x+1)$ -th code bit position, is identical to an LDPC code of a parity check matrix (hereinafter also referred to as a "transformed parity check matrix") that is obtained through column permutation to replace the $(K+qx+y+1)$ -th column of the original parity check matrix H with the $(K+Py+x+1)$ -th column.

[0226]

Furthermore, as illustrated in Fig. 26, the parity matrix of the transformed parity check matrix has a pseudo-cyclic structure whose number of unit columns is P (in Fig. 26, 360).

[0227]

The term "pseudo-cyclic structure", as used herein, refers to a structure in which a portion of a matrix has a cyclic structure. A transformed parity check matrix produced by performing column permutation, corresponding to

parity interleaving, on a parity check matrix of an LDPC code defined in the DVB-S.2 and similar standards has a portion of 360 rows and 360 columns in a right corner portion thereof (which corresponds to a shift matrix described below) in which only one element of "1" is missing (i.e., an element of "0" appears). In this regard, this cyclic structure is not a complete cyclic structure, called a pseudo-cyclic structure.

[0228]

Note that the transformed parity check matrix illustrated in Fig. 26 is a matrix obtained by performing permutation of rows (row permutation), in addition to column permutation corresponding to parity interleaving, on the original parity check matrix H such that the transformed parity check matrix includes component matrices described below.

[0229]

[Column Twist Interleaving]

[0230]

Next, column twist interleaving as reordering processing performed by the column twist interleaver 24 illustrated in Fig. 9 will be described with reference to Figs. 27 to 30.

[0231]

The transmitting device 11 illustrated in Fig. 8

transmits one or more code bits of an LDPC code as one symbol. More specifically, for example, QPSK is used as a modulation scheme for the transmission of 2 code bits as one symbol, and 16APSK or 16QAM is used as a modulation scheme for the transmission of 4 code bits as one symbol.

[0232]

In a case where 2 code bits are to be transmitted as one symbol, an error such as an erasure occurring in a certain symbol may cause all the code bits of the symbol to be erroneous (or erasures).

[0233]

Accordingly, in order to reduce the probability of a plurality of (code bits corresponding to) variable nodes connected to the same check node becoming simultaneously erasures to improve decoding performance, it is necessary to prevent variable nodes corresponding to code bits of one symbol from being connected to the same check node.

[0234]

In contrast, in the parity check matrix H of the LDPC code defined in the DVB-S.2 and similar standards, which is output from the LDPC encoder 115, as described above, the information matrix H_A has a cyclic structure and the parity matrix H_P has a stepwise structure. In addition, as described with reference to Fig. 26, in a transformed parity check matrix, which is a parity check matrix of an LDPC code

that has been subjected to parity interleaving, the parity matrix also has a cyclic structure (more specifically, as described above, a pseudo-cyclic structure).

[0235]

Fig. 27 illustrates a transformed parity check matrix.

[0236]

More specifically, part A of Fig. 27 illustrates a transformed parity check matrix of a parity check matrix H of an LDPC code having a code length N of 64800 bits and a code rate (r) of $3/4$.

[0237]

In the transformed parity check matrix illustrated in part A of Fig. 27, the positions of elements having the value 1 are indicated by dots ("·").

[0238]

Part B of Fig. 27 illustrates processing that the demultiplexer 25 (Fig. 9) performs on an LDPC code of the transformed parity check matrix illustrated in part A of Fig. 27, that is, an LDPC code that has been subjected to parity interleaving.

[0239]

In part B of Fig. 27, using a modulation scheme for mapping each symbol to one of 16 constellation points, such as 16APSK or 16QAM, code bits of the LDPC code that has been subjected to parity interleaving are written to four columns

of the memory 31 in the demultiplexer 25 in a column direction.

[0240]

The code bits written to the four columns of the memory 31 in the column direction are read in a row direction in units of 4 bits, and are mapped to one symbol.

[0241]

In this case, 4 code bits B_0 , B_1 , B_2 , and B_3 , which are to be mapped to one symbol, may be code bits corresponding to 1s in an arbitrary row of the transformed parity check matrix illustrated in part A of Fig. 27. In this case, the variable nodes corresponding to the code bits B_0 , B_1 , B_2 , and B_3 are connected to the same check node.

[0242]

Accordingly, in a case where 4 code bits B_0 , B_1 , B_2 , and B_3 of one symbol are code bits corresponding to 1s in an arbitrary row of the transformed parity check matrix, an erasure occurring in the symbol would make it difficult to determine an appropriate message for the same check node to which the variable nodes respectively corresponding to the code bits B_0 , B_1 , B_2 , and B_3 are connected, resulting in deterioration of decoding performance.

[0243]

Also for code rates other than a code rate of $3/4$, a plurality of code bits corresponding to a plurality of

variable nodes connected to the same check node may be mapped to one 16APSK or 16QAM symbol.

[0244]

Accordingly, the column twist interleaver 24 performs column twist interleaving on the LDPC code that has been subjected to parity interleaving, which is supplied from the parity interleaver 23, to interleave code bits of the LDPC code so that a plurality of code bits corresponding to $1s$ in an arbitrary row of the transformed parity check matrix are not included in one symbol.

[0245]

Fig. 28 is a diagram depicting column twist interleaving.

[0246]

More specifically, Fig. 28 illustrates the memory 31 (Figs. 22 and 23) of the demultiplexer 25.

[0247]

As described with reference to Fig. 22, the memory 31 has a storage capacity to store $N/(mb)$ bits in its column (vertical) direction and mb bits in its row (horizontal) direction, and includes mb columns. Then, the column twist interleaver 24 performs column twist interleaving by controlling a write start position from which the writing operation starts when a code bit of an LDPC code is written to the memory 31 in the column direction and is read from

the memory 31 in the row direction.

[0248]

More specifically, the column twist interleaver 24 appropriately changes a write start position with which the writing of a code bit starts in each of a plurality of columns so that a plurality of code bits read in the row direction, which are to be mapped to one symbol, does not match code bits corresponding to 1s in an arbitrary row of the transformed parity check matrix (That is, the column twist interleaver 24 reorders code bits of the LDPC code so that a plurality of code bits corresponding to 1s in an arbitrary row of the parity check matrix are not included in the same symbol).

[0249]

Here, Fig. 28 illustrates an example configuration of the memory 31 in a case where the modulation scheme is 16APSK or 16QAM and the multiple b described with reference to Fig. 22 is 1. Accordingly, the number of bits m of the code bits of the LDPC code that are to be mapped to one symbol is 4, and the memory 31 includes 4 ($= mb$) columns.

[0250]

The column twist interleaver 24 (instead of the demultiplexer 23 illustrated in Fig. 22) writes code bits of the LDPC code to the memory 31 (in the column direction) from the top to the bottom of each of the 4 columns of the

memory 31, where the writing operation moves toward the right, starting from the leftmost column.

[0251]

Further, when the writing of code bits up to the rightmost column is completed, the column twist interleaver 24 reads code bits from the memory 31 in the row direction, starting from the first row of all the columns of the memory 31, in units of 4 bits (i.e., mb bits), and outputs the read code bits as an LDPC code that has been subjected to column twist interleaving to the permutation unit 32 (Figs. 22 and 23) of the demultiplexer 25.

[0252]

In this regard, in the column twist interleaver 24, if the address of the first (or top) position of each column is represented by 0 and the addresses of the respective positions in the column direction are represented by integers arranged in ascending order, the write start position for the leftmost column is set to the position at the address 0, the write start position for the second column (from the left) is set to the position at the address 2, the write start position for the third column is set to the position at the address 4, and the write start position for the fourth column is set to the position of the address 7.

[0253]

Note that, after writing code bits up to the bottom of the column for which the write start position is set to a position other than the position at the address 0, the column twist interleaver 24 returns to the first position (i.e., the position at the address 0), and writes code bits up to the position immediately before the write start position. The column twist interleaver 24 then performs writing to the subsequent (right) column.

[0254]

The column twist interleaving operation described above may prevent a plurality of code bits corresponding to a plurality of variable nodes connected to the same check node for an LDPC code defined in DVB-T.2 and similar standards from being mapped to one symbol of 16APSK or 16QAM (i.e., from being included in the same symbol). Therefore, decoding performance can be improved in a communication path with an erasure.

[0255]

Fig. 29 illustrates the number of columns of the memory 31 which is necessary for column twist interleaving, and the addresses of write start positions, in association with each modulation scheme, for an LDPC code having a code length N of 64800 and each of the 11 code rates, which is defined in the DVB-T.2 standard.

[0256]

The multiple b is 1, and the number of bits m of one symbol is 2 when, for example, QPSK is employed as a modulation scheme. In this case, as illustrated in Fig. 29, the memory 31 has 2 columns for storing 2×1 ($= mb$) bits in its row direction, and stores $64800/(2 \times 1)$ bits in its column direction.

[0257]

Further, the write start position for the first column out of the 2 columns of the memory 31 is set to the position at the address 0, and the write start position for the second column is set to the position at the address 2.

[0258]

The multiple b is 1 when, for example, one of the first to third permutation types illustrated in Fig. 22 is employed as the permutation type of the permutation processing of the demultiplexer 25 (Fig. 9).

[0259]

The multiple b is 2, and the number of bits m of one symbol is 2 when, for example, QPSK is employed as a modulation scheme. In this case, as illustrated in Fig. 29, the memory 31 has 4 columns for storing 2×2 bits in its row direction, and stores $64800/(2 \times 2)$ bits in its column direction.

[0260]

Further, the write start position for the first column

out of the 4 columns of the memory 31 is set to the position at the address 0, the write start position for the second column is set to the position at the address 2, the write start position for the third column is set to the position at the address 4, and the write start position for the fourth column is set to the position at the address 7.

[0261]

Note that the multiple b is 2 when, for example, the fourth permutation type illustrated in Fig. 23 is employed as the permutation type of the permutation processing of the demultiplexer 25 (Fig. 9).

[0262]

The multiple b is 1, and the number of bits m of one symbol is 4 when, for example, 16QAM is employed as a modulation scheme. In this case, as illustrated in Fig. 29, the memory 31 has 4 columns for storing 4×1 bits in its row direction, and stores $64800/(4 \times 1)$ bits in its column direction.

[0263]

Further, the write start position for the first column out of the 4 columns of the memory 31 is set to the position at the address 0, the write start position for the second column is set to the position at the address 2, the write start position for the third column is set to the position at the address 4, and the write start position for the

fourth column is set to the position at the address 7.

[0264]

The multiple b is 2, and the number of bits m of one symbol is 4 when, for example, 16QAM is employed as a modulation scheme. In this case, as illustrated in Fig. 29, the memory 31 has 8 columns for storing 4×2 bits in its row direction, and stores $64800/(4 \times 2)$ bits in its column direction.

[0265]

Further, the write start position for the first column out of the 8 columns of the memory 31 is set to the position at the address 0, the write start position for the second column is set to the position at the address 0, the write start position for the third column is set to the position at the address 2, the write start position for the fourth column is set to the position at the address 4, the write start position for the fifth column is set to the position at the address 4, the write start position for the sixth column is set to the position at the address 5, the write start position for the seventh column is set to the position at the address 7, and the write start position for the eighth column is set to the position at the address 7.

[0266]

The multiple b is 1, and the number of bits m of one symbol is 6 when, for example, 64QAM is employed as a

modulation scheme. In this case, as illustrated in Fig. 29, the memory 31 has 6 columns for storing 6×1 bits in its row direction, and stores $64800/(6 \times 1)$ bits in its column direction.

[0267]

Further, the write start position for the first column out of the 6 columns of the memory 31 is set to the position at the address 0, the write start position for the second column is set to the position at the address 2, the write start position for the third column is set to the position at the address 5, the write start position for the fourth column is set to the position at the address 9, the write start position for the fifth column is set to the position at the address 10, and the write start position for the sixth column is set to the position at the address 13.

[0268]

The multiple b is 2, and the number of bits m of one symbol is 6 when, for example, 64QAM is employed as a modulation scheme. In this case, as illustrated in Fig. 29, the memory 31 has 12 columns for storing 6×2 bits in its row direction, and stores $64800/(6 \times 2)$ bits in its column direction.

[0269]

Further, the write start position for the first column out of the 12 columns of the memory 31 is set to the

position at the address 0, the write start position for the second column is set to the position at the address 0, the write start position for the third column is set to the position at the address 2, the write start position for the fourth column is set to the position at the address 2, the write start position for the fifth column is set to the position at the address 3, the write start position for the sixth column is set to the position at the address 4, the write start position for the seventh column is set to the position at the address 4, the write start position for the eighth column is set to the position at the address 5, the write start position for the ninth column is set to the position at the address 5, the write start position for the tenth column is set to the position at the address 7, the write start position for the eleventh column is set to the position at the address 8, and the write start position for the twelfth column is set to the position at the address 9.

[0270]

The multiple b is 1, and the number of bits m of one symbol is 3 when, for example, 256QAM is employed as a modulation scheme. In this case, as illustrated in Fig. 29, the memory 31 has 8 columns for storing 8×1 bits in its row direction, and stores $64800/(8 \times 1)$ bits in its column direction.

[0271]

Further, the write start position for the first column out of the 8 columns of the memory 31 is set to the position at the address 0, the write start position for the second column is set to the position at the address 0, the write start position for the third column is set to the position at the address 2, the write start position for the fourth column is set to the position at the address 4, the write start position for the fifth column is set to the position at the address 4, the write start position for the sixth column is set to the position at the address 5, the write start position for the seventh column is set to the position at the address 7, and the write start position for the eighth column is set to the position at the address 7.

[0272]

The multiple b is 2, and the number of bits m of one symbol is 8 when, for example, 256QAM is employed as a modulation scheme. In this case, as illustrated in Fig. 29, the memory 31 has 16 columns for storing 8×2 bits in its row direction, and stores $64800/(8 \times 2)$ bits in its column direction.

[0273]

Further, the write start position for the first column out of the 16 columns of the memory 31 is set to the position at the address 0, the write start position for the second column is set to the position at the address 2, the

write start position for the third column is set to the position at the address 2, the write start position for the fourth column is set to the position at the address 2, the write start position for the fifth column is set to the position at the address 2, the write start position for the sixth column is set to the position at the address 3, the write start position for the seventh column is set to the position at the address 7, the write start position for the eighth column is set to the position at the address 15, the write start position for the ninth column is set to the position at the address 16, the write start position for the tenth column is set to the position at the address 20, the write start position for the eleventh column is set to the position at the address 22, the write start position for the twelfth column is set to the position at the address 22, the write start position for the thirteenth column is set to the position at the address 27, the write start position for the fourteenth column is set to the position at the address 27, the write start position for the fifteenth column is set to the position at the address 28, and the write start position for the sixteenth column is set to the position at the address 32.

[0274]

The multiple b is 1, and the number of bits m of one symbol is 10 when, for example, 1024QAM is employed as a

modulation scheme. In this case, as illustrated in Fig. 29, the memory 31 has 10 columns for storing 10×1 bits in its row direction, and stores $64800/(10 \times 1)$ bits in its column direction.

[0275]

Further, the write start position for the first column out of the 10 columns of the memory 31 is set to the position at the address 0, the write start position for the second column is set to the position at the address 3, the write start position for the third column is set to the position at the address 6, the write start position for the fourth column is set to the position at the address 9, the write start position for the fifth column is set to the position at the address 11, the write start position for the sixth column is set to the position at the address 13, the write start position for the seventh column is set to the position at the address 15, the write start position for the eighth column is set to the position at the address 17, the write start position for the ninth column is set to the position at the address 18, and the write start position for the tenth column is set to the position at the address 20.

[0276]

The multiple b is 2, and the number of bits m of one symbol is 10 when, for example, 1024QAM is employed as a modulation scheme. In this case, as illustrated in Fig. 29,

the memory 31 has 20 columns for storing 10×2 bits in its row direction, and stores $64800/(10 \times 2)$ bits in its column direction.

[0277]

Further, the write start position for the first column out of the 20 columns of the memory 31 is set to the position at the address 0, the write start position for the second column is set to the position at the address 1, the write start position for the third column is set to the position at the address 3, the write start position for the fourth column is set to the position at the address 4, the write start position for the fifth column is set to the position at the address 5, the write start position for the sixth column is set to the position at the address 6, the write start position for the seventh column is set to the position at the address 6, the write start position for the eighth column is set to the position at the address 9, the write start position for the ninth column is set to the position at the address 13, the write start position for the tenth column is set to the position at the address 14, the write start position for the eleventh column is set to the position at the address 14, the write start position for the twelfth column is set to the position at the address 16, the write start position for the thirteenth column is set to the position at the address 21, the write start position for the

fourteenth column is set to the position at the address 21, the write start position for the fifteenth column is set to the position at the address 23, the write start position for the sixteenth column is set to the position at the address 25, the write start position for the seventeenth column is set to the position at the address 25, the write start position for the eighteenth column is set to the position at the address 26, the write start position for the nineteenth column is set to the position at the address 28, and the write start position for the twentieth column is set to the position at the address 30.

[0278]

The multiple b is 1, and the number of bits m of one symbol is 12 when, for example, 4096QAM is employed as a modulation scheme. In this case, as illustrated in Fig. 29, the memory 31 has 12 columns for storing 12×1 bits in its row direction, and stores $54800/(12 \times 1)$ bits in its column direction.

[0279]

Further, the write start position for the first column out of the 12 columns of the memory 31 is set to the position at the address 0, the write start position for the second column is set to the position at the address 0, the write start position for the third column is set to the position at the address 2, the write start position for the

fourth column is set to the position at the address 2, the write start position for the fifth column is set to the position at the address 3, the write start position for the sixth column is set to the position at the address 4, the write start position for the seventh column is set to the position at the address 4, the write start position for the eighth column is set to the position at the address 5, the write start position for the ninth column is set to the position at the address 5, the write start position for the tenth column is set to the position at the address 7, the write start position for the eleventh column is set to the position at the address 8, and the write start position for the twelfth column is set to the position at the address 9.

[0280]

The multiple b is 2, and the number of bits m of one symbol is 12 when, for example, 4096QAM is employed as a modulation scheme. In this case, as illustrated in Fig. 29, the memory 31 has 24 columns for storing 12×2 bits in its row direction, and stores $64800/(12 \times 2)$ bits in its column direction.

[0281]

Further, the write start position for the first column out of the 24 columns of the memory 31 is set to the position at the address 0, the write start position for the second column is set to the position at the address 5, the

write start position for the third column is set to the position at the address 8, the write start position for the fourth column is set to the position at the address 8, the write start position for the fifth column is set to the position at the address 8, the write start position for the sixth column is set to the position at the address 8, the write start position for the seventh column is set to the position at the address 10, the write start position for the eighth column is set to the position at the address 10, the write start position for the ninth column is set to the position at the address 10, the write start position for the tenth column is set to the position at the address 12, the write start position for the eleventh column is set to the position at the address 13, the write start position for the twelfth column is set to the position at the address 16, the write start position for the thirteenth column is set to the position at the address 17, the write start position for the fourteenth column is set to the position at the address 19, the write start position for the fifteenth column is set to the position at the address 21, the write start position for the sixteenth column is set to the position at the address 22, the write start position for the seventeenth column is set to the position at the address 23, the write start position for the eighteenth column is set to the position at the address 26, the write start position for the nineteenth

column is set to the position at the address 37, the write start position for the twentieth column is set to the position at the address 39, the write start position for the twenty-first column is set to the position at the address 40, the write start position for the twenty-second column is set to the position at the address 41, the write start position for the twenty-third column is set to the position at the address 41, and the write start position for the twenty-fourth column is set to the position at the address 41.

[0282]

Fig. 30 illustrates the number of columns of the memory 31 which is necessary for column twist interleaving, and the addresses of write start positions, in association with each modulation scheme, for an LDPC code having a code length N of 16200 and each of the 10 code rates, which is defined in the DVB-T.2 standard.

[0283]

The multiple b is 1, and the number of bits m of one symbol is 2 when, for example, QPSK is employed as a modulation scheme. In this case, as illustrated in Fig. 30, the memory 31 has 2 columns for storing 2×1 bits in its row direction, and stores $16200/(2 \times 1)$ bits in its column direction.

[0284]

Further, the write start position for the first column

out of the 2 columns of the memory 31 is set to the position at the address 0, and the write start position for the second column is set to the position at the address 0.

[0285]

The multiple b is 2, and the number of bits m of one symbol is 2 when, for example, QPSK is employed as a modulation scheme. In this case, as illustrated in Fig. 30, the memory 31 has 4 columns for storing 2×2 bits in its row direction, and stores $16200/(2 \times 2)$ bits in its column direction.

[0286]

Further, the write start position for the first column out of the 4 columns of the memory 31 is set to the position at the address 0, the write start position for the second column is set to the position at the address 2, the write start position for the third column is set to the position at the address 3, and the write start position for the fourth column is set to the position at the address 3.

[0287]

The multiple b is 1, and the number of bits m of one symbol is 4 when, for example, 16QAM is employed as a modulation scheme. In this case, as illustrated in Fig. 30, the memory 31 has 4 columns for storing 4×1 bits in its row direction, and stores $16200/(4 \times 1)$ bits in its column direction.

[0288]

Further, the write start position for the first column out of the 4 columns of the memory 31 is set to the position at the address 0, the write start position for the second column is set to the position at the address 2, the write start position for the third column is set to the position at the address 3, and the write start position for the fourth column is set to the position at the address 3.

[0289]

The multiple b is 2, and the number of bits m of one symbol is 4 when, for example, 16QAM is employed as a modulation scheme. In this case, as illustrated in Fig. 30, the memory 31 has 8 columns for storing 4×2 bits in its row direction, and stores $16200/(4 \times 2)$ bits in its column direction.

[0290]

Further, the write start position for the first column out of the 8 columns of the memory 31 is set to the position at the address 0, the write start position for the second column is set to the position at the address 0, the write start position for the third column is set to the position at the address 0, the write start position for the fourth column is set to the position at the address 1, the write start position for the fifth column is set to the position at the address 1, the write start position for the sixth

column is set to the position at the address 20, the write start position for the seventh column is set to the position at the address 20, and the write start position for the eighth column is set to the position at the address 21.

[0291]

The multiple b is 1, and the number of bits m of one symbol is 6 when, for example, 64QAM is employed as a modulation scheme. In this case, as illustrated in Fig. 30, the memory 31 has 6 columns for storing 6×1 bits in its row direction, and stores $16200/(6 \times 1)$ bits in its column direction.

[0292]

Further, the write start position for the first column out of the 6 columns of the memory 31 is set to the position at the address 0, the write start position for the second column is set to the position at the address 0, the write start position for the third column is set to the position at the address 2, the write start position for the fourth column is set to the position at the address 3, the write start position for the fifth column is set to the position at the address 7, and the write start position for the sixth column is set to the position at the address 7.

[0293]

The multiple b is 2, and the number of bits m of one symbol is 6 when, for example, 64QAM is employed as a

modulation scheme. In this case, as illustrated in Fig. 30, the memory 31 has 12 columns for storing 6×2 bits in its row direction, and stores $16200/(6 \times 2)$ bits in its column direction.

[0294]

Further, the write start position for the first column out of the 12 columns of the memory 31 is set to the position at the address 0, the write start position for the second column is set to the position at the address 0, the write start position for the third column is set to the position at the address 0, the write start position for the fourth column is set to the position at the address 2, the write start position for the fifth column is set to the position at the address 2, the write start position for the sixth column is set to the position at the address 2, the write start position for the seventh column is set to the position at the address 3, the write start position for the eighth column is set to the position at the address 3, the write start position for the ninth column is set to the position at the address 3, the write start position for the tenth column is set to the position at the address 6, the write start position for the eleventh column is set to the position at the address 7, and the write start position for the twelfth column is set to the position at the address 7.

[0295]

The multiple b is 1, and the number of bits m of one symbol is 8 when, for example, 256QAM is employed as a modulation scheme. In this case, as illustrated in Fig. 30, the memory 31 has 8 columns for storing 8×1 bits in its row direction, and stores $16200/(8 \times 1)$ bits in its column direction.

[0296]

Further, the write start position for the first column out of the 8 columns of the memory 31 is set to the position at the address 0, the write start position for the second column is set to the position at the address 0, the write start position for the third column is set to the position at the address 0, the write start position for the fourth column is set to the position at the address 1, the write start position for the fifth column is set to the position at the address 7, the write start position for the sixth column is set to the position at the address 20, the write start position for the seventh column is set to the position at the address 20, and the write start position for the eighth column is set to the position at the address 21.

[0297]

The multiple b is 1, and the number of bits m of one symbol is 10 when, for example, 1024QAM is employed as a modulation scheme. In this case, as illustrated in Fig. 30, the memory 31 has 10 columns for storing 10×1 bits in its

row direction, and stores $16200/(10 \times 1)$ bits in its column direction.

[0298]

Further, the write start position for the first column out of the 10 columns of the memory 31 is set to the position at the address 0, the write start position for the second column is set to the position at the address 1, the write start position for the third column is set to the position at the address 2, the write start position for the fourth column is set to the position at the address 2, the write start position for the fifth column is set to the position at the address 3, the write start position for the sixth column is set to the position at the address 3, the write start position for the seventh column is set to the position at the address 4, the write start position for the eighth column is set to the position at the address 4, the write start position for the ninth column is set to the position at the address 5, and the write start position for the tenth column is set to the position at the address 7.

[0299]

The multiple b is 2, and the number of bits m of one symbol is 10 when, for example, 1624QAM is employed as a modulation scheme. In this case, as illustrated in Fig. 30, the memory 31 has 20 columns for storing 10×2 bits in its row direction, and stores $16200/(10 \times 2)$ bits in its column

direction.

[03001

Further, the write start position for the first column out of the 20 columns of the memory 31 is set to the position at the address 0, the write start position for the second column is set to the position at the address 0, the write start position for the third column is set to the position at the address 0, the write start position for the fourth column is set to the position at the address 2, the write start position for the fifth column is set to the position at the address 2, the write start position for the sixth column is set to the position at the address 2, the write start position for the seventh column is set to the position at the address 2, the write start position for the eighth column is set to the position at the address 2, the write start position for the ninth column is set to the position at the address 5, the write start position for the tenth column is set to the position at the address 5, the write start position for the eleventh column is set to the position at the address 5, the write start position for the twelfth column is set to the position at the address 5, the write start position for the thirteenth column is set to the position at the address 5, the write start position for the fourteenth column is set to the position at the address 7, the write start position for the fifteenth column is set to

the position at the address 7, the write start position for the sixteenth column is set to the position at the address 7, the write start position for the seventeenth column is set to the position at the address 7, the write start position for the eighteenth column is set to the position at the address 8, the write start position for the nineteenth column is set to the position at the address 8, and the write start position for the twentieth column is set to the position at the address 10.

[0301]

The multiple b is 1, and the number of bits m of one symbol is 12 when, for example, 4096QAM is employed as a modulation scheme. In this case, as illustrated in Fig. 30, the memory 31 has 12 columns for storing 12×1 bits in its row direction, and stores $16200/(12 \times 1)$ bits in its column direction.

[0302]

Further, the write start position for the first column out of the 12 columns of the memory 31 is set to the position at the address 0, the write start position for the second column is set to the position at the address 0, the write start position for the third column is set to the position at the address 0, the write start position for the fourth column is set to the position at the address 2, the write start position for the fifth column is set to the

position at the address 2, the write start position for the sixth column is set to the position at the address 2, the write start position for the seventh column is set to the position at the address 3, the write start position for the eighth column is set to the position at the address 3, the write start position for the ninth column is set to the position at the address 3, the write start position for the tenth column is set to the position at the address 6, the write start position for the eleventh column is set to the position at the address 7, and the write start position for the twelfth column is set to the position at the address 7.

[0303]

The multiple b is 2, and the number of bits m of one symbol is 12 when, for example, 4096QAM is employed as a modulation scheme. In this case, as illustrated in Fig. 30, the memory 31 has 24 columns for storing 12×2 bits in its row direction, and stores $16200/(12 \times 2)$ bits in its column direction.

[0304]

Further, the write start position for the first column out of the 24 columns of the memory 31 is set to the position at the address 0, the write start position for the second column is set to the position at the address 0, the write start position for the third column is set to the position at the address 0, the write start position for the

fourth column is set to the position at the address 0, the write start position for the fifth column is set to the position at the address 0, the write start position for the sixth column is set to the position at the address 0, the write start position for the seventh column is set to the position at the address 0, the write start position for the eighth column is set to the position at the address 1, the write start position for the ninth column is set to the position at the address 1, the write start position for the tenth column is set to the position at the address 1, the write start position for the eleventh column is set to the position at the address 2, the write start position for the twelfth column is set to the position at the address 2, the write start position for the thirteenth column is set to the position at the address 2, the write start position for the fourteenth column is set to the position at the address 3, the write start position for the fifteenth column is set to the position at the address 7, the write start position for the sixteenth column is set to the position at the address 9, the write start position for the seventeenth column is set to the position at the address 9, the write start position for the eighteenth column is set to the position at the address 9, the write start position for the nineteenth column is set to the position at the address 10, the write start position for the twentieth column is set to the

position at the address 10, the write start position for the twenty-first column is set to the position at the address 10, the write start position for the twenty-second column is set to the position at the address 10, the write start position for the twenty-third column is set to the position at the address 10, and the write start position for the twenty-fourth column is set to the position at the address 11.

[0305]

Fig. 31 is a flowchart depicting a process performed in the LDPC encoder 115, the bit interleaver 116, and the QAM encoder 117 illustrated in Fig. 2.

[0306]

The LDPC encoder 115 waits for LDPC target data to be supplied from the BCH encoder 114. In step S101, the LDPC encoder 115 encodes the LDPC target data into an LDPC code, and supplies the LDPC code to the bit interleaver 116. Then, the process proceeds to step S102.

[0307]

In step S102, the bit interleaver 116 performs bit interleaving on the LDPC code supplied from the LDPC encoder 115, and supplies a symbol obtained by symbolizing the LDPC code that has been subjected to bit interleaving, to the QAM encoder 117. Then, the process proceeds to step S103.

[0308]

More specifically, in step S102, in the bit interleaver

116 (Fig. 3), the parity interleaver 23 performs parity interleaving on the LDPC code supplied from the LDPC encoder 115, and supplies the LDPC code that has been subjected to parity interleaving to the column twist interleaver 24.

[0309]

The column twist interleaver 24 performs column twist interleaving on the LDPC code supplied from the parity interleaver 23, and supplies the resulting LDPC code to the demultiplexer 25.

[0310]

The demultiplexer 25 performs permutation processing to permute the code bits of the LDPC code that has been subjected to column twist interleaving by the column twist interleaver 24 and to map the permuted code bits to symbol bits of a symbol (i.e., bits representing the symbol).

[0311]

Here, the permutation processing of the demultiplexer 25 may be performed in accordance with any of the first to fourth permutation types illustrated in Figs. 22 and 23, and may also be performed in accordance with a certain predetermined allocation rule to allocate code bits of an LDPC code to symbol bits representing a symbol.

[0312]

The symbols obtained by the permutation processing performed by the demultiplexer 25 are supplied from the

demultiplexer 25 to the QAM encoder 117.

[0313]

In step S103, the QAM encoder 117 maps the symbols supplied from the demultiplexer 25 to constellation points defined by the modulation scheme for the orthogonal modulation to be performed by the QAM encoder 117, and then performs orthogonal modulation. The resulting data is supplied to the time interleaver 118.

[0314]

As described above, parity interleaving and column twist interleaving may improve resistance to erasures or burst errors in a case where a plurality of code bits of an LDPC code are transmitted as one symbol.

[0315]

Here, in Fig. 9, the parity interleaver 23 serving as a block configured to perform parity interleaving and the column twist interleaver 24 serving as a block configured to perform column twist interleaving are configured as separate units, for convenience of illustration. However, the parity interleaver 23 and the column twist interleaver 24 may be integrated into a single unit.

[0316]

More specifically, both parity interleaving and column twist interleaving can be performed by writing and reading code bits to and from a memory, and can be represented by a

matrix that converts an address at which a code bit is to be written i.e., a write address) to an address at which a code bit is to be read (i.e., a read address).

[0317]

Accordingly, once a matrix obtained by multiplying a matrix representing parity interleaving and a matrix representing column twist interleaving is determined, an LDPC code that has been subjected to parity interleaving and then column twist interleaving can be obtained by converting code bits using the determined matrix.

[0318]

Furthermore, the demultiplexer 25 in addition to the parity interleaver 23 and the column twist interleaver 24 may also be integrated into a single unit.

[0319]

More specifically, the permutation processing performed in the demultiplexer 25 can also be represented by a matrix that converts a write address in the memory 31 at which an LDPC code is stored to a read address.

[0320]

Accordingly, once a matrix obtained by multiplying a matrix representing parity interleaving, a matrix representing column twist interleaving, and a matrix representing permutation processing is determined, parity interleaving, column twist interleaving, and permutation

processing can be performed in a batch way using the determined matrix.

[0321]

Note that either parity interleaving or column twist interleaving may be performed, or neither of them may be performed. For example, as in the DVB-S.2 system, if the communication path 13 (Fig. 7) is a non-AWGN channel that does not much take into account burst errors, flutters, and so forth, such as a satellite link, none of parity interleaving and column twist interleaving may be performed.

[0322]

Next, simulations for measuring error rates (bit error rates) that were performed on the transmitting device 11 illustrated in Fig. 8 will be described with reference to Figs. 32 to 34.

[0323]

The simulations were performed using a communication path with a flutter having a D/U of 0 dB.

[0324]

Fig. 32 illustrates a model of a communication path employed in the simulations.

[0325]

More specifically, part A of Fig. 32 illustrates a model of a flutter employed in the simulations.

[0326]

Further, part B of Fig. 32 illustrates a model of a communication path having the flutter represented by the model illustrated in part A of Fig. 32.

[0327]

Note that, in part B of Fig. 32, H represents the model of the flutter illustrated in part A of Fig. 32. In part B of Fig. 32, furthermore, N represents the ICI (Inter Carrier Interference). In the simulations, an expected value $E[N^2]$ of the power of the ICI was approximated by AWGN.

[0328]

Figs. 33 and 34 illustrate relationships between Doppler frequencies f_a of flutters and error rates obtained in the simulations.

[0329]

Note that Fig. 33 illustrates relationships between error rates and Doppler frequencies f_d in a case where the modulation scheme is 16QAM, the code rate (r) is 3/4, and the permutation type is the first permutation type. Fig. 34 illustrates relationships between error rates and Doppler frequencies f_a in a case where the modulation scheme is 64QAM, the code rate (r) is 5/6, and the permutation type is the first permutation type.

[0330]

In Figs. 33 and 34, furthermore, bold lines indicate relationships between error rates and Doppler frequencies f_a .

in a case where parity interleaving, column twist interleaving, and permutation processing were all carried out, and thin lines indicate relationships between error rates and Doppler frequencies f_d in a case where only permutation processing out of parity interleaving, column twist interleaving, and permutation processing was carried out.

[0331]

It can be seen from any of Figs. 33 and 34 that the error-rate performance is improved (i.e., error rates are reduced) in the case where parity interleaving, column twist interleaving, and permutation processing were all carried out, compared to the case where only permutation processing was carried out.

[0332]

[Example Configuration of LDPC Encoder 115]

[0333]

Fig. 35 is a block diagram illustrating an example configuration of the LDPC encoder 115 illustrated in Fig. 8.

[0334]

Note that the LDPC encoder 122 illustrated in Fig. 8 also has a similar configuration.

[0335]

As described with reference to Figs. 12 and 13, LDPC codes having two types of code lengths N of 64800 bits and

16200 bits are defined in the DVB-S.2 and similar standards.

[0336]

In addition, 11 code rates, $1/4$, $1/3$, $2/5$, $1/2$, $3/5$, $2/3$, $3/4$, $4/5$, $5/6$, $8/9$, and $9/10$, are defined for LDPC codes having a code length N of 64800 bits, and 10 code rates, $1/4$, $1/3$, $2/5$, $1/2$, $3/5$, $2/3$, $3/4$, $4/5$, $5/6$, and $8/9$, are defined for LDPC codes having a code length N of 16200 bits (Figs. 12 and 13).

[0337]

The LDPC encoder 115 is capable of performing encoding (i.e., error correcting encoding) using, for example, the LDPC codes having code lengths N of 64800 bits and 16200 bits and the respective code rates, in accordance with the parity check matrix H prepared for each code length N and each code rate.

[0338]

The LDPC encoder 115 includes an encoding processing unit 601 and a storage unit 602.

[0339]

The encoding processing unit 601 includes a code rate setting unit 611, an initial value table read unit 612, a parity check matrix generation unit 613, an information bit read unit 614, an encoding parity computation unit 615, and a control unit 616. The encoding processing unit 601 performs LDPC encoding on the LDPC target data supplied to

the LDPC encoder 115, and supplies the resulting LDPC code to the bit interleaver 116 (Fig. 8).

[0340]

More specifically, the code rate setting unit 611 sets a code length N and a code rate of the LDPC code in accordance with, for example, an operation of an operator or the like.

[0341]

The initial value table read unit 612 reads a parity check matrix initial value table, described below, corresponding to the code length N and code rate set by the code rate setting unit 611 from the storage unit 602.

[0342]

The parity check matrix generation unit 613 generates a parity check matrix H on the basis of the parity check matrix initial value table read by the initial value table read unit 612, by arranging elements of 1 in an information matrix H_A having an information length K (= code length N - parity length M) corresponding to the code length N and code rate set by the code rate setting unit 611, in a column direction at intervals of 360 columns (i.e., the number of unit columns P of the cyclic structure). The parity check matrix H is stored in the storage unit 602.

[0343]

The information bit read unit 614 reads (or extracts)

information bits corresponding to the information length K from the LDPC target data supplied to the LDPC encoder 115.

[0344]

The encoding parity computation unit 615 reads the parity check matrix H generated by the parity check matrix generation unit 613 from the storage unit 602, and generates a code word (i.e., an LDPC code) by calculating parity bits corresponding to the information bits read by the information bit read unit 614 in accordance with a certain formula by using the parity check matrix H .

[0345]

The control unit 616 controls the blocks included in the encoding processing unit 601.

[0346]

The storage unit 602 has stored therein a plurality of parity check matrix initial value tables and the like respectively corresponding to the plurality of code rates and the like illustrated in Figs. 12 and 13 for the respective code lengths N such as 64800 bits and 16200 bits. In addition, the storage unit 602 temporarily stores data necessary for the processing of the encoding processing unit 601.

[0347]

Fig. 36 is a flowchart depicting a process of the LDPC encoder 115 illustrated in Fig. 35.

[0348]

In step S201, the code rate setting unit 611 determines (or sets) a code length N and a code rate r for LDPC encoding.

[0349]

In step S202, the initial value table read unit 612 reads a predetermined parity check matrix initial value table corresponding to the code length N and code rate r determined by the code rate setting unit 611 from the storage unit 602.

[0350]

In step S203, the parity check matrix generation unit 613 determines (or generates) a parity check matrix H of an LDPC code having the code length N and code rate r determined by the code rate setting unit 611 by using the parity check matrix initial value table read by the initial value table read unit 612 from the storage unit 602, and supplies the parity check matrix H to the storage unit 602 for storage.

[0351]

In step S204, the information bit read unit 614 reads information bits of the information length K ($= N \times r$) corresponding to the code length N and code rate r determined by the code rate setting unit 611 from the LDPC target data supplied to the LDPC encoder 116, and also reads

the parity check matrix H determined by the parity check matrix generation unit 613 from the storage unit 602. Then, the information bit read unit 614 supplies the read information bits and parity check matrix H to the encoding parity computation unit 615.

[0352]

In step S205, the encoding parity computation unit 615 sequentially computes parity bits of a code word c satisfying Expression (8) by using the information bits and the parity check matrix H supplied from the information bit read unit 614.

[0353]

$$Hc^T = 0 \quad \dots (8)$$

[0354]

In Expression (8), c denotes a row vector as a code word (i.e., LDPC code), and c^T denotes the transpose of the row vector c .

[0355]

Here, as described above, if an information bit portion of the row vector c as the LDPC code (i.e., one code word) is represented by a row vector A and a parity bit portion is represented by a row vector T , the row vector c can be represented by the equation $c = [AT]$ using the row vector A corresponding to information bits and the row vector T corresponding to parity bits.

[0356]

It is necessary for the parity check matrix H and the row vector $c = [A|T]$ corresponding to the LDPC code to satisfy the equation $Hc^T = 0$. The values of the elements of the row vector T corresponding to parity bits in the row vector $c = [A|T]$ satisfying the equation $Hc^T = 0$ can be sequentially determined by setting the elements in the respective rows of the column vector Hc^T in the equation $Hc^T = 0$ to zero in order, starting from the element in the first row, in a case where the parity matrix H_p in the parity check matrix $H = [H_A|H_p]$ has the stepwise structure illustrated in Fig. 11.

[0357]

The encoding parity computation unit 615 determines parity bits T corresponding to the information bits A supplied from the information bit read unit 614, and outputs a code word $c = [A|T]$, which is represented by the information bits A and the parity bits T , as a result of LDPC encoding of the information bits A .

[0358]

Then, in step S206, the control unit 616 determines whether or not to terminate the LDPC encoding operation. If it is determined in step S206 that the LDPC encoding operation is not to be terminated, for example, if there is any LDPC target data to be subjected to LDPC encoding, the

process returns to step S201 (or step S204), and the processing of steps S201 (or steps S204) to S206 is subsequently repeatedly performed.

[0359]

Further, if it is determined in step S206 that the LDPC encoding operation is to be terminated, for example, if there is no LDPC target data to be subjected to LDPC encoding, the LDPC encoder 115 terminates the process.

[0360]

As described above, parity check matrix initial value tables corresponding to the respective code lengths N and the respective code rates r are prepared, and the LDPC encoder 115 performs LDPC encoding with a certain code length N and a certain code rate r by using a parity check matrix H generated from the parity check matrix initial value table corresponding to the certain code length N and the certain code rate r .

[0361]

[Example of Parity Check Matrix Initial Value Table]

[0362]

A parity check matrix initial value table is a table showing the positions of elements of z in an information matrix E_A (Fig. 10) having an information length K corresponding to a code length N and code rate r of an LDPC code (i.e., an LDPC code defined by the parity check matrix

H) in the parity check matrix H , in units of 360 columns (i.e., the number of unit columns P of the cyclic structure). A parity check matrix initial value table is created in advance for each of parity check matrices H having the respective code lengths N and the respective code rates r .
[0363]

Fig. 37 is a diagram illustrating an example of a parity check matrix initial value table.
[0364]

More specifically, Fig. 37 illustrates a parity check matrix initial value table for a parity check matrix H having a code length N of 16200 bits and a code rate (nominal code rate defined in DVB-T.2) r of $1/4$, which is defined in the DVB-T.2 standard.
[0365]

The parity check matrix generation unit 613 (Fig. 35) determines a parity check matrix H in the following way using the parity check matrix initial value table.
[0366]

More specifically, Fig. 38 illustrates a method for determining a parity check matrix H from a parity check matrix initial value table.
[0367]

Note that the parity check matrix initial value table illustrated in Fig. 38 is a parity check matrix initial

value table for a parity check matrix H having a code length N of 16200 bits and a code rate r of $2/3$, which is defined in the DVB-T.2 standard.

[0368]

As described above, a parity check matrix initial value table is a table showing the positions of elements of 1 in an information matrix H_A (Fig. 10) having an information length K corresponding to a code length N and code rate r of an LDPC code in units of 360 columns (i.e., the number of unit columns P of the cyclic structure). In the i -th row of the parity check matrix initial value table, row numbers of elements of 1 in the $\{1+360 \times (i-1)\}$ -th column of the parity check matrix H (i.e., row numbers in which the row number of the first row of the parity check matrix H is set to 0), the number of which is equal to the number of column weights assigned to the $\{1+360 \times (i-1)\}$ -th column, are arranged.

[0369]

Here, since the parity matrix H_T (Fig. 10) of the parity check matrix H , corresponding to the parity length M , is determined in the manner illustrated in Fig. 25, the information matrix H_A (Fig. 10) of the parity check matrix H , corresponding to the information length K , is determined using the parity check matrix initial value table.

[0370]

The number of rows $x + 1$ of the parity check matrix

initial value table differs depending on the information length K .

[0371]

A relationship given by Expression (9) is established between the information length K and the number of rows $k + 1$ of the parity check matrix initial value table.

[0372]

$$K = (k + 1) \times 360 \quad \dots (9)$$

[0373]

Here, in Expression (9), 360 is the number of unit columns P of the cyclic structure described with reference to Fig. 26.

[0374]

In the parity check matrix initial value table illustrated in Fig. 38, 13 values are arranged in each of the first to third rows, and three values are arranged in each of the fourth to $(k+1)$ -th row (in Fig. 38, the 30th row).

[0375]

Accordingly, the column weights of the parity check matrix H determined from the parity check matrix initial value table illustrated in Fig. 38 are 13 for the first to $\{1-360 \times (3-1)-1\}$ -th columns, and 3 for the $\{1-360 \times (3-1)\}$ -th to K -th columns.

[0376]

In the parity check matrix initial value table illustrated in Fig. 38, the first row shows 0, 2084, 1613, 1548, 1286, 1460, 3196, 4297, 2481, 3369, 3451, 4620, and 2622, indicating that the elements of the rows with the row numbers 0, 2084, 1613, 1548, 1286, 1460, 3196, 4297, 2481, 3369, 3451, 4620, and 2622 in the first column of the parity check matrix H are 1 (and that the other elements are 0).

[0377]

In the parity check matrix initial value table illustrated in Fig. 38, furthermore, the second row shows 1, 122, 1516, 3448, 2880, 1407, 1847, 3799, 3529, 373, 971, 4358, and 3108, indicating that the elements of the rows with the row numbers 1, 122, 1516, 3448, 2880, 1407, 1847, 3799, 3529, 373, 971, 4358, and 3108 in the 361st ($= 1 + 360 \times (2 - 1)$) column of the parity check matrix H are 1.

[0378]

In the manner described above, a parity check matrix initial value table shows the positions of elements of 1 in an information matrix H_1 of a parity check matrix H in units of 360 columns.

[0379]

The elements in the columns other than the $\{1+360 \times (i-1)\}$ -th column of the parity check matrix H , that is, the elements in the $\{2+360 \times (i-1)\}$ -th to $\{360 \times i\}$ -th columns, are arranged by cyclically shifting the elements of 1 in the

$\{1+360 \times (i-1)\}$ -th column, which are defined using the parity check matrix initial value table, downward (i.e., downward along the columns) in a periodic manner in accordance with the parity length M .

[0380]

More specifically, for example, the elements in the $\{2+360 \times (i-1)\}$ -th column are obtained by cyclically shifting the elements in the $\{1+360 \times (i-1)\}$ -th column downward by $M/360 (= q)$. The elements in the subsequent $\{3+360 \times (i-1)\}$ -th column are obtained by cyclically shifting the elements in the $\{1+360 \times (i-1)\}$ -th column downward by $2 \times M/360 (= 2 \times q)$ (i.e., by cyclically shifting the elements in the $\{2+360 \times (i-1)\}$ -th column downward by $M/360 (= q)$).

[0381]

It is assumed now that the value in the i -th row (i.e., the i -th row from the top) and the j -th column (i.e., the j -th column from the left) of a parity check matrix initial value table is represented by $h_{i,j}$, and the row number of the j -th element of 1 in the w -th column of a parity check matrix H is represented by $H_{w,j}$. In this case, the row number H_w of an element of 1 in the w -th column, which is a column other than the $\{1+360 \times (i-1)\}$ -th column of the parity check matrix P , can be determined using Expression (10).

[0382]

$$H_w = \text{mod}(h_{i,j} + \text{mod}((w-1), P) \times q, M)$$

... (10)

[0383]

Here, $\text{mod}(x, y)$ represents the remainder after division of x by y .

[0384]

In addition, P denotes the number of unit columns of cyclic structure, described above, and is, for example, 360 in the DVB-S.2, DVB-T.2, and DVB-C.2 standards, as described above. Further, q denotes the value $M/360$ that is obtained by dividing the parity length M by the number of unit columns P of the cyclic structure (≈ 360).

[0385]

The parity check matrix generation unit 613 (Fig. 35) specifies a row number of an element of 1 in the $(i+360 \times (j-1))$ -th column of the parity check matrix H by using the parity check matrix initial value table.

[0386]

The parity check matrix generation unit 613 (Fig. 35) further determines the row number H_{w-} of an element of 1 in the w -th column, which is a column other than the $(i+360 \times (j-1))$ -th column of the parity check matrix H , in accordance with Expression (10), and generates a parity check matrix H whose elements corresponding to the row numbers obtained in the way described above are 1.

[0387]

[New LDPC Codes]

[0388]

Incidentally, there has been a demand for proposing an improved version (hereinafter also referred to as "DVB-Sx") of the DVB-S.2 standard.

[0389]

In the CfT (Call for Technology), which was submitted in the meeting for DVB-Sx standardization, a certain number of ModCodes (which are combinations of modulation schemes (Modulation) and LDPC codes (Code)) are demanded for each range of C/N (Carrier to Noise Ratio) (SNR (Signal to Noise Ratio)) in accordance with use case.

[0390]

More specifically, in the CfT, the first request is to prepare 20 ModCodes for a C/N range of 7 dB from 5 dB to 12 dB for DTH (Direct To Home) use.

[0391]

In the CfT, additionally, the second request is to prepare 22 ModCodes for a C/N range of 12 dB from 12 dB to 24 dB, the third request is to prepare 12 ModCodes for a C/N range of 9 dB from -3 dB to 5 dB, and the fourth request is to prepare 5 ModCodes for a C/N range of 7 dB from -10 dB to -3 dB.

[0392]

In the CfT, furthermore, it is also requested that the

FER (Frame Error Rate) for the ModCods in the first to fourth requests be approximately 10^{-5} (or less).

[0393]

Note that, in the CFT, the first request has a priority of "1", which is the highest, whereas the second to fourth requests have a priority of "2", which is lower than the priority of the first request.

[0394]

Accordingly, the present technology provides (a parity check matrix of) an LDPC code capable of satisfying at least the first request having the highest priority in the CFT, as a new LDPC code.

[0395]

Fig. 39 illustrates BER/FER curves for LDPC codes having a code length N of 64k bits and 11 code rates, which are defined in the DVE-S.2, in a case where QPSK is employed as a modulation scheme.

[0396]

In Fig. 39, the horizontal axis represents E_s/N_0 (the ratio of the signal power per symbol to the noise power) corresponding to the C/N, and the vertical axis represents FER/BER. Note that, in Fig. 39, solid lines indicate FERs, and dotted lines indicate BERs (Bit Error Rates).

[0397]

In Fig. 39, FER (BER) curves for LDPC codes having a

code length N of 64k bits and 11 code rates, which are defined in the DVB-S.2 standard, are plotted for an E_s/N_0 range of 10 dB in a case where QPSK is employed as a modulation scheme.

[0398]

More specifically, in Fig. 39, 11 FER curves for ModCods for which the modulation scheme is fixed to QPSK are drawn for an E_s/N_0 range of approximately 10 dB from approximately -3 dB to approximately 7 dB.

[0399]

Accordingly, for LDPC codes having a code length N of 64k bits and 11 code rates, which are defined in the DVB-S.2 standard, the interval between FER curves for ModCods on average (hereinafter also referred to as an "average interval") is approximately 1 dB ($\approx 10 \text{ dB} / (10 - 1)$).

[0400]

In contrast, since the first request in the CFT requests that 20 ModCods be prepared for an E_s/N_0 (C/N) range of 7 dB, the average interval between FER curves for ModCods is approximately 0.3 dB ($\approx 7 \text{ dB} / (20 - 1)$).

[0401]

In a case where the modulation scheme is fixed to one type such as QPSK, LDPC codes with code rates, the number of which is approximately three times ($\approx 1 \text{ dB} / 0.3 \text{ dB}$) the 11 code rates, or approximately 30 code rates, would be

sufficient to ensure sufficient room to obtain ModCods having an average interval of 0.3 dB which meets the first request in the CFT, compared to the case of DVB-S.2 in which ModCods having an average interval of approximately 1 dB are obtained using LDPC codes with the 11 code rates.

[0402]

In the present technology, accordingly, LDPC codes having a code length of 64k and code rates of $i/30$ (where i is a positive integer less than 30) are prepared as LDPC codes having code rates for which approximately 30 code rates are readily settable, and are provided as new LDPC codes which meet at least the first request having the highest priority in the CFT.

[0403]

It is to be noted that parity matrices H_p of parity check matrices H of the new LDPC codes have a stepwise structure (Fig. 11), similarly to an LDPC code defined in the DVB-S.2 standard, in terms of keeping compatibility with DVB-S.2 as much as possible.

[0404]

In addition, similarly to an LDPC code defined in the DVB-S.2 standard, information matrices H_A of parity check matrices H of the new LDPC codes have a cyclic structure, where the number of unit columns P of the cyclic structure is also 360.

[0405]

Figs. 40 to 106 are diagrams illustrating an example of parity check matrix initial value tables for new LDPC codes having a code length N of 64k bits and code rates of $i/30$, as described above.

[0406]

Here, the new LDPC codes are LDPC codes whose code rates are represented by $i/30$, and therefore include LDPC codes having up to 29 code rates, $1/30$, $2/30$, $3/30$, ..., $28/30$, and $29/30$.

[0407]

However, an LDPC code with a code rate of $1/30$ may be used in a limited fashion in terms of efficiency. In addition, an LDPC code with a code rate of $29/30$ may be used in a limited fashion in terms of error rate (BER/FER).

[0408]

For the reason described above, among LDPC codes with 29 code rates, namely, code rates of $1/30$ to $29/30$, one or both of an LDPC code with a code rate of $1/30$ and an LDPC code with a code rate of $29/30$ can be configured not to be used as new LDPC codes.

[0409]

Herein, LDPC codes with 28 code rates, for example, LDPC codes with code rates of $2/30$ to $29/30$ among code rates of $1/30$ to $29/30$, are used as new LDPC codes, and parity

check matrix initial value tables for parity check matrices H of the new LDPC codes will be given hereinbelow.

[0410]

Fig. 40 illustrates a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of $2/30$.

[0411]

Fig. 41 illustrates a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of $3/30$.

[0412]

Fig. 42 illustrates a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of $4/30$.

[0413]

Fig. 43 illustrates a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of $5/30$.

[0414]

Fig. 44 illustrates a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of $6/30$.

[0415]

Fig. 45 illustrates a parity check matrix initial value table for a parity check matrix H of an LDPC code having a

code length N of 64k bits and a code rate r of $7/30$.

[0416]

Figs. 46 and 47 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of $8/30$.

[0417]

Figs. 48 and 49 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of $9/30$.

[0418]

Figs. 50 and 51 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of $10/30$.

[0419]

Figs. 52 and 53 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of $11/30$.

[0420]

Figs. 54 and 55 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of

12/30.

[0421]

Figs. 56 and 57 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of 13/30.

[0422]

Figs. 58 and 59 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of 14/30.

[0423]

Figs. 60 and 61 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of 15/30.

[0424]

Figs. 62, 63, and 64 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of 16/30.

[0425]

Figs. 65, 66, and 67 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of

17/30.

[0426]

Figs. 68, 69, and 70 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of 18/30.

[0427]

Figs. 71, 72, and 73 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of 19/30.

[0428]

Figs. 74, 75, and 76 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of 20/30.

[0429]

Figs. 77, 78, and 79 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of 21/30.

[0430]

Figs. 80, 81, and 82 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of

22/30.

[0431]

Figs. 83, 84, and 85 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of 23/30.

[0432]

Figs. 86, 87, and 88 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of 24/30.

[0433]

Figs. 89, 90, and 91 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of 25/30.

[0434]

Figs. 92, 93, and 94 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of 26/30.

[0435]

Figs. 95, 96, 97, and 98 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate

r of 27/30.

[0436]

Figs. 99, 100, 101, and 102 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of 28/30.

[0437]

Figs. 103, 104, 105, and 106 illustrate a parity check matrix initial value table for a parity check matrix H of an LDPC code having a code length N of 64k bits and a code rate r of 29/30.

[0438]

The LDPC encoder 115 (Figs. 8 and 35) is capable of performing encoding on a (new) LDPC code having a code length N of 64k bits and any of 28 code rates r of 2/30 to 29/30 by using a parity check matrix H determined from one of the parity check matrix initial value tables illustrated in Figs. 40 to 106.

[0439]

In the illustrated example, the storage unit 602 of the LDPC encoder 115 (Fig. 8) stores the parity check matrix initial value tables illustrated in Figs. 40 to 106.

[0440]

It is to be noted that not all the LDPC codes with 28 code rates r of 2/30 to 29/30 (which are determined from the

parity check matrix initial value tables) illustrated in Figs. 40 to 106 may be used as new LDPC. That is, an LDPC code or codes with any one or more code rates among the LDPC codes with 28 code rates r of $2/30$ to $29/30$ illustrated in Figs. 40 to 106 may be employed as a new LDPC code or codes. [0441]

LDPC codes obtained using parity check matrices H determined from the parity check matrix initial value tables illustrated in Figs. 40 to 106 may be high-performance LDPC codes. [0442]

The term "high-performance LDPC code", as used herein, refers to an LDPC code obtained from an appropriate parity check matrix H . [0443]

Furthermore, the term "appropriate parity check matrix H " refers to a parity check matrix satisfying a certain condition in which the BER (and FER) is (or are) reduced when an LDPC code obtained from a parity check matrix H is transmitted with a low E_s/N_0 or E_b/N_0 (which is the ratio of the signal power per bit to the noise power). [0444]

An appropriate parity check matrix H may be determined through simulations for measuring BERs when, for example, LDPC codes obtained from various parity check matrices

satisfying a certain condition are transmitted with a low E_b/N_0 .

[0445]

Examples of the certain condition that an appropriate parity check matrix H is to satisfy include a condition that analysis results obtained using an analytical technique for the performance evaluation of codes, called density evolution, are good, and a condition that a loop of elements of 1, called cycle 4, does not exist.

[0446]

Here, it is well established that a concentration of elements of 1, like cycle 4, in an information matrix H_A will reduce the decoding performance of an LDPC code. Thus, the absence of cycle 4 is demanded as a certain condition that an appropriate parity check matrix H is to satisfy.

[0447]

Note that the certain condition that an appropriate parity check matrix H is to satisfy may be determined, as desired, in terms of various factors such as improved decoding performance of an LDPC code and easy (or simplified) decoding processing of an LDPC code.

[0448]

Figs. 107 and 108 are diagrams depicting density evolution through which analysis results are obtained, as a certain condition that an appropriate parity check matrix H

is to satisfy.

[0449]

Density evolution is a code analysis technique for calculating an expected value of error probability for the set of all LDPC codes ("ensemble") whose code length N , which is characterized by a degree sequence described below, is infinite (∞).

[0450]

For example, if a noise variance increases from zero in an AWGN channel, the expected value of error probability for a certain ensemble is initially zero, and becomes non-zero if the noise variance is greater than or equal to a certain threshold.

[0451]

In the density evolution method, it can be determined whether the ensemble performance (i.e., the appropriateness of a parity check matrix) is good or not, by comparing noise variance thresholds (hereinafter also referred to as "performance thresholds") over which the expected values of error probability for ensembles become non-zero.

[0452]

Note that the general performance of a specific LDPC code can be predicted by determining an ensemble including the LDPC code and performing density evolution on the ensemble.

[0453]

Accordingly, once an ensemble with good performance is found, an LDPC code with good performance may be found from among the LDPC codes included in the ensemble.

[0454]

Here, the degree sequence, described above, represents the ratio of variable nodes or check nodes with a weight of each value to the code length N of an LDPC code.

[0455]

For example, a regular (3,6) LDPC code with a code rate of $1/2$ belongs to an ensemble characterized by a degree sequence indicating that the weight (column weight) for all the variable nodes is 3 and the weight (row weight) for all the check nodes is 6.

[0456]

Fig. 107 illustrates a Tanner graph of the above-described ensemble.

[0457]

The Tanner graph illustrated in Fig. 107 includes N variable nodes indicated by circles ("O"); in Fig. 107, the number of which is equal to the code length N , and $N/2$ check nodes indicated by squares ("□") in Fig. 107, the number of which is equal to a value obtained by multiplying the code length N by the code rate $1/2$.

[0458]

Three edges, the number of which is equal to the column weight, are connected to each variable node. Therefore, $3N$ edges in total are connected to the N variable nodes.

[0459]

In addition, six edges, the number of which is equal to the row weight, are connected to each check node. Therefore, $3N$ edges in total are connected to the $N/2$ check nodes.

[0460]

In the Tanner graph illustrated in Fig. 107, one interleaver is also included.

[0461]

The interleaver randomly reorders the $3N$ edges connected to the N variable nodes, and connects each of the reordered edges to one of the $3N$ edges connected to the $N/2$ check nodes.

[0462]

There are $(3N)!$ ($= (3N) \times (3N-1) \times \dots \times 1$) reordering patterns in which the interleaver reorders the $3N$ edges connected to the N variable nodes. Accordingly, an ensemble characterized by a degree sequence indicating that the weight for all the variable nodes is 3 and the weight for all the check nodes is 6 is the set of $(3N)!$ LDPC codes.

[0463]

In a simulation for determining an LDPC code with good performance (i.e., an appropriate parity check matrix), a

multi-edge type ensemble was used in density evolution.

[0464]

In the multi-edge type, an interleaver through which edges connected to variable nodes and edges connected to check nodes extend is divided into a plurality of pieces (multi-edge), which may allow more accurate characterization of an ensemble.

[0465]

Fig. 108 illustrates an example of a Tanner graph of a multi-edge type ensemble.

[0466]

In the Tanner graph illustrated in Fig. 108, two interleavers, namely, a first interleaver and a second interleaver, are included.

[0467]

In addition, the Tanner graph illustrated in Fig. 108 includes v_1 variable nodes each having one edge connected to the first interleaver and zero edges connected to the second interleaver, v_2 variable nodes each having one edge connected to the first interleaver and two edges connected to the second interleaver, and v_3 variable nodes each having zero edges connected to the first interleaver and two edges connected to the second interleaver.

[0468]

The Tanner graph illustrated in Fig. 108 further

includes c1 check nodes each having two edges connected to the first interleaver and zero edges connected to the second interleaver, c2 check nodes each having two edges connected to the first interleaver and two edges connected to the second interleaver, and c3 check nodes each having zero edges connected to the first interleaver and three edges connected to the second interleaver.

[0463]

Here, density evolution and an implementation thereof are described in, for example, "On the Design of Low-Density Parity-Check Codes within 0.0045 dB of the Shannon Limit", S.Y. Chung, G.D. Forney, T.J. Richardson, R. Urbanke, IEEE Communications Letters, VOL. 5, NO. 2, Feb 2001.

[0470]

In a simulation for determining (a parity check matrix initial value table of) a new LDPC code, an ensemble for which the performance threshold, which is E_b/N_0 (which is the ratio of the signal power per bit to the noise power) at which a BER begins to drop (i.e., decreases), is less than or equal to a certain value was found using multi-edge type density evolution, and an LDPC code that reduces a BER in a plurality of modulation schemes used in DVB-S.2 and the like, such as QPSK, was selected as an LDPC code with good performance from among the LDPC codes belonging to the ensemble.

[0471]

The parity check matrix initial value tables of the new LDPC codes described above are parity check matrix initial value tables of LDPC codes having a code length N of 64k bits, which are determined through the simulations described above.

[0472]

Fig. 109 is a diagram illustrating minimum cycle lengths and performance thresholds for parity check matrices H which are determined from parity check matrix initial value tables of new LDPC codes having a code length N of 54k bits and 28 code rates of $2/30$ to $29/30$ illustrated in Figs. 40 to 106.

[0473]

Here, a minimum cycle length (or girth) is a minimum value of the length (loop length) of a loop composed of elements of 1 in a parity check matrix H .

[0474]

Cycle 4 (a loop of elements of 1, with a loop length of 4) does not exist in a parity check matrix H determined from a parity check matrix initial value table of a new LDPC code.

[0475]

In addition, as the code rate r decreases, the redundancy of an LDPC code increases. Thus, the performance threshold tends to be improved (i.e., decreased) as the code

rate r decreases.

[0476]

Fig. 110 is a diagram depicting a parity check matrix H (hereinafter also referred to as a "parity check matrix H of a new LDPC code") (determined from each of the parity check matrix initial value tables) illustrated in Figs. 40 to 106.

[0477]

The parity check matrix H of the new LDPC code has a column weight X for KX columns, starting with the first column, a column weight of $Y1$ for the subsequent $KY1$ columns, a column weight of $Y2$ for the subsequent $KY2$ columns, a column weight of 2 for the subsequent $(M-1)$ columns, and a column weight of 1 for the last column.

[0478]

Here, the sum of columns given by $KX+KY1+KY2+M-1+1$ equals the code length $N = 64800$ bits.

[0479]

Fig. 111 is a diagram illustrating the numbers of columns KX , $KY1$, $KY2$, and M , and the column weights X , $Y1$, and $Y2$ illustrated in Fig. 110 for the respective code rates r of the new LDPC codes.

[0480]

In a parity check matrix H of a new LDPC code having a code length N of 64k, similarly to the parity check matrix described with reference to Figs. 12 and 13, the column

weight tends to increase as the ordinal number of the columns of the parity check matrix H decreases (i.e., as the column comes closer to the left end of the parity check matrix H). Accordingly, robustness to errors (or resistance to errors) tends to increase as the ordinal number of the code bits of a new LDPC code decreases (i.e., the first code bit tends to be the most robust to errors).

[0481]

It is noted that the amount of shift q used in cyclic shifting which is performed to determine a parity check matrix from a parity check matrix initial value table of a new LDPC code having a code length N of 64k in the way described with reference to Fig. 38 is represented by the equation $q = M/P = M/360$.

[0482]

Accordingly, the amounts of shift for new LDPC codes with code rates of 2/30, 3/30, 4/30, 5/30, 6/30, 7/30, 8/30, 9/30, 10/30, 11/30, 12/30, 13/30, 14/30, 15/30, 16/30, 17/30, 18/30, 19/30, 20/30, 21/30, 22/30, 23/30, 24/30, 25/30, 26/30, 27/30, 28/30, and 29/30 are 168, 162, 156, 150, 144, 138, 132, 126, 120, 114, 108, 102, 96, 90, 84, 78, 72, 66, 60, 54, 48, 42, 36, 30, 24, 18, 12, and 6, respectively.

[0483]

Figs. 112, 113, and 114 are diagrams illustrating simulated BERs/FERs for the new LDPC codes illustrated in

Figs. 40 to 106.

[0484]

The simulations were based on the assumption of an AWGN communication path (or channel), in which BPSK was employed as a modulation scheme and the number of times of repetitive decoding $C(it)$ was 50.

[0485]

In Figs. 112, 113, and 114, the horizontal axis represents E_b/N_0 , and the vertical axis represents BER/FER. Note that solid lines indicate BERs and dotted lines indicate FERs.

[0486]

In Figs. 112 to 114, FER (BER) curves for the respective new LDPC codes with 28 code rates of 2/39 to 29/30 exhibit FERs less than or equal to 10^{-5} for an E_b/N_0 range of (approximately) 15 dB from (substantially) -10 dB to 5 dB.

[0487]

In the simulations, 28 ModCods having an FER less than or equal to 10^{-5} for an E_b/N_0 range of 15 dB from -10 dB to 5 dB can be set. Accordingly, 20 or more ModCods having an FER less than or equal to 10^{-5} for a range of 7 dB from 5 dB to 12 dB can be sufficiently predicted to be set by taking into account various modulation schemes other than BPSK used in the simulations, such as QPSK, 8PSK, 16APSK, 32APSK,

16QAM, 32QAM, and 64QAM.

[0488]

Thus, it is possible to provide an LDPC code having good error-rate performance, meeting the first request in the CFT.

[0489]

In addition, referring to Figs. 112 to 114, most of FER (BER) curves for new LDPC codes are drawn at almost equal intervals less than 1 dB for each of low-, intermediate-, and high-code-rate groups. Accordingly, the new LDPC codes may provide broadcasters that broadcast programs using the transmitting device 11 with an advantage in facilitating selection of code rates to be used for broadcasting in accordance with the state of channels (i.e., the communication path 13).

[0490]

Note that, in the simulations for determining the BER/FER curves illustrated in Figs. 112 to 114, BCH encoding was performed on information, and the resulting BCH codes underwent LDPC encoding.

[0491]

Fig. 115 includes diagrams depicting BCH encoding which was used in the simulations.

[0492]

More specifically, part A of Fig. 115 is a diagram

illustrating parameters of BCH encoding that is performed prior to the LDPC encoding into an LDPC code of 64k, which is defined in the DVB-S.2 standard.

[0493]

In DVB-S.2, 192, 160, or 128 redundancy bits are added in accordance with the code rate of an LDPC code, thereby providing BCH encoding capable of 12-, 10-, or 8-bit error correction.

[0494]

Part B of Fig. 115 is a diagram illustrating parameters of BCH encoding which were used in the simulations.

[0495]

In the simulations, similarly to the case of DVB-S.2, BCH encoding capable of 12-, 10-, or 8-bit error correction was performed by addition of 192, 160, or 128 redundancy bits in accordance with the code rate of an LDPC code.

[0496]

[Example Configuration of Receiving Device 12]

[0497]

Fig. 116 is a block diagram illustrating an example configuration of the receiving device 12 illustrated in Fig. 7.

[0498]

An OFDM processing unit (OFDM operation) 151 receives an OFDM signal from the transmitting device 11 (Fig. 7), and

performs signal processing on the OFDM signal. The data (i.e., symbols) obtained through signal processing performed by the OFDM processing unit 151 is supplied to a frame management unit (Frame Management) 152.

[0499]

The frame management unit 152 performs processing (frame interpretation) of a frame including the symbols supplied from the OFDM processing unit 151 to obtain symbols of target data and symbols of control data, and supplies the symbols of the target data and the symbols of the control data to frequency deinterleavers 161 and 153, respectively.

[0500]

The frequency deinterleaver 153 performs frequency deinterleaving on the symbols supplied from the frame management unit 152 in units of symbols, and supplies the resulting symbols to a QAM decoder 154.

[0501]

The QAM decoder 154 demaps the symbols (i.e., symbols mapped to constellation points) supplied from the frequency deinterleaver 153 (i.e., decodes the constellation points) for orthogonal demodulation, and supplies the resulting data (i.e., an LDPC code) to an LDPC decoder 155.

[0502]

The LDPC decoder 155 performs LDPC decoding on the LDPC code supplied from the QAM decoder 154, and supplies the

resulting LDPC target data (in the illustrated example, a BCH code) to a BCH decoder 156.

[0503]

The BCH decoder 156 performs BCH decoding on the LDPC target data supplied from the LDPC decoder 155, and outputs the resulting control data (signalling).

[0504]

On the other hand, the frequency deinterleaver 161 performs frequency deinterleaving on the symbols supplied from the frame management unit 152 in units of symbols, and supplies the resulting symbols to an MISO/MIMO decoder 162.

[0505]

The MISO/MIMO decoder 162 performs space-time decoding on the data (i.e., symbols) supplied from the frequency deinterleaver 161, and supplies the resulting data to a time deinterleaver 163.

[0506]

The time deinterleaver 163 performs time deinterleaving on the data (i.e., symbols) supplied from the MISO/MIMO decoder 162 in units of symbols, and supplies the resulting data to a QAM decoder 164.

[0507]

The QAM decoder 164 demaps the symbols (i.e., symbols mapped to constellation points) supplied from the time deinterleaver 163 (i.e., decodes the constellation points)

for orthogonal demodulation, and supplies the resulting data (i.e., symbols) to a bit deinterleaver 165.

[0508]

The bit deinterleaver 165 performs bit deinterleaving on the data (i.e., symbols) supplied from the QAM decoder 164, and supplies the resulting LDPC code to an LDPC decoder 166.

[0509]

The LDPC decoder 166 performs LDPC decoding on the LDPC code supplied from the bit deinterleaver 165, and supplies the resulting LDPC target data (in the illustrated example, a BCH code) to a BCH decoder 167.

[0510]

The BCH decoder 167 performs BCH decoding on the LDPC target data supplied from the LDPC decoder 166, and supplies the resulting data to a BB descrambler 168.

[0511]

The BB descrambler 168 performs BB descrambling on the data supplied from the BCH decoder 167, and supplies the resulting data to a null deletion unit (Null Deletion) 169.

[0512]

The null deletion unit 169 deletes the null added by the padder 112 illustrated in Fig. 8, from the data supplied from the BB descrambler 168, and supplies the resulting data to a demultiplexer 170.

[0513]

The demultiplexer 170 separates one or more streams (target data) multiplexed in the data supplied from the null deletion unit 169, performs necessary processing, and outputs the resulting data as output streams.

[0514]

Note that the receiving device 12 may be configured without including some of the blocks illustrated in Fig. 116. More specifically, for example, if the transmitting device 11 (Fig. 8) is configured without including the time interleaver 118, the MISO/MIMO encoder 119, the frequency interleaver 120, and the frequency interleaver 124, the receiving device 12 may be configured without including the time deinterleaver 163, the MISO/MIMO decoder 162, the frequency deinterleaver 161, and the frequency deinterleaver 153, which are the blocks corresponding to the time interleaver 118, the MISO/MIMO encoder 119, the frequency interleaver 120, and the frequency interleaver 124 of the transmitting device 11, respectively.

[0515]

Fig. 117 is a block diagram illustrating an example configuration of the bit deinterleaver 165 illustrated in Fig. 116.

[0516]

The bit deinterleaver 165 includes a multiplexer (MUX)

54 and a column twist deinterleaver 55, and performs (bit) deinterleaving on the symbol bits of the symbols supplied from the QAM decoder 164 (Fig. 116).

[0517]

More specifically, the multiplexer 54 performs inverse permutation processing (which is the inverse of permutation processing), corresponding to the permutation processing performed by the demultiplexer 25 illustrated in Fig. 9, on the symbol bits of the symbols supplied from the QAM decoder 164. That is, the multiplexer 54 performs inverse permutation processing to restore the positions of the code bits (i.e., symbol bits) of the LDPC code permuted through the permutation processing to the original positions, and supplies the resulting LDPC code to the column twist deinterleaver 55.

[0518]

The column twist deinterleaver 55 performs column twist deinterleaving (which is the inverse of column twist interleaving), corresponding to column twist interleaving as the reordering processing performed by the column twist interleaver 24 illustrated in Fig. 9, on the LDPC code supplied from the multiplexer 54. That is, the column twist deinterleaver 55 performs inverse reordering processing, for example, column twist deinterleaving, to restore the code bits of the LDPC code whose order has been changed through

column twist interleaving as reordering processing to the original order.

[0519]

Specifically, the column twist deinterleaver 55 performs column twist deinterleaving by writing and reading the code bits of the LDPC code to and from a memory for deinterleaving which has a configuration similar to that of the memory 31 illustrated in, typically, Fig. 28.

[0520]

However, the column twist deinterleaver 55 writes code bits to the memory for deinterleaving in its row direction by using, as a write address, the read address at which a code bit has been read from the memory 31. In addition, the column twist deinterleaver 55 reads code bits from the memory for deinterleaving in its column direction by using, as a read address, the write address at which a code bit has been written to the memory 31.

[0521]

The LDPC code obtained as a result of column twist deinterleaving is supplied from the column twist deinterleaver 55 to the LDPC decoder 166.

[0522]

Here, if the LDPC code supplied from the QAM decoder 164 to the bit deinterleaver 165 has been subjected to parity interleaving, column twist interleaving, and

permutation processing, the bit deinterleaver 165 may perform all of the inverse operations, namely, parity deinterleaving corresponding to parity interleaving (which is the inverse of parity interleaving operation, i.e., parity deinterleaving for restoring the code bits of the LDPC code whose order has been changed through parity interleaving to the original order), inverse permutation processing corresponding to permutation processing, and column twist deinterleaving corresponding to column twist interleaving.

[0523]

In the bit deinterleaver 165 illustrated in Fig. 117, however, parity deinterleaving is not performed because the bit deinterleaver 165 does not include a block configured to perform parity deinterleaving corresponding to parity interleaving although it includes the multiplexer 54 that performs inverse permutation processing corresponding to permutation processing and the column twist deinterleaver 55 that performs column twist deinterleaving corresponding to column twist interleaving.

[0524]

Accordingly, the LDPC code on which inverse permutation processing and column twist deinterleaving have been performed but parity deinterleaving has not been performed is supplied from (the column twist deinterleaver 55 of) the

bit deinterleaver 165 to the LDPC decoder 166.

[0525]

The LDPC decoder 166 performs LDPC decoding on the LDPC code supplied from the bit deinterleaver 165 by using a transformed parity check matrix obtained by performing at least column permutation corresponding to parity interleaving on the parity check matrix H that the LDPC encoder 115 illustrated in Fig. 8 has used for LDPC encoding, and outputs the resulting data as a result of decoding the LDPC target data.

[0526]

Fig. 118 is a flowchart depicting a process performed by the QAM decoder 164, the bit deinterleaver 165, and the LDPC decoder 166 illustrated in Fig. 117.

[0527]

In step S111, the QAM decoder 164 demaps the symbols (i.e., symbols mapped to constellation points) supplied from the time deinterleaver 163 for orthogonal demodulation, and supplies the resulting data to the bit deinterleaver 165. Then, the process proceeds to step S112.

[0528]

In step S112, the bit deinterleaver 165 performs deinterleaving (i.e., bit deinterleaving) on the symbol bits of the symbols supplied from the QAM decoder 164. Then, the process proceeds to step S113.

[0529]

More specifically, in step S112, the multiplexer 54 in the bit deinterleaver 165 performs inverse permutation processing on the symbol bits of the symbols supplied from the QAM decoder 164, and supplies the code bits of the resulting LDPC code to the column twist deinterleaver 55.

[0530]

The column twist deinterleaver 55 performs column twist deinterleaving on the LDPC code supplied from the multiplexer 54, and supplies the resulting LDPC code to the LDPC decoder 166.

[0531]

In step S113, the LDPC decoder 166 performs LDPC decoding on the LDPC code supplied from the column twist deinterleaver 55 by using the parity check matrix H that the LDPC encoder 115 illustrated in Fig. 8 has used for LDPC encoding, that is, by using a transformed parity check matrix obtained by performing at least column permutation corresponding to parity interleaving on the parity check matrix H , and outputs the resulting data to the BCH decoder 167 as a result of decoding the LDPC target data.

[0532]

Note that, also in Fig. 117, similarly to the case illustrated in Fig. 9, the multiplexer 54 that performs inverse permutation processing and the column twist

deinterleaver 55 that performs column twist deinterleaving are configured as separate units, for convenience of illustration. However, the multiplexer 54 and the column twist deinterleaver 55 may be integrated into a single unit.

[0533]

In addition, if the bit interleaver 116 illustrated in Fig. 9 does not perform column twist interleaving, the bit deinterleaver 165 illustrated in Fig. 117 need not be provided with the column twist deinterleaver 55.

[0534]

Next, LDPC decoding performed by the LDPC decoder 166 illustrated in Fig. 116 will be described in further detail.

[0535]

As described above, the LDPC decoder 166 illustrated in Fig. 116 performs LDPC decoding on the LDPC code supplied from the column twist deinterleaver 55, on which inverse permutation processing and column twist deinterleaving have been performed but parity deinterleaving has not been performed, by using a transformed parity check matrix obtained by performing at least column permutation corresponding to parity interleaving on the parity check matrix H that the LDPC encoder 115 illustrated in Fig. 8 has used for LDPC encoding.

[0536]

Here, LDPC decoding may be performed using a

transformed parity check matrix so as to keep the operating frequency within a sufficiently feasible range while reducing the size of circuitry. Such LDPC decoding has been previously proposed (see, for example, Japanese Patent No. 4224777).

[0537]

Accordingly, first, LDPC decoding using a transformed parity check matrix, which has been previously proposed, will be described with reference to Figs. 119 to 122.

[0538]

Fig. 119 illustrates an example of a parity check matrix H of an LDPC code having a code length N of 90 and a code rate of $2/3$.

[0539]

Note that, in Fig. 119 (also in Figs. 120 and 121, described below), "0" is represented by a period (".").

[0540]

In the parity check matrix H illustrated in Fig. 119, a parity matrix has a stepwise structure.

[0541]

Fig. 120 illustrates a parity check matrix H' obtained by performing row permutation of Expression (11) and column permutation of Expression (12) on the parity check matrix H illustrated in Fig. 119.

[0542]

Row permutation: $(6s+t+1)$ -th row $\rightarrow$ $(5t+s+1)$ -th row

... (11)

[0543]

Column permutation: $(6x+y+61)$ -th column $\rightarrow$ $(5y+x+61)$ -th column

... (12)

[0544]

Note that, in Expressions (11) and (12), s , t , x , and y are integers in the ranges of $0 \leq s < 5$, $0 \leq t < 6$, $0 \leq x < 5$, and $0 \leq y < 6$, respectively.

[0545]

The row permutation of Expression (11) allows permutation such that the 1st, 7th, 13th, 19th, and 25th rows, whose numbers are divided by 6 yielding a remainder of 1, are replaced with the 1st, 2nd, 3rd, 4th, and 5th rows, respectively, and the 2nd, 8th, 14th, 20th, and 26th rows, whose numbers are divided by 6 yielding a remainder of 2, are replaced with the 6th, 7th, 8th, 9th, and 10th rows, respectively.

[0546]

Further, the column permutation of Expression (12) allows permutation such that the 61st, 67th, 73rd, 79th, and 85th columns, whose numbers are divided by 6 yielding a remainder of 1, among the columns subsequent to the 61st column (parity matrix), are replaced with the 61st, 62nd,

63rd, 64th, and 65th columns, respectively, and the 62nd, 68th, 74th, 80th, and 86th columns, whose numbers are divided by 6 yielding a remainder of 2, are replaced with the 66th, 67th, 68th, 69th, and 70th columns, respectively.

[0547]

A matrix obtained by performing row and column permutations on the parity check matrix H illustrated in Fig. 119 in the way described above is the parity check matrix H' illustrated in Fig. 120.

[0548]

Here, the row permutation of the parity check matrix H would not affect the order of the code bits of the LDPC code.

[0549]

Furthermore, the column permutation of Expression (12) corresponds to parity interleaving that is performed to interleave the $(K+qx+ty+1)$ -th code bit to the $(K+Py+x+1)$ -th code bit position as described above, when the information length K is 60, the number of unit columns P of the cyclic structure is 5, and the divisor q ($= M/P$) of the parity length M (in the illustrated example, 30) is 6.

[0550]

Accordingly, the parity check matrix H' illustrated in Fig. 120 is a transformed parity check matrix obtained by performing at least column permutation to replace the $(K+qx+ty+1)$ -th column of the parity check matrix (hereinafter

referred to as an "original parity check matrix" as appropriate) H illustrated in Fig. 119 with the $(K+Py+x+1)$ -th column.

[0551]

Multiplying the transformed parity check matrix H' illustrated in Fig. 120 by an LDPC code obtained by performing the same permutation as that of Expression (12) on the LDPC code of the original parity check matrix H illustrated in Fig. 119 yields a zero vector. More specifically, if a row vector obtained by performing column permutation of Expression (12) on a row vector c as an LDPC code (i.e., a code word) of the original parity check matrix H is represented by c' , Hc' is a zero vector due to the nature of the parity check matrix, and therefore $H'c'^T$ is also a zero vector.

[0552]

Thus, the transformed parity check matrix H' illustrated in Fig. 120 is a parity check matrix of an LDPC code c' obtained by performing column permutation of Expression (12) on the LDPC code c of the original parity check matrix H .

[0553]

Accordingly, a similar result of decoding to that obtained by decoding the LDPC code of the original parity check matrix H using the parity check matrix H may be

obtained by decoding (LDPC decoding) the LDPC code c' , which is obtained by performing column permutation of Expression (12) on the LDPC code c of the original parity check matrix H , using the transformed parity check matrix H' illustrated in Fig. 120 and then performing the inverse of the column permutation of Expression (12) on the decoded LDPC code c' .
[0554]

Fig. 121 illustrates the transformed parity check matrix H' illustrated in Fig. 120 whose elements are spaced apart from one another in units of 5×5 matrices.
[0555]

In Fig. 121, the transformed parity check matrix H' is represented by a combination of 5×5 ($= P \times P$) unit matrices, matrices each having one or more elements of 1 in a unit matrix which are replaced by elements of 0 (hereinafter referred to as "quasi-unit matrices" as appropriate), matrices produced by cyclically shifting a unit matrix or a quasi-unit matrix (hereinafter referred to as "shift matrices" as appropriate), matrices each of which is the sum of two or more of a unit matrix, a quasi-unit matrix, and a shift matrix (hereinafter referred to as "sum matrices" as appropriate), and 5×5 zero matrices.
[0556]

The transformed parity check matrix H' illustrated in Fig. 121 can be said to be composed of 5×5 unit matrices,

quasi-unit matrices, shift matrices, sum matrices, and zero matrices. These 5×5 matrices (unit matrices, quasi-unit matrices, shift matrices, sum matrices, and zero matrices) constituting the transformed parity check matrix H' are hereinafter referred to as "component matrices" as appropriate.

[0557]

An LDPC code of a parity check matrix represented by $P \times P$ component matrices may be decoded using an architecture that simultaneously performs check node computation and variable node computation each for P nodes.

[0558]

Fig. 122 is a block diagram illustrating an example configuration of a decoding device that performs the decoding operation described above.

[0559]

More specifically, Fig. 122 illustrates an example configuration of a decoding device configured to decode an LDPC code by using the transformed parity check matrix H' illustrated in Fig. 121, which is obtained by performing at least column permutation of Expression (12) on the original parity check matrix H illustrated in Fig. 119.

[0560]

The decoding device illustrated in Fig. 122 includes an edge data storage memory 300 having six FIFOs 300; to 300,, a

selector 301 for selecting one of the FIFOs 300₁ to 300₆, a check node calculation unit 302, two cyclic shift circuits 303 and 308, an edge data storage memory 304 having 18 FIFOs 304₁ to 304₁₈, a selector 305 for selecting one of the FIFOs 304₁ to 304₁₈, a received data memory 306 for storing received data, a variable node calculation unit 307, a decoded word calculation unit 309, a received data reordering unit 310, and a decoded data reordering unit 311. [0561]

First, a description will be made of a method for storing data in the edge data storage memories 300 and 304. [0562]

The edge data storage memory 300 includes the six FIFOs 300₁ to 300₆, the number of which is equal to a value obtained by dividing the number of rows of the transformed parity check matrix H' illustrated in Fig. 121, i.e., 30, by the number of rows of each component matrix (i.e., the number of unit columns P of the cyclic structure), i.e., 5. Each of the FIFOs 300 _{y} ($y = 1, 2, \dots, 6$) includes storage areas of multiple stages, and is configured such that messages corresponding to five edges, the number of which is equal to the number of rows and the number of columns of each component matrix (i.e., the number of unit columns P of the cyclic structure), can be simultaneously read from and written to the storage area of each stage. In addition, the

number of stages of the storage areas of each of the FIFOs 300_y is 9, which is the maximum of the numbers of 1s (Hamming weights) in the row direction of the transformed parity check matrix illustrated in Fig. 121.

[0563]

Data (i.e., messages v_i from variable nodes) corresponding to the positions of 1s in the first to fifth rows of the transformed parity check matrix H' illustrated in Fig. 121 is stored in the FIFO 300₁ in such a manner that every row is filled with the data elements in the lateral direction (i.e., 0s are ignored). More specifically, if the element in the j -th row and the i -th column is represented by (j,i) , data corresponding to the positions of 1s in the 5×5 unit matrix of $(1,1)$ to $(5,5)$ of the transformed parity check matrix H' is stored in the storage area of the first stage of the FIFO 300₁. Data corresponding to the positions of 1s in the shift matrix (which is a shift matrix obtained by cyclically shifting the 5×5 unit matrix to the right by three elements) of $(1,21)$ to $(5,25)$ of the transformed parity check matrix H' is stored in the storage area of the second stage. Similarly, data is stored in the storage areas of the third to eighth stages in association with the transformed parity check matrix H' . Furthermore, data corresponding to the positions of 1s in the shift matrix (which is a shift matrix obtained by replacing 1s in the

first row with 0s in the 5×5 unit matrix and cyclically shifting the 5×5 unit matrix to the left by one element) of (1,86) to (5,90) of the transformed parity check matrix H' is stored in the storage area of the ninth stage.

[0564]

Data corresponding to the positions of 1s in the sixth to tenth rows of the transformed parity check matrix H' illustrated in Fig. 121 is stored in the FIFO 300₂. More specifically, data corresponding to the positions of 1s in a first shift matrix included in a sum matrix (which is a sum matrix representing the sum of a first shift matrix obtained by cyclically shifting the 5×5 unit matrix to the right by one element and a second shift matrix obtained by cyclically shifting the 5×5 unit matrix to the right by two elements) of (6,1) to (10,5) of the transformed parity check matrix H' is stored in the storage area of the first stage of the FIFO 300₁. Furthermore, data corresponding to the positions of 1s in the second shift matrix included in the sum matrix of (6,1) to (10,5) of the transformed parity check matrix H' is stored in the storage area of the second stage.

[0565]

More specifically, in the case of a component matrix having a weight of 2 or more, when the component matrix is represented by the sum of two or more of a $P \times P$ unit matrix having a weight of 1, a quasi-unit matrix produced by

replacing one or more elements of 1 in the unit matrix with elements of 0, and a shift matrix produced by cyclically shifting the unit matrix or the quasi-unit matrix, data corresponding to the positions of 1s in the unit matrix having a weight of 1, the quasi-unit matrix, or the shift matrix (i.e., messages corresponding to edges belonging to the unit matrix, the quasi-unit matrix, or the shift matrix) is stored in the same address (i.e., the same FIFO among the FIFOs 300₁ to 300₆).

[0566]

Data is also stored in the storage areas of the subsequent third to ninth stages in association with the transformed parity check matrix H' .

[0567]

Similarly, data is stored in the FIFOs 300₇ to 300₈ in association with the transformed parity check matrix H' .

[0568]

The edge data storage memory 304 includes 18 FIFOs 304₁ to 304₁₈, the number of which is equal to a value obtained by dividing the number of columns of the transformed parity check matrix H' , i.e., 90, by the number of columns of each component matrix (i.e., the number of unit columns P of the cyclic structure), i.e., 5. Each of the FIFOs 304_x ($x = 1, 2, \dots, 18$) includes storage areas of multiple stages, and is configured such that messages corresponding to five edges,

the number of which is equal to the number of rows and the number of columns of each component matrix (i.e., the number of unit columns P of the cyclic structure), can be simultaneously read from and written to the storage area of each stage.

[0569]

Data (i.e., messages u_i from check nodes) corresponding to the positions of 1s in the first to fifth columns of the transformed parity check matrix H' illustrated in Fig. 121 is stored in the FIFO 304; in such a manner that every column is filled with the data elements in the longitudinal direction (i.e., 0s are ignored). Specifically, data corresponding to the positions of 1s in the 5×5 unit matrix of (1,1) to (5,5) of the transformed parity check matrix H' is stored in the storage area of the first stage of the FIFO 304₁. Data corresponding to the positions of 1s in a first shift matrix included in a sum matrix (which is a sum matrix representing the sum of a first shift matrix obtained by cyclically shifting the 5×5 unit matrix to the right by one element and a second shift matrix obtained by cyclically shifting the 5×5 unit matrix to the right by two elements) of (6,1) to (10,5) of the transformed parity check matrix H' is stored in the storage area of the second stage. Furthermore, data corresponding to the positions of 1s in the second shift matrix included in the sum matrix of

(6,1) to (10,5) of the transformed parity check matrix H' is stored in the storage area of the third stage.

[0570]

More specifically, in the case of a component matrix having a weight of 2 or more, when the component matrix is represented by the sum of two or more of a $P \times P$ unit matrix having a weight of 1, a quasi-unit matrix produced by replacing one or more elements of 1 in the unit matrix with elements of 0, and a shift matrix produced by cyclically shifting the unit matrix or the quasi-unit matrix, data corresponding to the positions of 1s in the unit matrix having a weight of 1, the quasi-unit matrix, or the shift matrix (i.e., messages corresponding to edges belonging to the unit matrix, the quasi-unit matrix, or the shift matrix) is stored in the same address (i.e., the same FIFO among the FIFOs 304₁ to 304₁₈).

[0571]

Data is also stored in the storage areas of the subsequent fourth and fifth stages in association with the transformed parity check matrix H' . The number of stages of storage areas of the FIFO 304₁ is 5, which is the maximum of the numbers of 1s (Hamming weights) in the row direction in the first to fifth columns of the transformed parity check matrix H' .

[0572]

Similarly, data is also stored in the FIFOs 304₁ and 304₂ in association with the transformed parity check matrix H', with the respective lengths (the numbers of stages) being 5. Data is also stored in the FIFOs 304₃ to 304₁₂ in association with the transformed parity check matrix H', with the respective lengths being 3. Data is also stored in the FIFOs 304₁₃ to 304₁₈ in association with the transformed parity check matrix H', with the respective lengths being 2. [0573]

A description will now be made of the operation of the decoding device illustrated in Fig. 122. [0574]

The edge data storage memory 300, which includes the six FIFOs 300₁ to 300₆, selects a FIFO to store data from among the FIFOs 300₁ to 300₆ in accordance with information (matrix data) D312 indicating which row in the transformed parity check matrix H' illustrated in Fig. 121 five messages D311 supplied from the cyclic shift circuit 308 located upstream of the edge data storage memory 300 belong to, and collectively stores the five messages D311 in the selected FIFO in order. Further, when reading data, the edge data storage memory 300 reads five messages D300₁ in order from the FIFO 300₁, and supplies the read messages D300₁ to the selector 301 located downstream of the edge data storage memory 300. After the reading of messages from the FIFO 300₁

is completed, the edge data storage memory 300 also reads messages in order from the FIFOs 300₂ to 300₅, and supplies the read messages to the selector 301.

[0575]

The selector 301 selects five messages received from a FIFO from which data is currently being read among the FIFOs 300₁ to 300₆ in accordance with a selection signal D301, and supplies the selected messages as messages D302 to the check node calculation unit 302.

[0576]

The check node calculation unit 302 includes five check node calculators 302₁ to 302₅, and performs check node computation in accordance with Expression (7) using the messages D302 (D302₁ to D302₅) (corresponding to messages v_i in Expression (7)) supplied through the selector 301. The check node calculation unit 302 supplies five messages D303 (D303₁ to D303₅) (corresponding to messages u_i in Expression (7)) obtained as a result of the check node computation to the cyclic shift circuit 303.

[0577]

The cyclic shift circuit 303 cyclically shifts the five messages D303₁ to D303₅ determined by the check node calculation unit 302 on the basis of information (matrix data) D305 indicating the number of original unit matrices (or quasi-unit matrices) which have been cyclically shifted

in the transformed parity check matrix H' to obtain the corresponding edge, and supplies results to the edge data storage memory 304 as messages D304.

{0578}

The edge data storage memory 304, which includes the 18 FIFOs 304₁ to 304₁₈, selects an FIFO to store data from among the FIFOs 304₁ to 304₁₈ in accordance with information D305 indicating which row in the transformed parity check matrix H' the five messages D304 supplied from the cyclic shift circuit 303 located upstream of the edge data storage memory 304 belong to, and collectively stores the five messages D304 in the selected FIFO in order. Further, when reading data, the edge data storage memory 304 reads five messages D306₁ in order from the FIFO 304₁, and supplies the read messages D306₁ to the selector 305 located downstream of the edge data storage memory 304. After the reading of data from the FIFO 304₁ is completed, the edge data storage memory 304 also reads messages in order from the FIFOs 304₂ to 304₁₈, and supplies the read messages to the selector 305.

{0579}

The selector 305 selects five messages from a FIFO from which data is currently being read among the FIFOs 304₁ to 304₁₈ in accordance with a selection signal D307, and supplies the selected messages as messages D308 to the variable node calculation unit 307 and the decoded word

calculation unit 309.

[0580]

On the other hand, the received data reordering unit 310 reorders an LDPC code D313 corresponding to the parity check matrix H illustrated in Fig. 119, which has been received through the communication path 13, by performing column permutation of Expression (12), and supplies the resulting data as received data D314 to the received data memory 306. The received data memory 306 calculates reception LLRs (log-likelihood ratios) from the received data D314 supplied from the received data reordering unit 310, and stores the reception LLRs. The received data reordering unit 310 further collectively supplies the reception LLRs in units of five reception LLRs as reception values D309 to the variable node calculation unit 307 and the decoded word calculation unit 309.

[0581]

The variable node calculation unit 307 includes five variable node calculators 307₁ to 307₅, and performs variable node computation in accordance with Expression (1) using the messages D308 (D308₁ to D308₅) (i.e., messages u_i in Expression (1)) supplied through the selector 305 and the five reception values D309 (reception values $u_{r,i}$ in Expression (1)) supplied from the received data memory 306. The variable node calculation unit 307 supplies messages

D310 (D310₁ to D310₅) (i.e., messages v_i in Expression (1)) obtained as a result of the computation to the cyclic shift circuit 308.

[0582]

The cyclic shift circuit 308 cyclically shifts the messages D310₁ to D310₅ calculated by the variable node calculation unit 307 on the basis of information indicating the number of original unit matrices (or quasi-unit matrices) which have been cyclically shifted in the transformed parity check matrix H' to obtain the corresponding edge, and supplies results to the edge data storage memory 300 as messages D311.

[0583]

The series of operations described above can be performed once to perform single decoding of an LDPC code (variable node computation and check node computation). After decoding an LDPC code a certain number of times, the decoding device illustrated in Fig. 122 determines and outputs final decoded data through the decoded word calculation unit 309 and the decoded data reordering unit 311.

[0584]

More specifically, the decoded word calculation unit 309 includes five decoded word calculators 309₁ to 309₅, and serves as a final stage of a plurality of decoding

operations to calculate decoded data (i.e., a decoded word) in accordance with Expression (5) using the five messages D308 (D308₁ to D308₅) (i.e., messages u_i in Expression (5)) output from the selector 305 and the five reception values D309 (i.e., reception values u_{0i} in Expression (5)) supplied from the received data memory 306. The decoded word calculation unit 309 supplies decoded data D315 obtained as a result of the calculation to the decoded data reordering unit 311.

[0585]

The decoded data reordering unit 311 changes the order of the decoded data D315 supplied from the decoded word calculation unit 309 by performing the inverse of the column permutation of Expression (12), and outputs the resulting data as final decoded data D316.

[0586]

As described above, one or both of the row permutation and the column permutation are performed on the parity check matrix (i.e., the original parity check matrix) to convert the parity check matrix into a parity check matrix (i.e., a transformed parity check matrix) that can be represented by a combination of component matrices, namely, a $P \times P$ unit matrix, a quasi-unit matrix produced by replacing one or more elements of 1 with elements of 0, a shift matrix produced by cyclically shifting the unit matrix or the

quasi-unit matrix, a sum matrix representing the sum of two or more of the unit matrix, the quasi-unit matrix, and the shift matrix, and a $P \times P$ zero matrix. This allows decoding of an LDPC code by using an architecture that simultaneously performs check node computation and variable node computation each for P nodes, where P is less than the number of rows or the number of columns of the parity check matrix. The use of an architecture that simultaneously performs node computation (computation of check nodes and computation of variable nodes) for P nodes, where P is less than the number of rows or the number of columns of a parity check matrix, makes it possible to perform multiple repetitive decoding while keeping the operating frequency within a feasible range, compared to the case where node computation is simultaneously performed for nodes, the number of which is equal to the number of rows or the number of columns of a parity check matrix.

[0587]

Similarly to the decoding device illustrated in Fig. 122, the LDPC decoder 166 included in the receiving device 12 illustrated in Fig. 116 is configured to perform LDPC decoding by, for example, simultaneously performing check node computation and variable node computation each for P nodes.

[0588]

More specifically, it is assumed now that, for ease of description, the parity check matrix of the LDPC code output from the LDPC encoder 115 included in the transmitting device 11 illustrated in Fig. 8 is, for example, the parity check matrix H illustrated in Fig. 119 in which a parity matrix has a stepwise structure. In this case, the parity interleaver 23 of the transmitting device 11 performs parity interleaving to interleave the $(K+qx+y+1)$ -th code bit to the $(K+Py+x+1)$ -th code bit position with the information length K being 60, the number of unit columns P of the cyclic structure being 5, and the divisor $q (= M/P)$ of the parity length M being 6.

[0589]

As described above, this parity interleaving operation corresponds to the column permutation of Expression (12). Thus, it is not necessary for the LDPC decoder 166 to perform the column permutation of Expression (12).

[0590]

In the receiving device 12 illustrated in Fig. 116, therefore, as described above, an LDPC code on which parity deinterleaving has not been performed, that is, an LDPC code on which the column permutation of Expression (12) has been performed, is supplied from the column twist deinterleaver 55 to the LDPC decoder 166. The LDPC decoder 166 performs processing similar to that of the decoding device

illustrated in Fig. 122, except that the column permutation of Expression (12) is not performed.

[0591]

More specifically, Fig. 123 illustrates an example configuration of the LDPC decoder 166 illustrated in Fig. 116.

[0592]

In Fig. 123, the LDPC decoder 166 has a configuration similar to the decoding device illustrated in Fig. 122, except that the received data reordering unit 310 illustrated in Fig. 122 is not included, and performs processing similar to that of the decoding device illustrated in Fig. 122, except that the column permutation of Expression (12) is not performed, which is not described herein.

[0593]

As described above, the LDPC decoder 166 may be configured without including the received data reordering unit 310, and can be smaller in size than the decoding device illustrated in Fig. 122.

[0594]

Note that, in Figs. 119 to 123, for ease of illustration, the code length N of an LDPC code is 90, the information length K is 60, the number of unit columns P of the cyclic structure (i.e., the number of rows and the

number of columns of a component matrix) is 5, and the divisor q ($= M/P$) of the parity length M is 6. However, the code length N , the information length K , the number of unit columns P of the cyclic structure, and the divisor q ($= M/P$) are not limited to the values described above.

[0595]

More specifically, the LDPC encoder 115 in the transmitting device 11 illustrated in Fig. 8 outputs an LDPC code with, for example, the code length N being 64800, 16200, or the like, the information length K being given by $N - Pq$ ($= N - M$), the number of unit columns P of the cyclic structure being 360, and the divisor q being given by M/P . The LDPC decoder 166 illustrated in Fig. 123 may be used to perform LDPC decoding on the LDPC code described above by simultaneously performing check node computation and variable node computation each for P nodes.

[0596]

Fig. 124 includes diagrams depicting the processing of the multiplexer 54 included in the bit deinterleaver 165 illustrated in Fig. 117.

[0597]

More specifically, part A of Fig. 124 illustrates an example functional configuration of the multiplexer 54.

[0598]

The multiplexer 54 includes an inverse permutation unit

1001 and a memory 1002.

[0599]

The multiplexer 54 performs inverse permutation processing (which is the inverse of permutation processing), corresponding to the permutation processing performed by the demultiplexer 25 of the transmitting device 11, on the symbol bits of the symbols supplied from the QAM decoder 164 located upstream of the multiplexer 54. That is, the multiplexer 54 performs inverse permutation processing to restore the positions of the code bits (symbol bits) of the LDPC code that have been permuted through the permutation processing to the original positions, and supplies the resulting LDPC code to the column twist deinterleaver 55 located downstream of the multiplexer 54.

[0600]

More specifically, mb symbol bits $y_0, y_1, \dots, y_{mb-1}$ of b symbols are supplied to the inverse permutation unit 1001 in the multiplexer 54 in units of (consecutive) b symbols.

[0601]

The inverse permutation unit 1001 performs inverse permutation to restore the mb symbol bits y_0 to y_{mb-1} to the order of the mb original code bits $b_0, b_1, \dots, b_{mb-1}$ (i.e., the order of the code bits b_0 to b_{mb-1} before the permutation unit 32 included in the demultiplexer 25 on the transmitting device 11 side performs permutation), and outputs the

resulting mb code bits b_0 to b_{mb-1} .

{0602}

Similarly to the memory 31 included in the demultiplexer 25 on the transmitting device 11 side, the memory 1002 has a storage capacity to store mb bits in its row (horizontal) direction and $N/(mb)$ bits in its column (vertical) direction. In other words, the memory 1002 includes mb columns for storing $N/(mb)$ bits.

{0603}

Note that code bits of the LDPC code output from the inverse permutation unit 1001 are written to the memory 1002 in the direction in which a code bit is read from the memory 31 in the demultiplexer 25 of the transmitting device 11, and the code bits written in the memory 1002 are read from the memory 1002 in the direction in which a code bit is written to the memory 31.

{0604}

Accordingly, as illustrated in part A of Fig. 124, the multiplexer 54 of the receiving device 12 writes code bits of the LDPC code output from the inverse permutation unit 1001 in the row direction in units of mb bits, where the writing operation moves from the top to the bottom of the memory 1002, starting from the first row.

{0605}

Further, when the writing of code bits corresponding to

one code length is completed, the multiplexer 54 reads the code bits from the memory 1002 in the column direction, and supplies the read code bits to the column twist deinterleaver 55 located downstream of the multiplexer 54.

[0606]

Here, part B of Fig. 124 is a diagram illustrating the reading of code bits from the memory 1002.

[0607]

The multiplexer 54 reads code bits of the LDPC code (in the column direction) from the top to the bottom of each of the columns of the memory 1002, where the reading operation moves toward the right, starting from the leftmost column.

[0608]

Fig. 125 is a diagram depicting the processing of the column twist deinterleaver 55 included in the bit deinterleaver 165 illustrated in Fig. 117.

[0609]

More specifically, Fig. 125 illustrates an example configuration of the memory 1002 of the multiplexer 54.

[0610]

The memory 1002 has a storage capacity to store mb bits in its column (vertical) direction and $N/(mb)$ bits in its row (horizontal) direction, and includes mb columns.

[0611]

The column twist deinterleaver 55 performs column twist

deinterleaving by controlling a read start position when code bits of the LDPC code are written to the memory 1002 in the row direction and are read from the memory 1002 in the column direction.

[0612]

More specifically, the column twist deinterleaver 55 performs inverse reordering processing to restore the code bits whose order has been changed through column twist interleaving to the original order, by changing the read start position with which the reading of a code bit is started, as desired, for each of a plurality of columns.

[0613]

Here, Fig. 125 illustrates an example configuration of the memory 1002 in a case where, as described with reference to Fig. 28, the modulation scheme is 16APSK, 16QAM, or the like and the multiple b is 1. In this case, the number of bits m of one symbol is 4, and the memory 1002 includes 4 ($=mb$) columns.

[0614]

Instead of the multiplexer 54, the column twist deinterleaver 55 writes code bits of the LDPC code output from the inverse permutation unit 1001 in the row direction, where the writing operation moves downward sequentially from the first row of the memory 1002.

[0615]

Further, when the writing of code bits corresponding to one code length is completed, the column twist deinterleaver 55 reads the code bits from the memory 1002 (in the column direction) from the top to the bottom, where the reading operation moves toward the right, starting from the leftmost column.

[0616]

Note that the column twist deinterleaver 55 reads code bits from the memory 1002, using, as a read start position of the code bit, the write start position from which the column twist interleaver 24 on the transmitting device 11 side writes a code bit.

[0617]

More specifically, if the address of the position of the first (or top) of each column is represented by 0 and the addresses of the respective positions in the column direction are represented by integers arranged in ascending order, the column twist deinterleaver 55 sets the read start position for the leftmost column to the position at the address 0, the read start position for the second column (from the left) to the position at the address 2, the read start position for the third column to the position at the address 4, and the read start position for the fourth column to the position at the address 7 in a case where the modulation scheme is 16APSK or 16QAM and the multiple m is 4.

[0618]

Note that, after reading code bits up to the bottom of the column for which the read start position is set to a position other than the position at the address 0, the column twist deinterleaver 55 returns to the first position (i.e., the position at the address 0), and reads code bits up to the position immediately before the read start position. The column twist deinterleaver 55 then performs reading from the subsequent (right) column.

[0619]

The column twist deinterleaving operation described above allows the order of code bits that have been reordered through column twist interleaving to return to the original order.

[0620]

Fig. 126 is a block diagram illustrating another example configuration of the bit deinterleaver 165 illustrated in Fig. 116.

[0621]

Note that, in Fig. 126, portions corresponding to those illustrated in Fig. 117 are assigned the same reference numerals, and a description thereof will be omitted hereinafter, as appropriate.

[0622]

More specifically, the bit deinterleaver 165

illustrated in Fig. 126 has a configuration similar to that illustrated in Fig. 117, except that a parity deinterleaver 1011 is further included.

[0623]

In Fig. 126, the bit deinterleaver 165 includes a multiplexer (MUX) 54, a column twist deinterleaver 55, and a parity deinterleaver 1011, and performs bit deinterleaving on code bits of the LDPC code supplied from the QAM decoder 164.

[0624]

More specifically, the multiplexer 54 performs inverse permutation processing (which is the inverse of permutation processing), corresponding to the permutation processing performed by the demultiplexer 25 of the transmitting device 11, on the LDPC code supplied from the QAM decoder 164. That is, the multiplexer 54 performs inverse permutation processing to restore the positions of the code bits permuted through permutation processing to the original positions, and supplies the resulting LDPC code to the column twist deinterleaver 55.

[0625]

The column twist deinterleaver 55 performs column twist deinterleaving, corresponding to column twist interleaving as the reordering processing performed by the column twist interleaver 24 of the transmitting device 11, on the LDPC

code supplied from the multiplexer 54.

[0626]

The LDPC code obtained as a result of column twist deinterleaving is supplied from the column twist deinterleaver 55 to the parity deinterleaver 1011.

[0627]

The parity deinterleaver 1011 performs parity deinterleaving (which is the inverse of parity interleaving operation), corresponding to parity interleaving performed by the parity interleaver 23 of the transmitting device 11, on the code bits on which column twist deinterleaving has been performed by the column twist deinterleaver 55. That is, the parity deinterleaver 1011 performs parity deinterleaving to restore the code bits of the LDPC code whose order has been changed through parity interleaving to the original order.

[0628]

The LDPC code obtained as a result of parity deinterleaving is supplied from the parity deinterleaver 1011 to the LDPC decoder 166.

[0629]

Accordingly, the bit deinterleaver 165 illustrated in Fig. 126 supplies an LDPC code on which inverse permutation processing, column twist deinterleaving, and parity deinterleaving have been performed, i.e., an LDPC code

obtained through LDPC encoding in accordance with the parity check matrix H , to the LDPC decoder 166.

[0630]

The LDPC decoder 166 performs LDPC decoding on the LDPC code supplied from the bit deinterleaver 165 by using the parity check matrix H that the LDPC encoder 115 of the transmitting device 11 has used for LDPC encoding. More specifically, the LDPC decoder 166 performs LDPC decoding on the LDPC code supplied from the bit deinterleaver 165 by using the parity check matrix H that the LDPC encoder 115 of the transmitting device 11 has used for LDPC encoding, or by using a transformed parity check matrix obtained by performing at least column permutation, corresponding to parity interleaving, on the parity check matrix H .

[0631]

Here, in Fig. 126, an LDPC code obtained through LDPC encoding in accordance with the parity check matrix H is supplied from (the parity deinterleaver 1011 of) the bit deinterleaver 165 to the LDPC decoder 166. Accordingly, in a case where the LDPC decoding of the LDPC code is performed using the parity check matrix H that the LDPC encoder 115 of the transmitting device 11 has used for LDPC encoding, the LDPC decoder 166 may be implemented as, for example, a decoding device configured to perform LDPC decoding using a full serial decoding method for sequentially performing

computation of messages (i.e., check node messages and variable node messages) on a node-by-node basis, or a decoding device configured to perform LDPC decoding using a full parallel decoding method for simultaneously (or in parallel) performing computation of messages for all the nodes.

[0632]

Furthermore, in a case where the LDPC decoder 166 performs LDPC decoding on an LDPC code using a transformed parity check matrix obtained by performing at least column permutation, corresponding to parity interleaving, on the parity check matrix H that the LDPC encoder 115 of the transmitting device 11 has used for LDPC encoding, the LDPC decoder 166 may be implemented as a decoding device having an architecture that simultaneously performs check node computation and variable node computation each for P (or a divisor of P other than 1) nodes, which is the decoding device (Fig. 122) including the received data reordering unit 310 configured to perform column permutation similar to column permutation for obtaining a transformed parity check matrix on an LDPC code to reorder the code bits of the LDPC code.

[0633]

Note that, in Fig. 126, the multiplexer 54 that performs inverse permutation processing, the column twist

deinterleaver 55 that performs column twist deinterleaving, and the parity deinterleaver 1011 that performs parity deinterleaving are configured as separate units, for convenience of illustration. However, two or more of the multiplexer 54, the column twist deinterleaver 55, and the parity deinterleaver 1011 may be integrated into a single unit, similarly to the parity interleaver 23, the column twist interleaver 24, and the demultiplexer 25 of the transmitting device 11.

[0634]

In addition, if the bit interleaver 116 (Fig. 8) of the transmitting device 11 is configured without including the parity interleaver 23 or the column twist interleaver 24, the bit deinterleaver 165 illustrated in Fig. 126 may be configured without including the column twist deinterleaver 55 or the parity deinterleaver 1011.

[0635]

Also in this case, the LDPC decoder 166 may be implemented as a decoding device of the full serial decoding type that performs LDPC decoding using the parity check matrix H itself, a decoding device of the full parallel decoding type that performs LDPC decoding using the parity check matrix H itself, or the decoding device (Fig. 122) including the received data reordering unit 310 configured to perform LDPC decoding by simultaneously performing check

node computation and variable node computation each for P nodes using a transformed parity check matrix H' .

[0636]

[Example Configuration of Receiving System]

[0637]

Fig. 127 is a block diagram illustrating a first example configuration of a receiving system to which the receiving device 12 is applicable.

[0638]

In Fig. 127, the receiving system includes an acquisition unit 1101, a transmission path decoding processing unit 1102, and an information source decoding processing unit 1103.

[0639]

The acquisition unit 1101 acquires a signal including an LDPC code obtained by performing at least LDPC encoding on LDPC target data such as image data and audio data of a program via a transmission path (or communication path) (not illustrated) such as terrestrial digital broadcasting, satellite digital broadcasting, a CATV network, the Internet, or any other suitable network, and supplies the signal to the transmission path decoding processing unit 1102.

[0640]

Here, in a case where the acquisition unit 1101 acquires a signal broadcasted from, for example, a broadcast

station via terrestrial, satellite, CATV (Cable Television), or any other network, the acquisition unit 1101 may be implemented as a tuner, an STB (Set Top Box), or the like. Further, in a case where the acquisition unit 1101 acquires a signal transmitted using, for example, multicast technology like IPTV (Internet Protocol Television) from a web server, the acquisition unit 1101 may be implemented as a network I/F (Interface) such as a NIC (Network Interface Card).

[0641]

The transmission path decoding processing unit 1102 corresponds to the receiving device 12. The transmission path decoding processing unit 1102 performs a transmission path decoding process, including at least processing for correcting errors caused in a transmission path, on the signal acquired by the acquisition unit 1101 via a transmission path, and supplies the resulting signal to the information source decoding processing unit 1103.

[0642]

More specifically, the signal acquired by the acquisition unit 1101 via a transmission path is a signal obtained by performing at least error correcting encoding to correct errors caused in a transmission path. The transmission path decoding processing unit 1102 performs a transmission path decoding process such as an error

correction process on the above-described signal.

[0643]

Here, examples of the error correcting encoding include LDPC encoding and BCH encoding. Here, at least LDPC encoding is performed as error correcting encoding.

[0644]

Furthermore, the transmission path decoding process may include, for example, demodulation of modulation signals.

[0645]

The information source decoding processing unit 1103 performs an information source decoding process, including at least processing for expanding compressed information into original information, on the signal on which the transmission path decoding process has been performed.

[0646]

More specifically, the signal acquired by the acquisition unit 1101 via a transmission path may have been subjected to compression encoding for compressing information in order to reduce the amount of data such as image data and audio data as information. In this case, the information source decoding processing unit 1103 performs an information source decoding process, such as processing for expanding compressed information into original information (i.e., expansion processing), on the signal on which the transmission path decoding process has been performed.

[0647]

Note that, if the signal acquired by the acquisition unit 1101 via a transmission path has not been subjected to compression encoding, the information source decoding processing unit 1103 does not perform processing for expanding compressed information into original information.

[0648]

Here, examples of the expansion processing include MPEG decoding. Furthermore, the transmission path decoding process may include descrambling and so forth in addition to expansion processing.

[0649]

In the receiving system having the configuration described above, the acquisition unit 1101 acquires a signal obtained by performing compression encoding such as MPEG encoding and error correcting encoding such as LDPC encoding on data such as image data and audio data, via a transmission path, and supplies the acquired signal to the transmission path decoding processing unit 1102.

[0650]

The transmission path decoding processing unit 1102 performs a transmission path decoding process, for example, processing similar to that performed by the receiving device 12, on the signal supplied from the acquisition unit 1101, and supplies the resulting signal to the information source

decoding processing unit 1103.

[0651]

The information source decoding processing unit 1103 performs an information source decoding process such as MPEC decoding on the signal supplied from the transmission path decoding processing unit 1102, and outputs the resulting images or audio.

[0652]

The receiving system illustrated in Fig. 127 as described above may be applied to, for example, a television tuner or the like that receives television broadcasting as digital broadcasting.

[0653]

Note that the acquisition unit 1101, the transmission path decoding processing unit 1102, and the information source decoding processing unit 1103 may be constructed as single independent devices (hardware (such as ICs (Integrated Circuits)) or software modules).

[0654]

In addition, the acquisition unit 1101, the transmission path decoding processing unit 1102, and the information source decoding processing unit 1103 may be configured such that the combination of the acquisition unit 1101 and the transmission path decoding processing unit 1102, the combination of the transmission path decoding processing

unit 1102 and the information source decoding processing unit 1103, or the combination of the acquisition unit 1101, the transmission path decoding processing unit 1102, and the information source decoding processing unit 1103 is constructed as a single independent device.

[0655]

Fig. 128 is a block diagram illustrating a second example configuration of the receiving system to which the receiving device 12 is applicable.

[0656]

Note that, in Fig. 128, portions corresponding to those illustrated in Fig. 127 are assigned the same reference numerals, and a description thereof will be omitted hereinafter, as appropriate.

[0657]

The receiving system illustrated in Fig. 128 is common to that illustrated in Fig. 127 in that the acquisition unit 1101, the transmission path decoding processing unit 1102, and the information source decoding processing unit 1103 are included, and is different from that illustrated in Fig. 127 in that an output unit 1111 is further included.

[0658]

The output unit 1111 may be, for example, a display device configured to display an image or a speaker configured to output audio, and outputs images, audio, or

the like as signals output from the information source decoding processing unit 1103. In other words, the output unit 1111 displays images or outputs audio.

[0659]

The receiving system illustrated in Fig. 128 as described above may be applied to, for example, a TV set (television receiver) that receives television broadcasting as digital broadcasting or a radio receiver that receives radio broadcasting.

[0660]

Note that, if the signal acquired by the acquisition unit 1101 has not been subjected to compression encoding, a signal output from the transmission path decoding processing unit 1102 is supplied to the output unit 1111.

[0661]

Fig. 129 is a block diagram illustrating a third example configuration of the receiving system to which the receiving device 12 is applicable.

[0662]

Note that, in Fig. 129, portions corresponding to those illustrated in Fig. 127 are assigned the same reference numerals, and a description thereof will be omitted hereinafter, as appropriate.

[0663]

The receiving system illustrated in Fig. 129 is common

to that illustrated in Fig. 127 in that the acquisition unit 1101 and the transmission path decoding processing unit 1102 are included.

[0664]

However, the receiving system illustrated in Fig. 129 is different from that illustrated in Fig. 127 in that the information source decoding processing unit 1103 is not included and a recording unit 1121 is further included.

[0665]

The recording unit 1121 records (or stores) the signal (e.g., TS packets of an MPEG TS stream) output from the transmission path decoding processing unit 1102 on (or in) a recording (or storage) medium such as an optical disk, a hard disk (magnetic disk), or a flash memory.

[0666]

The receiving system illustrated in Fig. 129 as described above may be applied to, for example, a recorder that records television broadcasting.

[0667]

Note that, in Fig. 129, the receiving system may include the information source decoding processing unit 1103, and the recording unit 1121 is capable of recording a signal that has been subjected to an information source decoding process by the information source decoding processing unit 1103, that is, an image or audio obtained by decoding.

[0668]

[Embodiment of Computer]

[0669]

Next, the series of processes described above may be performed by hardware or software. If the series of processes is performed by software, a program constituting the software is installed into a general-purpose computer or the like.

[0670]

Thus, Fig. 130 illustrates an example configuration of an embodiment of a computer into which a program for executing the series of processes described above is installed.

[0671]

The program may be recorded in advance on a hard disk 705 or a ROM 703 serving as a recording medium incorporated in the computer.

[0672]

Alternatively, the program may be temporarily or persistently stored in (or recorded on) a removable recording medium 711 such as a flexible disc, a CD-ROM (Compact Disc Read Only Memory), an MO (Magneto Optical) disc, a DVD (Digital Versatile Disc), a magnetic disk, or a semiconductor memory. The removable recording medium 711 may be provided as packaged software.

[0673]

The program may be installed into the computer from the removable recording medium 711 described above, or may be wirelessly transferred to the computer from a download site via an artificial satellite for digital satellite broadcasting or transferred to the computer via a network such as a LAN (Local Area Network) or the Internet by wired connection. In the computer, the program transferred in the way described above may be received by a communication unit 708, and installed into the hard disk 705 incorporated in the computer.

[0674]

The computer has a CPU (Central Processing Unit) 702 incorporated therein. An input/output interface 710 is connected to the CPU 702 via a bus 701. When an instruction is input by a user by, for example, operating an input unit 707 including a keyboard, a mouse, a microphone, and so forth via the input/output interface 710, the CPU 702 executes a program stored in the ROM (Read Only Memory) 703 in accordance with the instruction. Alternatively, the CPU 702 loads a program stored in the hard disk 705, a program transferred from a satellite or a network, received by the communication unit 708, and installed into the hard disk 705, or a program read from the removable recording medium 711 set in a drive 709 and installed into the hard disk 705 into

a RAM (Random Access Memory) 704, and executes the loaded program. Accordingly, the CPU 702 performs processing according to the flowcharts described above or processing performed with the configurations in the block diagrams described above. Then, the CPU 702 outputs a result of the processing, if necessary, for example, from an output unit 706 including an LCD (Liquid Crystal Display), a speaker, and so forth via the input/output interface 710, transmits the result from the communication unit 708, or records the result on the hard disk 705.

[0675]

It should be noted herein that processing steps describing a program for causing a computer to perform various kinds of processing may not necessarily be processed in a time-series manner in accordance with the order described herein in the flowcharts, and may also include processes executed in parallel or individually (for example, parallel processing or object-based processing).

[0676]

In addition, a program may be processed by a single computer, or may be processed by a plurality of computers in a distributed manner. Furthermore, a program may also be transferred to and executed by a remote computer.

[0677]

Note that embodiments of the present technology are not

limited to the embodiments described above, and a variety of changes can be made without departing from the scope of the present technology.

[0678]

More specifically, for example, the (parity check matrix initial value tables of) new LDPC codes described above may be used regardless of whether the communication path 13 (Fig. 7) is a satellite link, a terrestrial link, a cable (wired line), or any other unit. In addition, the new LDPC codes may also be used for data transmission other than digital broadcasting.

Reference Signs List

[0679]

11 transmitting device, 12 receiving device, 23 parity interleaver, 24 column twist interleaver, 25 demultiplexer, 31 memory, 32 permutation unit, 54 multiplexer, 55 column twist interleaver, 111 mode adaptation/multiplexer, 112 padder, 113 BB scrambler, 114 BCH encoder, 115 LDPC encoder, 116 bit interleaver, 117 QAM encoder, 118 time interleaver, 119 MISO/MIMO encoder, 120 frequency interleaver, 121 BCH encoder, 122 LDPC encoder, 123 QAM encoder, 124 frequency interleaver, 131 frame builder & resource allocation unit, 132 OFDM generation unit, 151 OFDM processing unit, 152 frame management unit, 153 frequency deinterleaver, 154 QAM decoder, 155 LDPC decoder, 156 BCH decoder, 161 frequency

deinterleaver, 162 MISO/MIMO decoder, 163 time deinterleaver,
164 QAM decoder, 165 bit deinterleaver, 166 LDPC decoder,
167 BCH decoder, 168 BB descrambler, 169 null deletion unit,
170 demultiplexer, 300 edge data storage memory, 301
selector, 302 check node calculation unit, 303 cyclic shift
circuit, 304 edge data storage memory, 305 selector, 306
received data memory, 307 variable node calculation unit,
308 cyclic shift circuit, 309 decoded word calculation unit,
310 received data reordering unit, 311 decoded data
reordering unit, 601 encoding processing unit, 602 storage
unit, 611 code rate setting unit, 612 initial value table
read unit, 613 parity check matrix generation unit, 614
information bit read unit, 615 encoding parity computation
unit, 616 control unit, 701 bus, 702 CPU, 703 ROM, 704 RAM,
705 hard disk, 706 output unit, 707 input unit, 708
communication unit, 709 drive, 710 input/output interface,
711 removable recording medium, 1001 inverse permutation
unit, 1002 memory, 1011 parity deinterleaver, 1101
acquisition unit, 1101 transmission path decoding processing
unit, 1102 information source decoding processing unit, 1111
output unit, 1121 recording unit

CLAIMS

[Claim 1]

A data processing apparatus comprising:

an encoding unit configured to encode information bits into an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 24/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

1504	2103	2621	2840	3869	4594	5246	6314	7327	7364	10425
11934	12898	12954								
27	1903	3923	4513	7812	8098	8428	9789	10519	11345	12032
12157	12573	12930								
17	191	660	2451	2475	2976	3398	3616	5769	6724	8641
10046	11552	12842								
13	1366	4993	6468	7689	8563	9131	10012	10914	11574	
11837	12203	12715	12946							
432	872	7607	3286	3306	3385	4137	5563	7549	9339	9948

12315 12656 12929

1113 1394 4104 4186 7240 8827 11522 11833 12359 12363
12629 12821 12904 12946

14 441 1432 1677 2432 8981 11473 11507 12599 12783
12793 12912 12922 12943

1579 1806 7971 8586 9845 10357 11600 12007 12020 12339
12576 12817 12830 12904

20 546 3672 5538 6944 8052 8781 9743 12269 12393 12418
12549 12555 12718

1 3540 4397 5011 6626 8617 9587 10360 10602 11402 11983
12068 12495 12838

30 1572 4908 7421 8041 8910 8963 11005 11530 12240
12340 12467 12892 12933

33 2060 3907 4215 5545 8306 8655 8743 8806 9315 9364
10685 11954 12959

1338 2596 4876 5207 9555 10421 10929 11648 11739 12375
12416 12643 12742 12754

9469 10544 10932 11250 11426 11582 11846 12139 12202
12210 12356 12378 12873 12929

2681 3337 3616 6113 7078 8167 8624 9697 10902 11781
11855 12395 12475 12659

28 4086 5432 6555 6848 7368 8794 11483 11572 12414
12816 12894 12936 12957

5 5044 5572 9023 9192 9589 9979 10009 10855 10991 11715
12314 12610 12945

17 272 602 5681 6530 9572 9886 11061 11495 12238 12265
12483 12885 12955

22 2245 4282 4469 5007 6650 6733 10151 10401 11571
12004 12261 12805 12844

23 3270 4468 8621 9662 11240 11934 12091 12444 12691
12717 12858 12888 12917

740 1519 4923 6191 7878 8350 9293 10779 11020 11287
11630 12792 12862 12920

12 28 3584 6072 7079 8075 10477 11130 11383 11780 12341
12667 12818 12927

14 118 5283 5382 8301 9097 9413 9664 10437 10701 11124
12685 12730 12734

32 1426 3078 4325 5355 7780 9042 9928 10077 10377 10679
11191 11750 12611

1 669 3831 3980 5381 5412 6552 8453 9435 10243 11546
11821 11987 12807

232 483 919 1232 2156 2396 2990 3774 8539 8704 8819
10810 11868 12634

2381 7309 9334

348 6494 12623

4872 6257 11090

7 11970 11985

6615 12788 12855

1173 5269 12647

1344 7738 8118

17 4828 9175
2329 6034 12642
1254 2366 5013
2984 5078 5664
7423 10265 11528
1656 8526 8716
22 287 2837
18 100 3079
299 3171 12169
33 5920 11144
1286 3650 9309
2283 8809 12588
3139 8242 9081
2507 6846 8113
5211 8722 12689
1064 2592 8659
6136 6925 12958
1256 12789 12932
4274 8045 8788
1824 3209 6326
11 8899 12669
6243 6338 8730
641 9679 12831
3459 9876 11195
3226 5148 2173

9078 12126 12771

10907 11278 12731

3392 4020 12838

2814 11588 12909

6063 9214 11519

6064 6827 12683

1610 2452 6582

903 6289 8074

4592 8138 12952

2587 6271 9945

2733 11844 11893

581 4601 10020

14 5597 6049

343 3582 5931

5263 6521 12046

1394 2457 5251

11 4627 12747

2650 10266 12390

6285 11893 12062

10143 12892 12956

8448 11917 12330

4209 11693 12356

1529 2360 9086

5389 8148 10224

64 4676 12962

9483 12659 12887

3587 6767 12478

3122 5245 9044

3267 10118 11466

1347 3857 6705

9384 9576 11971

1366 8708 10758

412 4249 12863

1676 10488 11850

17 1605 2455

14 111 6045

11368 12919 12953

10388 11530 12937

4549 5143 12218

3088 4185 11674

23 2554 7823

6615 9291 9863

2229 3629 10855

3818 5509 12764

2740 11525 12914

8297 8611 12948

3606 11104 12920

5097 10412 12759

6502 7266 12072

5425 5490 10728

22 73 8462
32 12439 12657
8483 9540 10430
7275 7377 7420
5748 9726 12356
5672 6150 9156
28 3527 5857
520 7099 11335
405 6173 12865
5847 12843 12934
4289 7679 10386
2950 3021 12938
8844 11214 12955
2130 10760 12665
734 4790 12940
8 6991 12772
19 8205 11289
12 1440 9077
8670 8837 12951
3531 9166 12937
15 8901 8929
838 10114 11740
2648 9959 10934
323 7499 12877
5505 5659 11395

6627 12709 12933
364 1976 12888
8213 9124 12793
9588 10088 11108
299 890 11634
7368 7598 11602
28 4669 12585
15 27 12474
1426 3614 4205
30 2087 11147
6226 6259 12941.

[Claim 2]

The data processing apparatus according to Claim 1,
wherein

where a row of the parity check matrix initial value
table is represented by i and a parity length of the LDPC
code is represented by M ,

a $(2+360 \times (i-1))$ -th column of the parity check matrix is
a column obtained by cyclically shifting a $(i+360 \times (i-1))$ -th
column of the parity check matrix, in which positions of
elements of i are represented in the parity check matrix
initial value table, downward by q , where q is equal to
 $M/360$.

[Claim 3]

The data processing apparatus according to Claim 2,

wherein

for the $\{1+360 \times (i-1)\}$ -th column of the parity check matrix,

an i -th row of the parity check matrix initial value table represents a row number of an element of 1 in the $\{1+360 \times (i-1)\}$ -th column of the parity check matrix, and

for each of the $\{2+360 \times (i-1)\}$ -th to $\{360 \times i\}$ -th columns, which are columns other than the $\{1+360 \times (i-1)\}$ -th column of the parity check matrix,

a row number $H_{w,j}$ of an element of 1 in a w -th column of the parity check matrix, which is a column other than the $\{1+360 \times (i-1)\}$ -th column of the parity check matrix, is represented by equation $H_{w,j} = \text{mod}(h_{i,j} + \text{mod}((w-1), 360) \times M/360, M)$,

where $h_{i,j}$ denotes a value in the i -th row and a j -th column of the parity check matrix initial value table, and $H_{w,j}$ denotes a row number of a j -th element of 1 in the w -th column of the parity check matrix H .

{Claim 4}

The data processing apparatus according to Claim 2, wherein g is 36.

{Claim 5}

The data processing apparatus according to Claim 1, further comprising:

a parity interleaving unit configured to interleave

only parity bits in code bits of the LDPC code.

[Claim 6]

The data processing apparatus according to Claim 1,
further comprising:

a column twist interleaving unit configured to perform
column twist interleaving on the LDPC code by shifting code
bits of the LDPC code in a column direction and storing the
shifted code bits.

[Claim 7]

The data processing apparatus according to Claim 1,
further comprising:

a permutation unit configured to permute code bits of
the LDPC code to replace the code bits of the LDPC code with
symbol bits of a symbol corresponding to one of a certain
number of constellation points defined by a certain digital
modulation scheme.

[Claim 8]

The data processing apparatus according to Claim 7,
wherein

the permutation unit permutes the code bits that are
stored in a column direction and that are read in a row
direction.

[Claim 9]

The data processing apparatus according to Claim 1,
wherein

the parity check matrix is a parity check matrix that does not have cycle 4.

[Claim 10]

The data processing apparatus according to Claim 1, wherein

the parity check matrix is a parity check matrix of an LDPC code belonging to an ensemble of LDPC codes having a performance threshold less than or equal to a certain value, the performance threshold being an E_b/N_0 at which a BER begins to drop and being detected using multi-edge type density evolution.

[Claim 11]

A data processing method comprising:

an encoding step of encoding information bits into an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 24/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix

portion in units of 360 columns, including

1504 2103 2621 2840 3869 4594 5246 6314 7327 7364 10425
11934 12898 12954

27 1903 3923 4513 7812 8098 8428 9789 10519 11345 12032
12157 12573 12930

17 191 660 2451 2475 2976 3398 3616 5769 6724 8641
10046 11552 12842

13 1366 4993 6468 7689 8563 9131 10012 10914 11574
11837 12203 12715 12946

432 872 2603 3286 3306 3385 4137 5563 7540 9339 9948
12315 12656 12929

1113 1394 4104 4186 7240 8827 11522 11833 12359 12363
12629 12821 12904 12946

14 441 1432 1677 2432 8981 11478 11507 12599 12783
12793 12912 12922 12943

1579 1806 7971 8586 9845 10357 11600 12007 12020 12339
12576 12817 12830 12954

20 546 3672 5538 6944 8052 8781 9743 12269 12393 12418
12549 12555 12718

1 3540 4397 5011 6626 8617 9587 10360 10602 11402 11983
12068 12495 12938

30 1572 4908 7421 8041 8910 8963 11005 11930 12240
12340 12467 12892 12933

33 2060 3907 4215 5545 8306 8655 8743 8806 9315 9364
10685 11954 12959

1338 2596 4876 5207 9555 10421 10929 11648 11739 12375
12416 12643 12742 12754
9469 10544 10932 11250 11426 11582 11846 12139 12202
12210 12356 12378 12873 12929
2681 3337 3616 6113 7078 8167 8624 9697 10908 11781
11855 12095 12475 12659
28 4086 5432 6555 6848 7368 8794 11483 11572 12414
12816 12894 12936 12957
5 5044 5572 9023 9192 9589 9979 10009 10855 10991 11715
12314 12610 12945
17 272 602 5681 6530 9572 9886 11061 11495 12238 12265
12483 12885 12955
22 2245 4282 4469 5007 6650 6733 10151 10401 11571
12004 12261 12805 12844
23 3270 4468 8621 9662 11240 11934 12091 12444 12691
12717 12858 12888 12917
740 1519 4923 6191 7878 8350 9293 10779 11020 11287
11630 12792 12862 12920
12 28 3584 6072 7079 8075 10477 11130 11383 11780 12341
12667 12818 12927
14 118 5285 5382 8301 9097 9413 9664 10437 10701 11124
12685 12730 12734
32 1426 3078 4325 5353 7780 9042 9928 10077 10377 10679
11191 11750 12611
1 669 3831 2980 5381 5412 6552 8453 9435 10243 11546

11821 11987 12807

232 483 919 1232 2156 2396 2990 3774 8539 8704 8819

10810 11868 12634

2381 7309 9334

348 6494 12623

4872 6257 11090

7 11970 11985

6615 12788 12855

1173 5269 12647

1944 7738 8116

17 4828 9175

2329 6034 12642

1254 2366 5615

2984 5078 5664

7423 10265 11528

1656 8526 8716

22 287 2837

18 106 3679

299 3171 12169

33 5920 11144

1286 3650 9309

2283 8809 12588

3199 8242 9081

2507 6846 8113

5211 8722 12639

1064 2592 8659
6136 6925 12958
1256 12789 12932
4274 8045 8788
1824 3209 6926
11 8899 12669
6249 6338 8730
641 9679 12831
3459 9876 11185
3226 6148 8173
9078 12126 12771
10907 11278 12731
3392 4020 12838
2814 11588 12909
6063 9214 11519
6064 6827 12683
1610 2452 6582
903 6289 8074
4592 8138 12952
2587 6271 9945
2733 11844 11803
581 4601 10020
14 5597 6049
343 3582 5931
5263 6521 12846

1394 2457 5251

11 4627 12747

2650 10366 12390

6285 11893 12062

10143 12892 12956

8448 11917 12330

4209 11693 12356

1529 2360 9086

5389 8148 10224

64 4876 12862

9483 12659 12887

3587 6767 12478

3122 5245 9044

3267 10118 11466

1347 3857 6705

9384 9576 11971

1366 8708 10758

412 4249 12863

1676 10488 11850

17 1605 2455

14 111 6045

11368 12919 12953

10588 11530 12937

4549 5143 12218

3088 4185 11674

23 2554 7823

6615 9291 9863

2229 3629 10855

3818 5509 12764

2740 11525 12914

8297 8611 12948

3606 11104 12920

5097 10412 12759

6502 7266 12072

5425 5490 10728

22 73 8462

32 12439 12657

8483 9540 10430

7275 7377 7420

5748 9726 12356

5672 6150 9156

28 3527 5857

520 7099 11335

405 6173 12865

5847 12843 12934

4289 7679 10386

2950 8021 12938

8844 11214 12955

2130 10760 12665

734 4799 12940

8 6991 12772
19 8205 11289
12 1440 9077
8670 8837 12951
3531 9166 12937
15 8901 8929
838 10114 11740
2648 9959 10934
323 7499 12877
5505 5659 11395
6627 12709 12933
364 1976 12888
8213 9124 12793
9588 10088 11108
299 890 11634
7368 7598 11602
28 4669 12585
15 27 12474
1426 3614 4205
30 2087 11147
6226 6259 12941.

[Claim 12]

The data processing method according to Claim 11,
wherein

where a row of the parity check matrix initial value

table is represented by i and a parity length of the LDPC code is represented by M ,

a $\{2+360 \times (i-1)\}$ -th column of the parity check matrix is a column obtained by cyclically shifting a $\{1+360 \times (i-1)\}$ -th column of the parity check matrix, in which positions of elements of 1 are represented in the parity check matrix initial value table, downward by q , where q is equal to $M/360$.

[Claim 13]

The data processing method according to Claim 12, wherein

for the $\{1+360 \times (i-1)\}$ -th column of the parity check matrix,

an i -th row of the parity check matrix initial value table represents a row number of an element of 1 in the $\{1+360 \times (i-1)\}$ -th column of the parity check matrix, and

for each of the $\{2+360 \times (i-1)\}$ -th to $\{360 \times i\}$ -th columns, which are columns other than the $\{1+360 \times (i-1)\}$ -th column of the parity check matrix,

a row number $H_{w,j}$ of an element of 1 in a w -th column of the parity check matrix, which is a column other than the $\{1+360 \times (i-1)\}$ -th column of the parity check matrix, is represented by equation $H_{w,j} = \text{mod}(h_{1,j} + \text{mod}((w-1), 360) \times M/360, M)$,

where $h_{1,j}$ denotes a value in the i -th row and a j -th column

of the parity check matrix initial value table, and $R_{w,j}$ denotes a row number of a j -th element of 1 in the w -th column of the parity check matrix H .

[Claim 14]

The data processing method according to Claim 12, wherein q is 36.

[Claim 15]

The data processing method according to Claim 11, further comprising:

interleaving only parity bits in code bits of the LDPC code.

[Claim 16]

The data processing method according to Claim 11, further comprising:

performing column twist interleaving on the LDPC code by shifting code bits of the LDPC code in a column direction and storing the shifted code bits.

[Claim 17]

The data processing method according to Claim 11, further comprising:

permuting code bits of the LDPC code to replace the code bits of the LDPC code with symbol bits of a symbol corresponding to one of a certain number of constellation points defined by a certain digital modulation scheme.

[Claim 18]

The data processing method according to Claim 17,
wherein

the permuting of code bits includes permuting the code bits that are stored in a column direction and that are read in a row direction.

[Claim 19]

The data processing method according to Claim 11,
wherein

the parity check matrix is a parity check matrix that does not have cycle 4.

[Claim 20]

The data processing method according to Claim 11,
wherein

the parity check matrix is a parity check matrix of an LDPC code belonging to an ensemble of LDPC codes having a performance threshold less than or equal to a certain value, the performance threshold being an E_b/N_0 at which a BER begins to drop and being detected using multi-edge type density evolution.

[Claim 21]

A data processing apparatus comprising:

a decoding unit configured to decode an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 24/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,
the parity check matrix includes an information matrix
portion corresponding to the information bits and a parity
matrix portion corresponding to the parity bits,

the information matrix portion is represented by a
parity check matrix initial value table, and

the parity check matrix initial value table is a table
showing positions of elements of 1 in the information matrix
portion in units of 360 columns, including

1504 2103 2621 2840 3869 4594 5246 6314 7327 7364 10425
11934 12898 12954

27 1903 3923 4513 7812 8098 8428 9789 10519 11345 12032
12157 12573 12930

17 191 660 2451 2475 2976 3398 3616 5769 6724 8641
10046 11552 12842

13 1366 4993 6468 7689 8563 9131 10012 10914 11574
11837 12203 12715 12946

432 872 2603 3286 3306 3385 4137 5563 7540 9339 9948
12315 12656 12929

1113 1394 4104 4186 7240 8827 11522 11833 12359 12363
12629 12821 12904 12946

14 441 1432 1677 2432 8981 11478 11507 12599 12783
12793 12912 12922 12943

1579 1806 7971 8586 9845 10357 11600 12007 12020 12339
12576 12817 12830 12904

20 546 3672 5538 6944 8052 8781 9743 12269 12393 12418
12549 12555 12718

1 3540 4397 5011 6626 8617 9587 10360 10602 11402 11983
12068 12495 12838

30 1572 4908 7421 8041 8910 8963 11005 11930 12240
12340 12467 12892 12933

33 2060 3907 4215 5545 8306 8655 8743 8806 9315 9364
10685 11954 12959

1338 2596 4876 5207 9555 10421 10929 11648 11739 12375
12416 12643 12742 12754

9469 10544 10932 11250 11426 11582 11846 12139 12202
12210 12356 12378 12873 12929

2681 3337 3616 6113 7078 8167 8624 9697 10908 11781
11855 12095 12475 12659

28 4086 5432 6555 6848 7368 8794 11483 11572 12414
12816 12894 12936 12957

5 5044 5572 9023 9192 9529 9979 10009 10855 10991 11715
12314 12610 12945

17 272 602 5681 6530 9572 9886 11061 11495 12238 12265
12483 12885 12955

22 2245 4282 4469 5007 6650 6733 10151 10401 11371
12004 12261 12805 12844

23 3270 4468 8621 9662 11240 11934 12091 12444 12691
12717 12858 12888 12917

740 1519 4923 6191 7872 8350 9293 10779 11020 11287

11630 12792 12862 12920

12 28 3584 6072 7079 8075 10477 11130 11383 11780 12341
12667 12818 12927

14 118 5283 5382 8301 9097 9413 9664 10437 10701 11124
12685 12730 12734

32 1426 3078 4325 5353 7780 9042 9928 10077 10377 10679
11191 11750 12611

1 669 3831 3980 5381 5412 6552 8453 9435 10243 11546
11821 11987 12807

232 483 919 1232 2156 2396 2990 3774 8539 8704 8819
10810 11868 12634

2381 7309 9334

348 6494 12623

4872 6257 11090

7 11970 11985

6615 12788 12855

1173 5269 12647

1944 7738 8116

17 4828 9175

2329 6034 12642

1254 2366 5013

2984 5078 5664

7423 10265 11528

1656 8526 8716

22 287 2837

18 100 3079
299 3171 12169
33 5920 11144
1286 3650 9309
2283 8809 12588
3199 8242 9081
2507 6846 8113
5211 8722 12689
1064 2592 8659
6136 6925 12958
1256 12789 12932
4274 8045 8788
1824 3209 6926
11 8899 12669
6249 6338 8730
641 9679 12831
3459 9876 11185
3226 6148 8173
9078 12126 12771
10907 11278 12731
3392 4020 12838
2814 11588 12909
6063 9214 11519
6064 6827 12683
1610 2452 6582

903 6289 8074

4592 8138 12952

2587 6271 9945

2733 11844 11893

581 4601 10020

14 5597 6049

343 3582 5931

5263 6521 12846

1394 2457 5251

11 4627 12747

2650 10366 12390

6285 11893 12062

10143 12832 12956

8448 11917 12330

4209 11693 12356

1529 2360 9086

5389 8148 10224

64 4876 12862

9483 12659 12887

3587 6767 12478

3122 5245 9044

3267 10118 11466

1347 3857 6705

9384 9576 11971

1366 8703 10758

412 4249 12863

1676 10488 11850

17 1605 2455

14 111 6045

11368 12919 12953

10588 11530 12937

4549 5143 12218

3088 4185 11674

23 2554 7823

6615 9291 9863

2229 3629 10855

3818 5509 12764

2746 11525 12914

8297 8611 12948

3606 11104 12920

5097 10412 12759

6502 7266 12072

5425 5490 10728

22 73 8462

32 12439 12657

8483 9540 10430

7275 7377 7420

5748 9726 12356

5672 6150 9156

28 3527 5857

520 7099 11335
405 6173 12865
5847 12843 12934
4289 7679 10386
2950 8021 12938
8844 11214 12955
2130 10760 12665
734 4790 12940
8 6991 12772
19 8205 11289
12 1440 9077
8670 8837 12951
3531 9166 12937
15 8901 8929
838 10114 11740
2648 9959 10934
323 7499 12877
5505 5663 11395
6627 12709 12933
364 1976 12888
8213 9124 12793
9588 10088 11108
299 890 11634
7368 7598 11602
28 4669 12585

15 27 12474
1426 3614 4205
30 2087 11147
6226 6259 12941.

[Claim 22]

The data processing apparatus according to Claim 21,
wherein

where a row of the parity check matrix initial value
table is represented by i and a parity length of the LDPC
code is represented by M ,

a $\{2+360 \times (i-1)\}$ -th column of the parity check matrix is
a column obtained by cyclically shifting a $\{1+360 \times (i-1)\}$ -th
column of the parity check matrix, in which positions of
elements of 1 are represented in the parity check matrix
initial value table, downward by q , where q is equal to
 $M/360$.

[Claim 23]

The data processing apparatus according to Claim 22,
wherein

for the $\{1+360 \times (i-1)\}$ -th column of the parity check
matrix,

an i -th row of the parity check matrix initial
value table represents a row number of an element of 1 in
the $\{1+360 \times (i-1)\}$ -th column of the parity check matrix, and

for each of the $\{2+360 \times (i-1)\}$ -th to $\{360 \times i\}$ -th columns,

which are columns other than the $\{1+360 \times (i-1)\}$ -th column of the parity check matrix,

a row number H_{w-1} of an element of 1 in a w -th column of the parity check matrix, which is a column other than the $\{1+360 \times (i-1)\}$ -th column of the parity check matrix, is represented by equation $H_{w-1} = \text{mod}\{h_{1,j} + \text{mod}\{(w-1), 360\} \times M/360, M\}$,

where $h_{1,j}$ denotes a value in the i -th row and a j -th column of the parity check matrix initial value table, and H_{w-1} denotes a row number of a j -th element of 1 in the w -th column of the parity check matrix H .

[Claim 24]

The data processing apparatus according to Claim 22, wherein q is 36.

[Claim 25]

The data processing apparatus according to Claim 21, further comprising:

a column twist deinterleaving unit configured to perform column twist deinterleaving on the LDPC code to restore code bits of the LDPC code to an original order in a case where column twist interleaving has been performed on the LDPC code by shifting the code bits the LDPC code in a column direction and storing the shifted code bits.

[Claim 26]

The data processing apparatus according to Claim 21,

further comprising:

an inverse permutation unit configured to perform inverse permutation processing on the LDPC code, in a case where permutation processing has been performed on the LDPC code to replace code bits of the LDPC code with symbol bits of a symbol corresponding to one of a certain number of constellation points defined by a certain digital modulation scheme, to restore the code bits whose positions have been replaced with the symbol bits to original positions.

[Claim 27]

The data processing apparatus according to Claim 26, wherein

the inverse permutation unit performs inverse permutation processing to restore the code bits that are stored in a row direction and that are read in a column direction to original positions.

[Claim 28]

The data processing apparatus according to Claim 21, wherein

the parity check matrix is a parity check matrix that does not have cycle 4.

[Claim 29]

The data processing apparatus according to Claim 21, wherein

the parity check matrix is a parity check matrix of an

LDPC code belonging to an ensemble of LDPC codes having a performance threshold less than or equal to a certain value, the performance threshold being an E_b/N_0 at which a BER begins to drop and being detected using multi-edge type density evolution.

[Claim 30]

A data processing method comprising:

a decoding step of decoding an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 24/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,
the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

1504 2103 2621 2840 3869 4894 5246 6314 7327 7364 10425
11934 12893 12954

27 1903 3923 4513 7812 8068 8428 9789 10519 11345 12032
12157 12573 12930

17 19, 660 2451 2475 2376 3398 3616 5769 6724 8641

10046 11552 12842

13 1366 4993 6468 7689 8563 9131 10012 10914 11574

11837 12203 12715 12946

432 872 2603 3286 3306 3385 4137 5563 7540 9339 9948

12315 12656 12929

1113 1394 4104 4186 7240 8827 11522 11833 12359 12363

12629 12821 12904 12946

14 441 1432 1677 2432 8981 11478 11507 12599 12783

12793 12912 12922 12943

1579 1806 7971 8586 9845 10357 11600 12007 12020 12339

12576 12817 12830 12904

20 546 3672 5538 6944 8052 8781 9743 12269 12393 12418

12549 12555 12718

1 3540 4397 5011 6626 8617 9587 10360 10602 11402 11983

12068 12495 12838

30 1572 4908 7421 8041 8910 8963 11005 11930 12240

12340 12467 12892 12933

33 2060 3907 4215 5545 8306 8655 8743 8806 9315 9364

10685 11954 12959

1338 2596 4876 5207 9555 10421 10929 11648 11739 12375

12416 12643 12742 12754

9469 10544 10932 11250 11426 11582 11846 12139 12202

12210 12356 12378 12873 12929

2681 3337 3616 6113 7078 8167 8624 9697 10902 11781

11855 12095 12475 12659

28 4086 5432 6555 6848 7368 8794 11483 11572 12414
12816 12894 12936 12957
5 5044 5572 9023 9192 9589 9979 10009 10855 10991 11715
12314 12610 12945
17 272 602 5681 6530 9572 9886 11061 11495 12238 12265
12483 12885 12955
22 2245 4282 4469 5007 6650 6733 10151 10401 11571
12004 12261 12805 12844
23 3270 4468 8621 9662 11240 11934 12091 12444 12691
12717 12858 12888 12917
740 1519 4923 6191 7878 8350 9293 10779 11020 11287
11530 12792 12862 12920
12 28 3584 6072 7073 8075 10477 11130 11383 11780 12341
12667 12818 12927
14 113 5283 5382 8301 9097 9413 9664 10437 10701 11124
12685 12730 12734
32 1426 3078 4325 5353 7780 9042 9928 10077 10377 10679
11191 11750 12611
1 669 3831 3980 5381 5412 6552 8453 9435 10243 11546
11821 11987 12807
232 483 919 1232 2156 2396 2990 3774 8539 8704 8819
10810 11868 12634
2381 7309 9334
348 6494 12623
4872 6257 11990

7 11970 11985
6615 12788 12855
1173 5269 12647
1944 7738 8116
17 4828 9175
2329 6034 12642
1254 2366 5013
2984 5078 5664
7423 10265 11528
1656 8526 8716
22 287 2837
18 100 3079
299 3171 12169
33 5920 11144
1286 3650 9309
2283 8809 12588
3199 8242 9081
2507 6846 8113
5211 8722 12689
1064 2592 8659
6136 6925 12958
1256 12789 12932
4274 6045 8788
1824 3209 6926
11 8899 12669

6249 6338 8730

641 9679 12831

3459 9876 11185

3226 6148 8173

9078 12126 12771

10907 11278 12731

3392 4020 12838

2814 11588 12909

6063 9214 11519

6064 6827 12683

1610 2452 6582

903 6289 8074

4592 8138 12952

2587 6271 9945

2733 11844 11893

581 4601 10020

14 5597 6049

343 3582 5931

5263 6521 12846

1394 2457 5251

11 4627 12747

2650 10366 12390

6285 11893 12062

10143 12892 12956

8448 11917 12330

4209 11693 12356

1529 2360 9086

5389 8148 10224

64 4876 12862

9483 12659 12887

3587 6767 12478

3122 5245 9044

3267 10118 11466

1347 3857 6705

9384 9576 11971

1366 8708 10758

412 4249 12863

1676 10488 11850

17 1605 2455

14 111 6045

11368 12919 12953

10588 11530 12937

4549 5143 12218

3088 4186 11674

23 2554 7823

6615 9291 9863

2223 3623 10855

3818 5509 12764

2740 11525 12914

8297 8611 12948

3606 11104 12920

5097 10412 12759

6502 7266 12072

5425 5490 10728

22 73 8462

32 12439 12657

8483 9540 10430

7275 7377 7420

5748 9726 12356

5672 6150 9156

28 3527 3857

520 7099 11355

405 6173 12865

5847 12843 12934

4289 7679 10386

2950 8021 12938

8344 11214 12955

2130 10760 12665

734 4790 12940

8 6991 12772

19 8205 11289

12 1440 9077

8679 8837 12951

3531 9166 12937

15 8901 8929

838 10114 11740
2648 9959 10934
323 7499 12877
5505 5659 11395
6627 12709 12933
364 1976 12888
8213 9124 12793
9588 10088 11108
299 890 11634
7368 7598 11602
28 4669 12585
15 27 12474
1426 3614 4205
30 2087 11147
6226 6259 12941.

[Claim 31]

The data processing method according to Claim 30,
wherein

where a row of the parity check matrix initial value
table is represented by i and a parity length of the LDPC
code is represented by M ,

a $\{2+360 \times (i-1)\}$ -th column of the parity check matrix is
a column obtained by cyclically shifting a $\{1+360 \times (i-1)\}$ -th
column of the parity check matrix, in which positions of
elements of 1 are represented in the parity check matrix

initial value table, downward by q , where q is equal to $M/360$.

[Claim 32]

The data processing method according to Claim 31, wherein

for the $\{1+360 \times (i-1)\}$ -th column of the parity check matrix,

an i -th row of the parity check matrix initial value table represents a row number of an element of 1 in the $\{1+360 \times (i-1)\}$ -th column of the parity check matrix, and

for each of the $\{2+360 \times (i-1)\}$ -th to $\{360 \times i\}$ -th columns, which are columns other than the $\{1+360 \times (i-1)\}$ -th column of the parity check matrix,

a row number $H_{w,i}$ of an element of 1 in a w -th column of the parity check matrix, which is a column other than the $\{1+360 \times (i-1)\}$ -th column of the parity check matrix, is represented by equation $H_{w,i} = \text{mod}\{h_{1,j} + \text{mod}\{(w-1), 360\} \times M/360, M\}$,

where $h_{1,j}$ denotes a value in the 1-th row and a j -th column of the parity check matrix initial value table, and $H_{w,i}$ denotes a row number of a j -th element of 1 in the w -th column of the parity check matrix H .

[Claim 33]

The data processing method according to Claim 31, wherein q is 36.

[Claim 34]

The data processing method according to Claim 30,
further comprising:

performing column twist deinterleaving on the LDPC code
to restore code bits of the LDPC code to an original order
in a case where column twist interleaving has been performed
on the LDPC code by shifting the code bits the LDPC code in
a column direction and storing the shifted code bits.

[Claim 35]

The data processing method according to Claim 30,
further comprising:

performing inverse permutation processing on the LDPC
code, in a case where permutation processing has been
performed on the LDPC code to replace code bits of the LDPC
code with symbol bits of a symbol corresponding to one of a
certain number of constellation points defined by a certain
digital modulation scheme, to restore the code bits whose
positions have been replaced with the symbol bits to
original positions.

[Claim 36]

The data processing method according to Claim 35,
wherein

the inverse permutation processing includes restoring
the code bits that are stored in a row direction and that
are read in a column direction to original positions.

[Claim 37]

The data processing method according to Claim 30,
wherein

the parity check matrix is a parity check matrix that
does not have cycle 4.

[Claim 38]

The data processing method according to Claim 30,
wherein

the parity check matrix is a parity check matrix of an
LDPC code belonging to an ensemble of LDPC codes having a
performance threshold less than or equal to a certain value,
the performance threshold being an E_b/N_0 at which a BER
begins to drop and being detected using multi-edge type
Density evolution.

[Claim 39]

A data processing apparatus comprising:

an encoding unit configured to encode information bits
into an LDPC (Low Density Parity Check) code having a code
length of 64800 bits and a code rate of 25/30 on the basis
of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix
portion corresponding to the information bits and a parity
matrix portion corresponding to the parity bits,

the information matrix portion is represented by a

parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

1860 2354 3967 4292 4488 5243 5373 5766 8378 9111 10468
10505 10774

24 2266 2380 3282 4255 4779 8729 9140 9566 10102 10661
10711 10797

605 650 1198 1669 2251 3133 5847 6197 6902 7545 10521
10600 10773

1016 1428 1612 2335 3102 3810 4926 5953 9964 10246
10569 10734 10784

3195 6308 8029 9030 9397 9461 9833 10239 10499 10675
10736 10757 10773

2 27 3641 4566 7332 9318 9323 9916 10365 10438 10561
10581 10750

2405 2458 4820 6232 6254 6347 7139 7474 8623 8779 8798
10747 10794

3164 4736 6474 7162 7420 7517 7835 8238 8432 8489 9006
10113 10440

20 2372 5561 5649 6907 8393 8505 9181 9567 9595 10398
10483 10714

1071 2899 5135 5780 6616 7111 7773 8582 9015 9912 10139
10387 10768

292 2833 5490 6031 6136 6713 7517 9096 10128 10328

10407 10525 10736

1044 3711 4421 5140 5207 8118 8749 8884 9205 10359

10372 10746 10784

3241 5696 6440 7240 7419 8613 8878 9593 9959 9997 10401

10404 10754

3133 4647 5912 6065 6694 7208 7346 8227 9465 9739 10452

10516 10770

2254 6444 7449 8095 8120 8710 9030 9162 9643 9968 10101

10571 10678

918 1445 2217 4262 4623 5401 5749 7446 7907 9539 10125

10514 10726

6 1341 1788 3105 4359 5263 5470 7552 8249 8644 10609

10674 10733

1994 3000 3151 3173 7742 8335 8438 8741 9232 9296 9817

10023 10257

467 1674 3016 3950 4055 5399 6688 7113 7273 8658 8702

9642 10543

2007 2541 3125 7380 7550 8122 8501 8665 9882 10403

10519 10594 10696

334 587 709 1540 2023 2876 6216 8768 9328 9481 10424

10507 10779

2165 4195 4306 5019 6961 7386 8447 9082 9837 10091

10461 10559 10570

7 903 2948 6312 6654 7738 7980 8312 9104 9743 10070

10278 10406

3047 3154 4160 4378 5461 8711 8809 9040 9173 9252 9537
9995 10735
2018 2355 3828 3854 6201 6696 8313 8459 8550 8833 9586
10202 10224
1402 1908 4286 4660 6029 6115 6737 7538 9495 9517 10055
10509 10644
3442 3589 3868 5051 5322 5580 8725 9046 9170 10041
10613 10681 10689
2733 7826 10622
3597 4753 7086
1394 7297 10264
2848 7502 10304
1649 2405 10793
647 2911 9069
2572 4006 7508
1361 8887 10103
3681 4023 9090
1496 4962 6325
2016 5120 9747
3954 5260 8568
3364 8719 10035
4208 4806 9973
29 3361 3490
1835 2317 10436
7312 8177 9041

7728 8097 10761

2109 7902 9685

5424 8943 9436

4369 7643 9152

2240 10140 10528

3435 6124 10604

8962 9357 10040

26 1931 8629

8275 10455 10643

8 24 4952

3995 6456 10633

28 10300 10337

4894 9286 9429

5587 6721 9120

1859 9198 9762

6374 6453 7011

1319 4530 5442

1507 10711 10798

2115 3445 3641

6668 9139 10163

4038 8117 10295

1479 3403 8247

2522 2934 3562

1526 5073 9650

2136 9820 10636

4214 8464 9891
8018 10330 10610
8984 10209 10647
3414 7272 8599
4883 9077 9525
22 8173 8425
2941 6536 10126
29 6540 7361
5 3787 10468
4264 4818 6906
3903 7041 10412
6078 7661 10619
6922 9723 9890
5112 5416 6253
5925 9961 10447
9 10311 10598
8790 8814 10793
4768 5466 10664
10 10675 10766
6814 8705 10737
17 769 6692
1503 10696 10742
1285 4632 8976
4279 4973 7907
4650 4775 10785

28 729 10331

1914 5240 10723

3569 4921 9561

4 9442 10796

494 2328 9507

1717 8768 10750

9540 10599 10774

11 10075 10644

10246 10607 10753

5510 7088 9053

1347 3584 5523

7872 10596 10736

628 10592 10695

5632 5688 10627

2375 10009 10561

4169 4630 8871

2896 10038 10521

89 9695 9799

20 7563 9069

4534 10321 10697

8212 9868 10716

7485 9312 10327

234 536 6233

5515 7550 9251

283 3182 7167

2444 5378 6130
6183 8315 10726
43 4871 8347
2427 10219 10728
10 21 9448
1067 8312 8420
4793 9522 10105
4688 10536 10724
3825 7496 10709
682 8544 10449
2794 7110 10741
9279 10741 10767
2897 5442 8771
33 7957 10460
5 10393 10792
6225 10224 10798
23 9014 10786
7836 8339 8642
3476 5455 9788
1939 10251 10384
4008 7890 10450
926 2090 3804
1038 2497 10701
22 6220 8405
5153 5944 10367

7260 7726 9529
3039 8397 10665
7262 9644 10083
5531 6248 10795
7926 8248 8413
4649 8971 10182.

[Claim 40]

A data processing method comprising:

an encoding step of encoding information bits into an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 25/36 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

1860 2354 3967 4292 4488 5243 5373 5766 8378 9111 10468
10595 10774
24 2266 2380 3282 4255 4779 8729 9140 9566 10102 10661
10711 10797

605 650 1108 1669 2251 3133 5847 6197 6902 7545 10521
10500 10773
1016 1428 1612 2335 3102 3810 4926 5953 9964 10246
10569 10734 10784
3195 6308 8029 9030 9397 9461 9833 10239 10499 10675
10736 10757 10773
2 27 3641 4566 7332 9318 9323 9916 10365 10438 10561
10581 10750
2405 2458 4820 6232 6254 6347 7139 7474 8623 8779 8798
10747 10794
3164 4736 6474 7162 7420 7517 7835 8238 8412 8489 9006
10113 10440
20 2372 5561 5649 6907 8393 8505 9181 9567 9593 10388
10483 10714
1071 2899 5135 5780 6616 7111 7773 8582 9015 9912 10139
10387 10768
292 2833 5490 6011 6136 6713 7517 9096 10128 10328
10407 10525 10736
1044 3711 4421 5140 5207 8118 8749 8884 9203 10359
10372 10746 10784
3241 5696 6440 7240 7419 8613 8878 9593 9959 9997 10401
10404 10754
3133 4647 5912 6065 6694 7209 7346 8227 9465 9739 10452
10516 10770
2254 6444 7449 8095 8120 8710 9030 9162 9643 9968 10101

10571 10678

918 1445 2217 4262 4623 5401 5749 7446 7907 9539 10125

10514 10726

6 1341 1788 3105 4359 5263 5470 7552 8249 8644 10609

10674 10733

1994 3000 3151 3173 7742 8335 8438 8741 9232 9296 9817

10023 10257

467 1674 3016 3950 4055 5399 6688 7113 7273 8658 8702

9642 10545

2907 2541 3125 7380 7550 8122 8501 8665 9882 10403

10519 10594 10696

334 587 709 1540 2023 2876 6216 8768 9328 9481 10424

10507 10779

2165 4185 4306 5019 6961 7366 8447 9082 9837 10091

10461 10559 10570

7 903 2948 6312 6654 7738 7980 8312 9104 9743 10070

10278 10406

3047 3154 4160 4378 5461 8711 8809 9040 9173 9252 9537

9995 10735

2018 2355 3828 3854 6201 6696 8313 8459 8550 8833 9586

10202 10224

1402 1908 4286 4660 6029 6115 6737 7538 9495 9517 10055

10509 10644

3442 3589 3668 3051 5322 5580 8725 9046 9170 10041

10613 10681 10689

2733 7826 10622
3597 4753 7086
1394 7297 10264
2848 7502 10304
1649 2405 10783
647 2911 9069
2572 4006 7508
1361 8887 10103
3681 4023 9090
1496 4962 6325
2016 5120 9747
3954 5260 8568
3364 8719 10035
4208 4306 9973
29 3361 3490
1835 2317 10436
7312 8177 9041
7728 8097 10761
2109 7992 9685
5424 8943 9436
4369 7643 9152
2240 10140 10528
3435 6124 10604
8962 9357 10040
26 1931 8629

8275 10455 10643

8 24 4952

3995 6456 10633

28 10300 10337

4894 9286 9429

5587 6721 9120

1859 9198 9762

6374 6453 7011

1319 4530 5442

1507 10711 10798

2115 3445 3641

6668 9139 10163

4038 8117 10295

1479 3403 8247

2522 2934 3562

1526 5073 9650

2136 9820 10636

4214 8464 9891

8018 10330 10610

8984 10209 10647

3414 7272 8599

4883 9077 9525

22 8173 8425

2941 6536 10126

29 6540 7361

5 3787 10468

4264 4818 6906

3903 7041 10412

6078 7661 10619

6922 9723 9890

5112 5416 6253

5925 9961 10447

9 10311 10598

8790 8814 10793

4768 5466 10664

10 10675 10766

6814 8705 10727

17 769 6692

1503 10696 10742

1285 4632 8976

4279 4973 7907

4650 4775 10785

28 729 10331

1914 5240 10723

3569 4921 9561

4 9442 10796

494 2328 9507

1717 8768 10750

9540 10599 10774

11 10675 10644

10246 10607 10753

5510 7088 9053

1347 3584 5523

7872 10596 10736

628 10592 10695

5632 5688 10627

2375 10009 10561

4169 4630 8871

2896 10038 10521

89 9695 9799

20 7563 9069

4534 10321 10697

9212 9868 10716

7485 9312 10327

234 536 6293

5515 7350 9251

283 3182 7167

2444 5378 6130

6183 8315 10726

43 4871 8347

2427 10219 10728

19 21 9448

1067 8312 8420

4793 9522 10105

4088 10536 10724

3825 7496 10709
682 9544 10449
2794 7110 10741
9279 10741 10767
2897 5442 8771
33 7957 10460
5 10393 10792
6225 10224 10798
23 9014 10786
7836 8339 8642
3476 5455 9788
1939 10251 10384
4008 7890 10450
926 2090 2804
1038 2497 10701
22 6220 8405
5153 5944 10367
7260 7726 9529
3039 8397 10665
7262 9644 10083
5531 6248 10795
7926 8248 8413
4649 8971 10182.

[Claim 41]

A data processing apparatus comprising:

a decoding unit configured to decode an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 25/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 260 columns, including

1860 2354 3967 4292 4488 5242 5373 5766 8378 9111 10468
10505 10774

24 2266 2380 3282 4255 4779 8729 9140 9566 10102 10661
10711 10797

605 650 1108 1669 2251 3133 5847 6197 6902 7545 10521
10609 10773

1016 1428 1612 2335 3102 3810 4926 5953 9964 10246
10569 10734 10781

3195 6308 8029 9030 9337 9461 9833 10239 10499 10615
10736 10757 10773

2 27 3641 4556 7332 9318 9223 9916 10365 10438 10561
10581 10750

2405 2458 4820 6232 6254 6347 7139 7474 8623 8779 8798
10747 10794

3164 4735 6474 7162 7420 7517 7835 8233 8412 8489 9006
10113 10440

20 2372 5561 5649 6907 8393 8505 9181 9567 9595 10388
10483 10714

1071 2899 5135 5780 6616 7111 7773 8582 9015 9912 10139
10387 10768

292 2833 5490 6011 6136 6713 7517 9096 10128 10328
10407 10525 10736

1044 3711 4421 5140 5207 8118 8749 8884 9205 10359
10372 10746 10784

3241 5696 6440 7240 7419 8613 8878 9593 9959 9997 10401
10404 10754

3133 4647 5912 6065 6694 7208 7346 8227 9465 9739 10452
10516 10770

2254 6444 7449 8095 8120 8710 9030 9162 9643 9968 10101
10571 10678

918 1445 2217 4262 4623 5401 5749 7446 7907 9539 10125
10514 10726

6 1341 1788 3105 4359 5263 5470 7552 8249 8644 10609
10674 10733

1994 3000 3151 3173 7742 8335 8438 8741 9232 9296 9817
10023 10257

467 1674 3016 3950 4055 5399 6696 7113 7273 9656 9702

9642 10545

2007 2541 3125 7380 7550 8122 8501 8665 9882 10403

10519 10594 10696

334 587 709 1540 2023 2876 6216 8768 9328 9481 10424

10507 10779

2165 4185 4306 5019 6961 7386 8447 9082 9837 10091

10461 10559 10570

7 903 2948 6312 6654 7738 7980 8312 9104 9743 10070

10278 10406

3047 3154 4160 4378 5467 8711 8809 9040 9173 9252 9537

9995 10735

2018 2355 3828 3854 6201 6696 8313 8459 8550 8833 9586

10202 10224

1402 1908 4286 4660 6029 6115 6737 7538 9495 9517 10055

10509 10644

3442 3589 3868 5051 5322 5580 8725 9046 9170 10041

10613 10681 10689

2733 7826 10622

3597 4753 7086

1394 7297 10264

2848 7502 10304

1649 2405 10783

647 2911 9069

2572 4006 7508

1361 8887 10103

3681 4023 9090

1496 4962 6325

2016 5120 9747

3954 5260 8568

3364 8719 10035

4208 4806 9973

29 3361 3490

1835 2317 10436

7312 8177 9041

7728 8097 10761

2109 7902 9685

5424 8943 9436

4369 7643 9152

2240 10140 10528

3435 6124 10604

8962 9357 10040

26 1931 8629

8275 10455 10643

8 24 4952

3995 6456 10633

28 10300 10337

4894 9286 9429

9587 6721 9120

1859 9198 9762

6374 6452 7011

1319 4530 5442
1507 10711 10798
2115 3445 3641
6668 9139 10163
4038 8117 10295
1479 3403 8247
2522 2934 3562
1526 5073 9650
2136 9820 10636
4214 8464 9891
8018 10330 10610
8984 10209 10647
3414 7272 8599
4883 9077 9525
22 8173 8425
2941 6536 10126
29 6540 7361
5 3787 10468
4264 4818 6906
3903 7041 10412
6078 7661 10619
6922 9723 9890
5112 5416 6253
5925 9961 10447
9 10311 10598

8790 9814 10793

4768 5466 10664

10 10675 10766

6814 8705 10737

17 769 6692

1503 10696 10742

1285 4632 8976

4279 4973 7907

4650 4775 10785

28 729 10331

1914 5240 10723

3569 4921 9561

4 9442 10796

494 2328 9507

1717 8768 10750

9540 10599 10774

11 10975 10644

10246 10607 10753

5510 7688 9053

1347 3584 5523

7872 10596 10736

628 10592 10695

5632 5688 10627

2375 10009 10561

4169 4630 8871

2896 10038 10521

89 9695 9799

20 7563 9069

4534 10321 10697

8212 9868 10716

7485 9312 10327

234 536 6293

5515 7350 9251

283 3182 7167

2444 5378 6130

6183 8315 10726

43 4871 8347

. 2427 10219 10728

10 21 9448

1067 8312 8420

4793 9522 10105

4688 10536 10724

3825 7496 10709

682 8544 10449

2794 7110 10741

9279 10741 10767

2897 5442 8771

33 7957 10460

5 10393 10792

6225 10224 10798

23 9014 10786
7836 8339 8642
3476 5455 9788
1939 10251 10384
4008 7890 10450
926 2090 3804
1038 2497 10701
22 6220 8405
5153 5944 10367
7260 7726 9529
3039 8397 10665
7262 9644 10083
5531 6248 10795
7926 8248 8413
4649 8971 10182.

[Claim 42]

A data processing method comprising:

a decoding step of decoding an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 25/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a
parity check matrix initial value table, and

the parity check matrix initial value table is a table
showing positions of elements of 1 in the information matrix
portion in units of 360 columns, including

1860 2354 3967 4292 4488 5243 5373 5766 8378 9111 10468
10505 10774

24 2266 2380 3282 4255 4779 8729 9140 9566 10102 10661
10711 10797

605 650 1108 1669 2251 3133 5847 6197 6902 7545 10521
10600 10773

1016 1428 1612 2335 3102 3810 4926 5953 9964 10246
10569 10734 10784

3195 6308 8029 9030 9397 9461 9833 10239 10499 10675
10736 10757 10773

2 27 3641 4566 7332 9318 9323 9916 10365 10438 10561
10581 10750

2405 2458 4920 6232 6254 6347 7139 7474 8623 8779 8798
10747 10794

3164 4736 6474 7162 7420 7517 7935 8238 8412 8489 9006
10113 10440

20 2372 5561 5649 6907 8393 8505 9181 9567 9595 10388
10483 10714

1071 2899 5135 5780 6616 7111 7773 8582 9015 9912 10139
10387 10768

292 2833 5490 6011 6136 6713 7517 9096 10128 10328
10407 10525 10736
1044 3711 4421 5140 5207 8118 8749 8884 9205 10359
10372 10746 10784
3241 5696 6440 7240 7419 8613 8878 9593 9959 9997 10401
10404 10754
3133 4647 5912 6665 6694 7208 7346 8227 9465 9739 10452
10516 10770
2254 6444 7449 8095 8120 8710 9030 9162 9643 9968 10101
10571 10678
918 1445 2217 4262 4623 5401 5749 7446 7907 9539 10125
10514 10726
6 1341 1788 3105 4359 5263 5470 7552 8249 8644 10609
10674 10733
1994 3000 3151 3173 7742 8335 8438 8741 9232 9296 9817
10023 10257
467 1674 3016 3950 4055 5399 6688 7113 7273 8658 8702
9642 10545
2007 2541 3125 7380 7550 8122 8501 8665 9882 10403
10519 10594 10696
334 587 709 1540 2023 2876 6216 8768 9328 9481 10424
10507 10779
2165 4185 4306 5019 6961 7386 8447 9082 9837 10091
10461 10559 10570
7 903 2948 6512 6654 7738 7980 8312 9104 9743 10070

10278 10406

3047 3154 4160 4378 5461 8711 8809 9040 9173 9252 9537

9995 10735

2018 2355 3828 3854 6201 6696 8313 8459 8550 8833 9586

10202 10224

1402 1908 4286 4660 6029 6115 6737 7538 9495 9517 10055

10509 10644

3442 3589 3868 5051 5322 5580 8725 9046 9170 10041

10613 10681 10689

2733 7826 10622

3597 4753 7086

1394 7297 10264

2848 7502 10304

1649 2405 10783

647 2911 9069

2572 4006 7508

1361 8887 10103

3681 4023 9090

1496 4962 6325

2016 5120 9747

3954 5260 8568

3364 8719 10035

4208 4806 9973

29 3361 3490

1835 2217 10436

7312 8177 9041

7728 8097 10761

2109 7902 9685

5424 8943 9436

4369 7643 9152

2240 10140 10528

3435 6124 10604

8962 9357 10040

26 1931 8629

8275 10455 10643

8 24 4952

3995 6456 10633

28 10300 10337

4894 9286 9429

5587 6721 9120

1859 9198 9762

6374 6453 7011

1319 4530 5442

1507 10711 10798

2115 3445 3641

6668 9139 10163

4038 8117 10295

1479 3403 8247

2522 2934 3562

1526 5073 9653

2136 9820 10636
4214 8464 9891
8018 10330 10610
8984 10209 10647
3414 7272 8599
4883 9077 9525
22 8173 8425
2941 6536 10126
29 6540 7361
5 3787 10468
4264 4818 6906
3903 7041 10412
6078 7661 10619
6922 9723 9890
5112 5416 6253
5925 9961 10447
9 10311 10598
3790 8814 10793
4768 5466 10664
10 10675 10766
6814 8705 10737
17 769 6692
1503 10696 10742
1285 4632 8976
4279 4973 7907

4650 4775 10785

28 729 10331

1914 5240 10723

3569 4921 9561

4 9442 10796

494 2328 9507

1717 8768 10750

9540 10599 10774

11 10075 10644

10246 10607 10753

5510 7088 9053

1347 3584 5523

7872 10596 10736

628 10592 10695

5632 5689 10627

2375 10009 10561

4169 4630 8871

2896 10038 10521

39 9695 9799

20 7563 9069

4534 10321 10697

8212 9868 10716

7485 9312 10327

224 536 6293

5415 7359 9251

283 3182 7167
2444 5378 6130
6183 8315 10726
43 4871 8347
2427 10219 10728
10 21 9448
1067 8312 8420
4793 9522 10105
4688 10536 10724
3825 7496 10709
682 8544 10449
2794 7110 10741
9279 10741 10767
2897 5442 8771
33 7957 10460
5 10393 10792
6225 10224 10798
23 9014 10786
7836 8339 8642
3476 5435 9788
1939 10251 10384
4008 7890 10450
926 2090 3804
1038 2497 10701
22 6220 8405

5153 5944 10367
7260 7726 9529
3039 8397 10665
7262 9644 10083
5531 6248 10795
7926 8248 8413
4649 8971 10182.

[Claim 43]

A data processing apparatus comprising:

an encoding unit configured to encode information bits into an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 26/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

142 2307 2598 2650 4028 4434 5781 5881 6016 6323 6681
6698 8125
2932 4923 5248 5256 5983 6773 6828 7739 8426 8494 8534

8539 8583

899 3295 3833 5399 6820 7400 7753 7890 8109 8451 8529

8564 8602

21 3060 4720 5429 5636 5927 6966 8110 8170 8247 8355

8365 8616

20 1745 2838 3799 4380 4418 4646 5059 7343 8161 8302

8456 8631

9 6274 6725 6792 7195 7333 8027 8186 8209 8273 8442

8548 8632

494 1365 2405 3799 5188 5291 7644 7926 8139 8458 9504

8594 8625

192 574 1179 4387 4695 5089 5931 7673 7789 8298 8301

8612 8632

11 20 1406 6111 6176 6256 6708 6834 7828 8232 8457 8495

8602

6 2654 3554 4483 4966 5866 6795 8069 8249 8301 8497

8509 8623

21 1144 2355 3124 6773 6905 6887 7742 7994 8358 8374

8580 8611

335 4473 4883 5528 6096 7543 7586 7921 8197 8319 8394

8484 8636

2919 4331 4419 4735 6366 6393 6844 7193 8165 8205 9544

8586 8617

12 19 742 930 3009 4330 6213 6224 7292 7430 7792 7922

8137

710 1439 1588 2434 3516 5239 6248 6827 8230 8448 8515
8581 8619
200 1075 1868 5581 7349 7642 7698 8037 8201 8210 8320
8391 8526
3 2501 4252 5256 5292 5567 6136 6321 6430 6486 7571
8521 8636
3062 4599 5885 6529 6616 7314 7319 7567 8024 8153 8302
8372 8598
105 381 1574 4351 5452 5603 5943 7467 7788 7933 8362
8513 8587
787 1857 3386 3659 6550 7131 7365 8015 8040 8312 8484
8525 8537
15 1118 4226 5197 5575 5761 6762 7038 8260 8338 8444
8512 8568
36 5216 5368 5616 6029 6591 8038 8067 8299 8351 8565
8578 8585
1 23 4300 4530 5426 5532 5817 6967 7124 7979 8022 8270
8437
629 2133 4828 5475 5875 5890 7194 8042 8345 8385 8518
8598 8612
11 1065 3782 4237 4993 7104 7863 7904 8104 8228 8321
8383 8565
2131 2274 3168 3215 3220 5597 6347 7812 8238 8354 8527
8557 8614
5600 6591 7491 7696

1766 8281 8626

1725 2280 5120

1650 3445 7652

4312 6911 8626

15 1013 5892

2263 2546 2979

1545 5873 7406

67 726 3697

2860 6443 8542

17 911 2820

1561 4580 6052

79 5269 7134

22 2410 2424

3501 5642 8627

808 6950 8571

4099 6389 7482

4023 5000 7833

5476 5765 7917

1008 3194 7207

20 495 5411

1703 8388 8635

6 4395 4921

200 2053 8206

1089 5126 5562

10 4193 7720

1967 2151 4608

22 738 3513

3385 5066 8152

440 1118 8537

3429 6058 7716

5213 7519 8382

5564 8365 8620

43 3219 8603

4 5409 5815

5 6376 7654

4091 5724 5953

5348 6754 8613

1634 6398 6632

72 2058 8605

3497 5811 7579

3846 6743 8559

15 5933 8629

2133 5859 7068

4131 4617 8566

2960 8270 8410

2059 3617 8210

544 1441 6895

4043 7482 8592

294 2180 8524

2058 3227 8373

364 5756 8617
5383 8555 8619
1704 2480 4181
7338 7929 1990
2615 3905 7981
4298 4548 8296
8262 8319 8630
892 1893 8028
5694 7237 8595
1487 5012 5810
4335 8593 8624
3509 4531 5273
10 22 830
4161 5208 6280
275 7063 8634
4 2725 3113
2279 7403 8174
1637 3328 3930
2810 4939 5624
3 1234 7687
2799 7740 8616
22 7701 8636
4302 7857 7993
7477 7794 8592
9 6111 8591

5 8605 8628
347 3497 4033
1747 2613 8636
1827 5600 7042
580 1822 6842
232 7134 7783
4629 5000 7231
951 2806 4947
571 3474 8577
2437 2496 7945
23 5873 8162
12 1168 7686
8315 8540 8596
1766 2506 4733
929 1516 3338
21 1216 6555
782 1452 8617
8 6083 6087
667 3240 4583
4030 4661 5790
559 7122 8553
3202 4388 4909
2533 3673 8594
1991 3954 6206
6835 7900 7980

189 5722 8573

2680 4928 4998

243 2579 7735

4281 8132 8566

7656 7671 8609

1116 2291 4166

21 388 8021

6 1123 8369

311 4918 8511

0 3248 6290

13 6762 7172

4209 5632 7563

49 127 8074

581 1735 4075

0 2235 5479

2178 5820 6179

16 3575 6054

1095 4564 6458

9 1581 5953

2537 6469 8552

14 3874 4844

0 3269 3551

2114 7372 7926

1875 2388 4057

3232 4042 6663

9 401 583
13 4100 6584
2299 4190 4410
21 3670 4979.

[Claim 44]

A data processing method comprising:

an encoding step of encoding information bits into an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 26/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

142 2307 2598 2650 4028 4434 5781 5881 6016 6323 6681
6698 8125
2932 4928 5248 5256 5983 6773 6828 7789 8426 8494 8534
8539 8583
399 3295 3833 5399 6320 7400 7753 7890 8109 8451 8529
8564 8602

21 3060 4720 5429 5636 5927 6966 8110 8170 8247 8355
8365 8616
20 1745 2838 3799 4380 4418 4646 5059 7343 8161 8302
8456 8631
9 6274 6725 6792 7195 7333 8027 8186 8209 8273 8442
8548 8632
494 1365 2405 3799 5188 5291 7644 7926 8139 8458 8504
8594 8625
192 574 1179 4387 4695 5089 5831 7673 7789 8298 8301
8612 8632
11 20 1406 6111 6176 6256 6708 6834 7828 8232 9457 8495
8602
6 2654 3554 4483 4966 5866 6795 8069 8249 8301 8497
8509 8623
21 1144 2355 3124 5773 6805 6887 7742 7994 8358 8374
9580 8611
335 4473 4883 5528 6096 7542 7586 7921 8197 8319 8394
8489 8636
2919 4331 4419 4735 6366 6393 6844 7193 8165 8205 8544
8586
8617
12 19 742 930 3009 4330 6213 6224 7292 7430 7792 7922
8137
710 1439 1588 2434 3516 5239 6248 6827 8230 8448 8515
8581 8619

200 1075 1868 5581 7349 7642 7698 8037 8201 8210 8320
8391 8526
3 2501 4252 5256 5292 5567 6136 6321 6430 6486 7571
8521 8636
3062 4599 5885 6529 6616 7314 7319 7567 8024 8153 8302
8372 8598
105 381 1574 4351 5452 5603 5943 7467 7788 7933 8362
8513 8587
787 1857 3386 3659 6550 7131 7965 8015 8040 8312 8484
8525 8537
15 1118 4226 5197 5575 5761 6762 7038 8260 8338 8444
8512 8568
36 5216 5368 5616 6029 6591 8038 8067 8299 8351 8565
8578 8585
1 23 4300 4530 5426 5532 5817 6967 7124 7979 8022 8270
8437
629 2133 4828 5475 5875 5890 7194 8042 8345 8385 8518
8598 8612
11 1065 3782 4237 4993 7104 7863 7904 8104 8228 8321
8383 8565
2131 2274 3168 3215 3220 5597 6347 7812 8238 8354 8527
8557 8614
5600 6591 7491 7696
1766 8281 8626
1725 2280 5120

1650 3445 7652

4312 6911 8626

15 1013 5892

2263 2546 2979

1545 5873 7406

67 726 3697

2860 6443 8542

17 911 2820

1561 4580 6052

79 5269 7134

22 2410 2424

3501 5642 8627

808 6950 8571

4099 6389 7482

4023 5000 7833

5476 5765 7917

1008 3194 7207

20 495 5411

1703 8388 8635

6 4395 4921

200 2053 8206

1089 5126 5562

10 4193 7720

1967 2151 4608

22 739 3513

3385 5066 8152
440 1118 8537
3429 6058 7716
5213 7519 8382
5564 8365 8620
43 3219 8603
4 5409 5815
5 6376 7654
4091 5724 5953
5348 6754 8613
1634 6398 6632
72 2058 8605
3497 5811 7579
3846 6743 8559
15 5933 8629
2133 5859 7068
4151 4617 8566
2960 8270 8410
2059 3617 8210
544 1441 6895
4043 7482 8592
294 2180 8524
3058 8227 8373
364 5756 8617
5383 8555 8615

1704 2480 4181

7338 7929 7990

2615 3905 7981

4298 4548 8296

8262 8319 8630

892 1893 8028

5694 7237 8595

1487 5012 5810

4335 8593 8624

3509 4531 5273

10 22 830

4161 5208 6280

275 7063 8634

4 2725 3113

2279 7403 8174

1637 3328 3930

2810 4939 5624

3 1234 7687

2799 7740 8616

22 7701 8636

4302 7857 7993

7477 7794 8592

9 6111 8591

5 8606 8628

247 3497 4033

1747 2613 8636

1827 5600 7042

580 1822 6842

232 7134 7783

4629 5000 7231

951 2806 4947

571 3474 8577

2437 2496 7945

23 5873 8162

12 1168 7686

8315 8540 8596

1766 2506 4733

929 1516 3338

21 1216 6555

782 1452 8617

8 6083 6087

667 3240 4583

4030 4661 5790

559 7122 8553

3202 4388 4909

2533 3673 8594

1991 3954 6206

6835 7900 7980

189 5722 8573

2680 4928 4998

243 2579 7735
4281 8132 8566
7656 7671 8609
1116 2291 4166
21 388 8021
6 1123 8369
311 4918 8511
0 3248 6290
13 6762 7172
4209 5632 7563
49 127 8074
581 1735 4075
0 2235 5470
2178 5820 6179
16 3575 6054
1095 4564 6458
9 1581 5953
2537 6469 8552
14 3874 4844
0 3269 3551
2114 7372 7926
1875 2388 4057
3232 4042 6663
9 401 583
13 4100 6584

2299 4190 4410

21 3670 4979.

[Claim 45]

A data processing apparatus comprising:

a decoding unit configured to decode an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 26/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

142 2307 2598 2650 4028 4434 5781 5881 6016 6323 6681
6698 8125

2932 4928 5248 5256 5983 6773 6828 7789 8426 8494 8534
8539 8583

899 3295 3833 5399 6820 7400 7753 7890 8109 8451 8529
8564 8602

21 3060 4720 5429 5636 5927 6966 8110 8170 8247 8355
8365 8616

20 1745 2838 3799 4380 4418 4646 5059 7343 8161 8302
8456 8631
9 6274 6725 6792 7195 7333 8027 8186 8209 8273 8442
8548 8632
494 1365 2405 3799 5188 5291 7644 7926 8139 8458 8504
8594 8625
192 574 1179 4387 4695 5089 5831 7673 7789 8298 8301
8612 8632
11 20 1406 6111 6176 6256 6708 6834 7828 8232 8457 8495
3602
6 2654 3554 4483 4966 5866 6795 8069 8249 8301 8497
8509 8623
21 1144 2355 3124 6773 6805 6887 7742 7994 8358 8374
8580 8611
335 4473 4883 5528 6096 7543 7586 7921 8197 8319 8394
8489 8636
2919 4331 4419 4735 6366 6393 6844 7193 8165 8205 8544
8586 8617
12 19 742 930 3009 4330 6213 6224 7292 7430 7792 7922
8137
710 1439 1588 2434 3516 5239 6248 6827 8230 8448 8575
8581 8619
200 1075 1868 5581 7349 7642 7698 8037 8201 8210 8320
8391 8526
3 2501 4252 5256 5292 5567 6136 6321 6430 6486 7571

8521 8636

3062 4599 5885 6529 6616 7314 7319 7567 8024 8153 8302

8372 8598

105 381 1574 4351 5452 5603 5943 7467 7788 7933 8362

8513 8587

787 1857 3386 3659 6550 7131 7965 8015 8040 8312 8484

8525 8537

15 1118 4226 5197 5575 5761 6762 7038 8260 8338 8444

8512 8568

36 5216 5368 5616 6029 6591 8038 8067 8299 8351 8565

8578 8585

1 23 4300 4530 5426 5532 5817 6967 7124 7979 8022 8270

8437

629 2133 4828 5475 5875 5890 7194 8042 8345 8385 8518

8598 8612

11 1065 3782 4237 4993 7104 7863 7904 8104 8228 8321

8383 8565

2131 2274 3168 3215 3220 5597 6347 7812 8238 8354 8527

8557 8614

5600 6591 7491 7696

1766 8281 8626

1725 2280 5120

1650 3445 7652

4312 6911 8626

15 1015 5892

2263 2546 2979

1545 5873 7406

67 726 3697

2860 6443 8542

17 911 2820

1561 4580 6052

79 5269 7134

22 2410 2424

3501 5642 8627

808 6950 8571

4099 6389 7482

4023 5000 7833

5476 5765 7917

1008 3194 7207

20 495 5411

1703 8388 8635

6 4395 4921

200 2053 8206

1089 5126 5562

10 4193 7720

1967 2151 4608

22 738 3513

3385 5066 8152

440 1118 8537

3429 6058 7716

5213 7519 8382

5564 8365 8620

43 3219 8603

4 5409 5815

5 6376 7654

4091 5724 5953

5348 6754 8613

1634 6398 6632

72 2058 8605

3497 5811 7579

3846 6743 8559

15 5933 8629

2133 5859 7068

4151 4617 8566

2960 8270 8410

2059 3617 8210

544 1441 6895

4043 7482 8592

294 2160 8524

3058 8227 8373

364 5756 8617

5383 8555 8619

1704 2480 4181

7338 7929 7990

2615 3905 7981

4298 4548 8296

8262 8319 8630

892 1893 8028

5694 7237 8595

1487 5012 5810

4335 8593 8624

3509 4531 5273

10 22 830

4161 5208 6280

275 7063 8634

4 2725 3113

2279 7403 8174

1637 3328 3930

2810 4939 5624

3 1234 7687

2799 7740 8616

22 7701 8636

4302 7857 7993

7477 7794 8592

9 6111 8591

5 8606 8628

347 3497 4033

1747 2613 8636

1827 5600 7042

580 1822 6842

232 7134 7783
4629 5000 7231
951 2806 4947
571 3474 8577
2437 2496 7945
23 5873 8162
12 1168 7686
8315 8540 8596
1766 2506 4733
929 1516 3338
21 1216 6555
782 1452 8617
3 6083 6087
667 3240 4583
4030 4661 5790
559 7122 8553
3202 4388 4909
2533 3673 8594
1991 3954 6206
6835 7900 7980
189 5722 8573
2680 4928 4998
243 2579 7735
4281 8132 8566
7656 7671 8609

1116 2291 4166

21 388 8021

6 1123 8369

311 4918 8511

0 3248 6290

13 6762 7172

4209 5632 7563

49 127 8074

581 1735 4075

0 2235 5470

2178 5820 6179

16 3575 6054

1095 4564 6458

9 1581 5953

2537 6469 8552

14 3874 4844

0 3269 3551

2114 7372 7926

1875 2388 4057

3232 4042 6663

9 401 533

13 4100 6584

2299 4190 4410

21 3670 4979.

[Claim 46]

A data processing method comprising:

a decoding step of decoding an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 26/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

142 2307 2598 2650 4028 4434 5781 5881 6016 6323 6681
6698 8125

2932 4928 5248 5256 5983 6773 6828 7789 8426 8494 8534
8539 8583

899 3295 3833 5399 6820 7400 7753 7890 8109 8451 8529
8564 8602

21 3060 4720 5429 5636 5927 6966 8110 8170 8247 8355
8365 8616

20 1745 2838 3799 4380 4418 4646 5059 7343 8161 8302
8456 8631

9 6274 6725 6792 7195 7333 8027 8186 8209 8273 8442

8548 8632

494 1365 2405 3799 5188 5291 7644 7926 8139 8458 8504

8594 8625

192 574 1179 4387 4695 5089 5831 7673 7739 8298 8301

8612 8632

11 20 1406 6111 6176 6256 6708 6834 7828 8232 8457 8495

8602

6 2654 3554 4483 4966 5866 6795 8069 8249 8301 8497

8509 8623

21 1144 2355 3124 6773 6805 6887 7742 7994 8358 8374

8580 8611

335 4473 4883 5528 6096 7543 7586 7921 8197 8319 8394

8489 8636

2919 4331 4419 4735 6366 6393 6844 7193 8165 8205 8544

8586 8617

12 19 742 930 3009 4330 6213 6224 7292 7436 7792 7922

8137

710 1439 1588 2434 3516 5239 6248 6827 8230 8448 8515

8581 8619

200 1075 1868 5581 7349 7642 7698 8037 8201 8210 8320

8391 8526

3 2501 4252 5256 5292 5567 6136 6321 6439 6486 7371

8521 8636

3062 4599 5885 6529 6616 7314 7319 7567 8024 8153 8302

8372 8598

105 381 1574 4351 5452 5603 5943 7467 7788 7933 8362
8513 8587
787 1857 3386 3659 6550 7131 7965 8015 8040 8312 8484
8525 8537
15 1118 4226 5197 5575 5761 6762 7038 8260 8338 8444
8512 8568
36 5216 5368 5616 6029 6591 8038 8067 8299 8351 8565
8578 8585
1 23 4300 4530 5426 5532 5817 6967 7124 7979 8022 8270
8437
629 2133 4828 5475 5875 5890 7194 8042 8345 8385 8518
8598 8612
11 1065 3782 4237 4993 7104 7863 7904 8104 8228 8321
8383 8565
2131 2274 3168 3215 3220 5597 6347 7812 8238 8354 8527
8557 8614
5600 6591 7491 7696
1766 8281 8626
1725 2280 5120
1650 3445 7652
4312 6911 8626
15 1013 5892
2263 2546 2979
1545 3873 7406
67 726 3697

2860 6443 8542

17 911 2820

1561 4580 6052

79 5269 7134

22 2410 2424

3501 5642 8627

808 6950 8571

4099 6389 7482

4023 5000 7833

5476 5765 7917

1008 3194 7207

20 495 5411

1703 8388 8635

6 4395 4921

200 2053 8206

1089 5126 5562

10 4193 7720

1967 2151 4608

22 738 3513

3385 5066 8152

440 1118 8537

3429 6058 7716

5213 7519 8382

5564 8365 8620

43 3219 8603

4 5409 5815

5 6376 7654

4091 5724 5953

5348 6754 8613

1634 6398 6632

72 2058 8605

3497 5811 7579

3846 6743 8559

15 5933 8629

2133 5859 7068

4151 4617 8566

2960 8270 8410

2059 3617 8210

544 1441 6895

4043 7482 8592

294 2180 8524

3058 8227 8373

364 5756 8617

5383 8555 8619

1704 2480 4181

7338 7929 7990

2615 3905 7981

4298 4548 8296

8262 8319 8630

892 1893 8028

5694 7237 8595

1487 5012 5810

4335 8593 8624

3509 4531 5273

10 22 830

4161 5208 6280

275 7063 8634

4 2725 3113

2279 7403 8174

1637 3328 3930

2810 4939 5624

3 1234 7687

2799 7740 8616

22 7701 8636

4302 7857 7993

7477 7794 8592

9 6111 8591

5 8606 8628

347 3497 4033

1747 2613 8636

1827 5600 7042

380 1822 6842

232 7134 7783

4629 5000 7231

951 2806 4947

571 3474 8577
2437 2496 7945
23 5873 8162
12 1168 7686
8315 8540 8596
1766 2506 4733
929 1516 3338
21 1216 6555
782 1452 8617
8 6083 6087
667 3240 4583
4030 4661 5790
559 7122 8553
3202 4388 4909
2533 3673 8594
1991 3954 6206
6835 7900 7980
189 5722 8573
2680 4923 4998
243 2579 7735
4281 8132 8566
7656 7671 8609
1116 2291 4166
21 388 8021
6 1123 8369

311 4918 8511
0 3248 6290
13 6762 7172
4209 5632 7563
49 127 8074
581 1735 4075
0 2235 5470
2178 5820 6179
16 3575 6054
1095 4564 6458
9 1581 5953
2537 6469 8552
14 3874 4844
0 3269 3551
2114 7372 7926
1875 2388 4057
3232 4042 6663
9 401 583
13 4100 6584
2299 4190 4410
21 3670 4979.

[Claim 47]

A data processing apparatus comprising:
an encoding unit configured to encode information bits
into an LDPC (Low Density Parity Check) code having a code

length of 64800 bits and a code rate of 27/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

658 706 898 1149 2577 2622 2772 3266 3329 5243 6079
6277

289 784 1682 3584 3995 4821 4856 5063 5974 6168 6437
6453

658 1426 2043 2065 2986 4118 4284 5394 5444 5477 5727
6018

641 928 1225 2841 4052 4840 4992 5268 5533 6249 6461
6475

2312 2917 3713 3849 4059 4241 4610 5440 5727 6101 6397
6444

1165 1592 1891 2154 3981 4817 5181 5748 5788 6012 6266
6350

13 2758 3069 4233 4697 5100 5279 5677 5919 5969 6280
6422

818 1500 2125 2340 3774 4707 4901 5170 5744 6008 6316
6353
857 3054 3409 3496 3704 4868 5326 6211 6292 6356 6367
6381
0 7 12 1709 2166 3418 3723 4887 5770 6043 6069 6431
2481 3379 4650 4900 4919 5060 5410 5425 6056 6173 6283
6386
15 814 854 1871 2934 3387 3915 5180 5303 5442 5581 5665
146 1882 3076 4458 4848 5252 5602 5778 5821 6213 6251
6401
2 947 1419 1566 3437 3646 4615 4634 4735 5819 5943 6280
1231 2309 2920 4158 4185 4298 4711 5082 5757 5762 6204
6209
257 297 337 2783 3230 4134 4480 4749 5295 5689 5921
6202
1436 2151 2629 3217 3930 4078 5386 5799 5906 6146 6226
6366
133 530 2448 4745 5000 5020 5224 5273 6211 6266 6431
6453
13 2644 3895 3898 4485 4722 5142 5462 5951 6031 6084
6351
6 3000 3873 3995 4680 5158 5504 5692 5755 6255 6338
6359
166 465 1658 2549 2941 4244 5071 5149 5452 5874 5939
6038

2309 2937 4282 4628 5113 5454 5731 5825 6021 6171 6402
6472
3 1077 2116 2426 2830 4853 5066 5571 5850 5916 6389
6421
817 1608 2229 2925 3281 4393 5042 5058 5377 5464 5588
6448
1848 3871 4381 4776 5366 5578 5648 6143 6389 6434 6465
6473
1263 1616 3150 3497 3759 4078 5530 5665 5694 5913 6397
6420
11 813 2185 2795 3349 4652 4678 5078 5504 6011 6286
6387
3060 3161 4584 4996 5143 5542 5697 5937 6141 6155 6342
6446
1638 2333 2632 3450 3505 3911 4399 4454 5499 5860 6044
6360
550 1744 4517
5772 6071 6471
3582 3622 5776
6153 6380 6446
3977 5932 6447
2071 4597 4891
11 1428 3776
1111 3874 5048
1410 2144 4445

4681 5481 6462

4044 5037 5497

2716 2891 6411

3299 4384 6224

1843 6087 6400

4664 5009 5856

1548 4383 5055

3172 4190 6373

5899 6443 6470

2572 3647 6240

1295 2158 6466

5604 6269 6368

3 5551 6454

3325 5797 6261

666 1397 5538

3069 4274 6410

4042 5992 6437

743 3075 3447

1344 2725 6386

283 2808 6303

2 4627 4632

26 1565 4000

4012 4946 6472

1629 6158 6467

6200 6251 6376

2969 4344 4440
2317 3115 4832
2099 5263 6285
2409 5868 5997
3752 4200 6350
3125 5841 6142
1 2249 6328
16 2525 6379
3198 5269 5960
4 1705 2069
990 4948 5520
1664 3836 4521
1765 4110 6454
9 1373 6387
1969 2405 6368
623 1428 3946
3111 6380 6436
1861 5611 5934
9 2444 3081
5 5508 6317
3184 4288 5995
1060 4803 6400
5921 5825 6289
1608 4754 5648
4702 6391 6421

3899 4811 6128
927 2286 5313
4123 6181 6453
2893 4150 5261
605 4332 5094
17 3518 6358
2858 6126 6478
15 1316 6465
2 2032 2983
5249 6340 6427
5 6003 6200
4478 6315 6420
5158 6390 6447
2598 3229 5399
3747 6424 6446
1412 2453 6332
5236 5715 6455
2137 3421 4368
15 3880 5245
17 3156 5638
3227 3798 6230
2094 3129 6458
1412 5573 5932
175 1182 6304
3555 6407 6463

583 1654 6339
14 6261 6449
3553 5383 5679
2092 2744 4153
0 4466 6472
11 3840 4354
17 5457 6222
1467 6083 6220
3449 3858 6337
3782 5318 6426
417 5038 5790
3571 5638 5873
6117 6241 6476
1898 5680 6219
3235 3817 6429
2095 4194 6224
2 4092 6448
5 6330 6383
285 5075 6334
10 505 2867
1183 5956 6466
839 4716 6471
984 3254 6432
1501 4790 6465
8 1457 1707

1660 1969 6438

4349 6182 6305

1423 3848 5490

1651 2969 6345

344 4164 6298

2397 6027 6274

2233 2778 6161

13 1778 2977

9 1916 3377

0 3 6190

395 4893 6394

3512 4098 6400

3490 6281 6473

12 1359 6465

4202 5179 6412

3007 3542 4271

2400 3350 6351

7 5490 5716

4695 5231 6266

777 6292 6402

919 4851 6367

6 644 3893

5386 6190 6434

17 169 4896.

[Claim 48]

A data processing method comprising:

an encoding step of encoding information bits into an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 27/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

658 706 898 1149 2577 2622 2772 3266 3329 5243 6079

6271

289 784 1682 3584 3995 4821 4856 5063 5974 6168 6437

6453

658 1426 2043 2065 2986 4118 4284 5394 5444 5477 5727

6018

641 928 1225 2841 4052 4840 4992 5268 5533 6249 6461

6475

2312 2317 3713 3849 4056 4241 4610 5440 5727 6101 6397

6444

1165 1592 1891 2154 3381 4817 5181 5748 5788 6012 6266

6350

13 2758 3069 4233 4697 5100 5279 5677 5919 5969 6280

6422

818 1500 2125 2340 3774 4707 4901 5170 5744 6008 6316

6353

857 3054 3409 3496 3704 4868 5326 6211 6292 6356 6367

6381

0 7 12 1709 2166 3418 3723 4887 5770 6043 6069 6431

2481 3379 4650 4900 4919 5060 5410 5425 6056 6173 6283

6386

15 814 854 1871 2934 3387 3915 5180 5303 5442 5581 5665

146 1882 3076 4458 4848 5252 5602 5778 5821 6213 6251

6401

2 947 1410 1566 3437 3646 4615 4634 4735 5819 5943 6280

1231 2309 2920 4158 4185 4298 4711 5082 5757 5762 6204

6209

257 297 337 2783 3230 4134 4480 4749 5295 5689 5921

6292

1436 2151 2629 3217 3930 4078 5386 5799 5906 6146 6226

6366

133 530 2448 4745 5000 5020 5224 5273 6211 6266 6431

6453

13 2644 3895 3898 4485 4722 5142 5462 5951 6031 6084

6351

6 3000 3873 3995 4680 5158 5504 5692 5755 6255 6338

6359

166 465 1658 2549 2941 4244 5071 5149 5452 5874 5939

6038

2309 2937 4282 4628 5113 5454 5731 5825 6021 6171 6402

6472

3 1077 2116 2426 2830 4853 5066 5571 5850 5916 6389

6421

817 1608 2229 2925 3281 4393 5042 5058 5377 5464 5588

6448

1848 3871 4381 4776 5366 5578 5648 6143 6389 6434 6465

6473

1263 1616 3150 3497 3759 4078 5530 5665 5694 5913 6397

6420

11 813 2185 2795 3349 4652 4678 5078 5504 6011 6286

6387

3060 3161 4584 4996 5143 5542 5697 5937 6141 6155 6342

6445

1638 2333 2632 3450 3505 3911 4399 4454 5499 5860 6044

6360

650 1744 4517

5772 6071 6471

3582 3622 5776

6153 6380 6446

3977 5932 6447

2071 4597 4891

11 1428 3776
1111 3874 5048
1410 2144 4445
4681 5481 6462
4044 5037 5497
2716 2891 6411
3299 4384 6224
1843 6087 6400
4664 5009 5856
1548 4383 5055
3172 4190 6373
5899 6443 6470
2572 3647 6240
1295 2158 6466
5604 6269 6368
3 5551 6454
3325 5797 6261
666 1397 5538
3069 4274 6410
4042 5992 6437
743 3075 3447
1344 2725 6386
283 2808 6303
2 4627 4632
26 1565 4090

4012 4946 6472

1629 6158 6467

6300 6351 6376

2969 4344 4440

2317 3115 4032

2099 5263 6285

2409 5868 5997

3752 4200 6350

3125 5841 6142

1 2249 6328

16 2525 6379

3198 5269 5960

4 1705 2069

990 4948 5520

1664 3836 4521

1765 4110 6454

3 1373 6387

1969 2405 6368

623 1428 3946

3111 6380 6436

1861 5611 5934

9 2444 3981

5 5509 6317

3184 4988 5993

1969 4802 6400

5021 5826 6289

1608 4754 5648

4702 6391 6421

3899 4811 6128

927 2286 5313

4123 6181 6453

2893 4150 5261

605 4332 5094

17 3518 6358

2858 6126 6478

15 1316 6465

2 2032 2983

5249 6340 6427

5 6003 6200

4478 6315 6420

5158 6390 6447

2598 3229 5399

3747 6424 6446

1412 2453 6332

5256 5715 6455

2137 3421 4368

15 3880 5245

17 3156 5638

3227 3738 6230

2094 3129 6438

1412 5573 5932

175 1182 6304

3555 6407 6463

583 1654 6339

14 6261 6449

3553 5383 5679

2092 2744 4153

0 4466 6472

11 3840 4354

17 5457 6222

1467 6083 6220

3449 3858 6337

3782 5318 6426

417 5038 5790

3571 5638 5873

6117 6241 6476

1898 5680 6213

3235 3817 6429

2095 4194 6224

2 4092 6448

5 6330 6383

285 5075 6334

10 505 2867

1183 5856 6466

839 4716 6471

984 3254 6432
1501 4790 6465
8 1457 1707
1660 1969 6438
4349 6182 6305
1423 3848 5490
3651 2969 6345
344 4164 6298
2397 6027 6274
2233 2778 6161
13 1778 2977
9 1316 3377
0 3 6130
395 4893 6394
3512 4098 6400
3490 6281 6473
12 1359 6465
4202 5179 6412
3007 3542 4271
2400 3350 6351
7 5490 5716
4695 5231 6266
777 6292 6402
919 4851 6367
6 644 3891

5386 6190 6434

17 169 4896.

[Claim 49]

A data processing apparatus comprising:

a decoding unit configured to decode an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 27/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

658 706 898 1149 2577 2622 2772 3266 3329 5243 6079

6271

289 784 1682 3584 3995 4821 4856 5063 5974 6168 6437

6453

658 1426 2043 2065 2986 4118 4284 5394 5444 5477 5727

6018

641 928 1225 2841 4052 4840 4992 5268 5533 6249 6461

6475

2312 2917 3713 3849 4059 4241 4610 5440 5727 6101 6397
6444
1165 1592 1891 2154 3981 4817 5181 5748 5788 6012 6266
6350
13 2758 3069 4233 4697 5100 5279 5677 5919 5969 6280
6422
818 1500 2125 2340 3774 4707 4901 5170 5744 6008 6316
6353
857 3054 3409 3496 3704 4868 5326 6211 6292 6356 6367
6381
0 7 12 1709 2166 3418 3723 4887 5770 6043 6069 6431
2481 3379 4650 4900 4919 5060 5410 5425 6056 6173 6283
6386
15 814 854 1871 2934 3387 3915 5180 5303 5442 5581 5665
146 1882 3076 4458 4848 5252 5602 5778 5821 6213 6251
6401
2 947 1419 1566 3437 3646 4615 4634 4735 5819 5943 6280
1231 2309 2920 4158 4185 4298 4711 5082 5757 5762 6204
6209
257 297 337 2723 3230 4134 4480 4749 5295 5689 5921
6202
1436 2151 2629 3217 3930 4078 5386 5799 5906 6146 6226
6366
133 530 2448 4745 5000 5020 5224 5273 6211 6266 6431
6453

13 2644 3895 3898 4485 4722 5142 5462 5951 6031 6084
6351
6 3000 3873 3995 4680 5158 5504 5692 5755 6255 6338
6359
166 465 1658 2549 2941 4244 5071 5149 5452 5874 5939
6038
2309 2937 4282 4628 5113 5454 5731 5825 6021 6171 6402
6472
3 1077 2116 2426 2830 4853 5066 5571 5850 5916 6389
6421
817 1608 2229 2925 3281 4393 5042 5058 5377 5464 5588
6448
1848 3871 4381 4776 5366 5578 5648 6143 6389 6434 6465
6473
1263 1616 3150 3497 3759 4078 5530 5665 5694 5913 6397
6420
11 813 2185 2795 3349 4652 4678 5078 5504 6011 6286
6387
3060 3161 4584 4996 5143 5542 5697 5937 6141 6155 6342
6445
1638 2333 2632 3450 3505 3911 4399 4454 5499 5860 6044
6360
656 1744 4517
5772 6071 6471
3582 3622 5776

6153 6380 6446

3977 5932 6447

2071 4597 4891

11 1428 3776

1111 3874 5048

1410 2144 4445

4681 5481 6462

4044 5037 5497

2716 2891 6411

3299 4384 6224

1843 6087 6400

4664 5009 5856

1548 4383 5055

3172 4190 6373

5899 6443 6470

2572 3647 6240

1295 2158 6466

5604 6269 6368

3 5551 6454

3325 5797 6261

666 1397 5538

3069 4274 6410

4042 5992 6437

743 2073 3447

1344 2725 6386

283 2808 6303

2 4627 4632

26 1565 4000

4012 4946 6472

1629 6158 6467

6300 6351 6376

2969 4344 4440

2317 3115 4832

2099 5263 6283

2409 5868 5997

3752 4200 6350

3125 5841 6142

1 2249 6328

16 2525 6379

3198 5269 5960

4 1705 2069

990 4948 5520

1664 3836 4521

1765 4110 6454

9 1373 6387

1969 2405 6368

623 1428 3946

3111 6380 6436

1861 5611 5934

9 2444 3081

5 5508 6317
3184 4988 5995
1060 4803 6400
5021 5826 6289
1608 4754 5648
4702 6391 6421
3899 4811 6128
927 2286 5313
4123 6181 6453
2893 4150 5261
605 4332 5694
17 3518 6358
2858 6126 6478
15 1316 6465
2 2032 2983
5249 6340 6427
5 6003 6200
4478 6315 6420
5158 6390 6447
2598 3229 5399
3747 6424 6446
1412 2453 6332
5256 5715 6455
2137 3421 4368
15 3880 5245

17 3156 5638
3227 3798 6230
2094 3129 6458
1412 5573 5932
175 1182 6304
3555 6407 6463
583 1654 6339
14 6261 6449
3553 5383 5679
2092 2744 4153
0 4466 6472
11 3840 4354
17 5457 6222
1467 6083 6220
3449 3858 6337
3782 5318 6426
417 5038 5790
3571 5638 5873
6117 6241 6476
1898 5680 6213
3235 3817 6429
2095 4194 6224
2 4092 6448
5 6330 6383
285 5075 6334

10 505 2867

1183 5956 6466

839 4716 6471

984 3254 6432

1501 4790 6465

8 1457 1707

1660 1969 6438

4349 6182 6305

1423 3848 5490

1651 2969 6345

344 4164 6298

2397 6027 6274

2233 2778 6161

13 1778 2977

9 1916 3377

0 3 6190

395 4893 6394

3512 4098 6400

3490 6281 6473

12 1359 6465

4202 3179 6412

3007 3542 4271

2400 3350 6351

7 5490 5716

4695 5231 6266

777 6292 6402
919 4851 6367
6 644 3893
5386 6190 6434
17 169 4896.

[Claim 50]

A data processing method comprising:

a decoding step of decoding an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 27/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

658 706 898 1149 2577 2622 2772 3266 3329 5243 6079
6271

289 784 1682 3584 3995 4821 4856 5063 5974 6168 6437
6453

658 1126 2043 2065 2486 4118 4284 5394 5444 5477 5727

6018

641 928 1225 2841 4052 4840 4992 5268 5533 6249 6461

6475

2312 2917 3713 3849 4059 4241 4610 5440 5727 6101 6397

6444

1165 1592 1891 2154 3981 4817 5181 5748 5788 6012 6266

6350

13 2758 3069 4233 4697 5100 5279 5677 5919 5969 6280

6422

818 1500 2125 2340 3774 4707 4901 5170 5744 6008 6316

6353

857 3054 3409 3496 3704 4868 5326 6211 6292 6356 6367

6381

0 7 12 1709 2166 3418 3723 4887 5770 6043 6069 6431

2481 3379 4650 4900 4910 5060 5410 5425 6056 6173 6283

6386

15 814 854 1871 2934 3387 3915 5180 5303 5442 5581 5665

146 1882 3076 4458 4848 5252 5602 5778 5821 6213 6251

6401

2 947 1419 1566 3437 3646 4615 4634 4735 5819 5943 6280

1231 2309 2920 4158 4135 4298 4711 5082 5757 5762 6204

6209

257 297 337 2783 3230 4134 4480 4749 5295 5689 5921

6202

1436 2151 2629 3217 3930 4078 5386 5799 5906 6146 6226

6366

133 530 2448 4745 5000 5020 5224 5273 6211 6266 6431

6453

13 2644 3895 3898 4485 4722 5142 5462 5951 6031 6084

6351

6 3000 3873 3995 4680 5158 5504 5692 5755 6255 6338

6359

166 465 1658 2549 2941 4244 5071 5149 5452 5874 5939

6038

2309 2937 4282 4628 5113 5454 5731 5825 6021 6171 6402

6472

3 1077 2116 2426 2830 4853 5066 5571 5850 5916 6389

6421

817 1668 2229 2925 3281 4393 5042 5058 5377 5464 5588

6448

1848 3871 4381 4776 5366 5578 5648 6143 6389 6434 6465

6473

1263 1616 3150 3497 3759 4078 5530 5665 5694 5913 6397

6420

11 813 2185 2795 3349 4652 4678 5078 5504 6011 6286

6387

3060 3161 4584 4996 5143 5542 5697 5937 6141 6155 6342

6445

1638 2333 2632 3450 3505 3911 4399 4454 5499 5860 6044

6360

650 1744 4517
5772 6071 6471
3582 3622 5776
6153 6380 6446
3977 5932 6447
2071 4597 4891
11 1428 3776
1111 3874 5048
1410 2144 4445
4681 5481 6462
4044 5037 5497
2716 2891 6411
3299 4384 6224
1843 6087 6400
4664 5009 5856
1548 4383 5055
3172 4190 6373
5899 6443 6470
2572 3647 6240
1295 2158 6466
5604 6269 6368
3 5551 6454
3325 5797 6261
666 1397 5538
3063 4274 6410

4042 5992 6437
743 3075 3447
1344 2725 6386
283 2808 6303
2 4627 4632
26 1565 4000
4012 4946 6472
1629 6158 6467
6300 6351 6376
2969 4344 4440
2317 3115 4832
2099 5263 6285
2409 5868 5997
3752 4200 6350
3125 5841 6142
1 2249 6328
16 2525 6379
3198 5269 5960
4 1705 2069
990 4948 5520
1664 3836 4521
1765 4110 6454
9 1373 6387
1969 2405 6368
623 1428 3946

3111 6380 6436

1861 5611 5934

9 2444 3081

5 5508 6317

3184 4988 5995

1060 4803 6400

5021 5826 6289

1608 4754 5648

4702 6391 6421

3899 4811 6128

927 2286 5313

4123 6181 6453

2893 4150 5261

605 4332 5094

17 3516 6358

2858 6126 6478

15 1316 6465

2 2032 2983

5249 6340 6427

5 6003 6200

4478 6315 6420

5158 6390 6447

2598 3229 3390

3747 6424 6446

1412 2453 6332

5256 5715 6455

2137 3421 4368

15 3880 5245

17 3156 5638

3227 3798 6230

2094 3129 6458

1412 5573 5932

175 1182 6304

3555 6407 6463

583 1654 6339

14 6261 6449

3553 5383 5679

2092 2744 4153

0 4466 6472

11 3840 4354

17 5457 6222

1467 6083 6220

3449 3858 6337

3782 5318 6426

417 3038 5790

3571 5638 5873

6117 6241 6476

1898 5680 6219

3235 3817 6429

2095 4194 6224

2 4092 6448

5 6330 6383

285 5075 6334

10 505 2867

1183 5956 6466

839 4716 6471

984 3254 6432

1501 4790 6465

8 1457 1707

1660 1969 6438

4349 6182 6305

1423 3848 5490

1651 2969 6345

344 4164 6298

2397 6027 6274

2233 2778 6161

13 1778 2977

9 1916 3377

0 3 6190

395 4893 6394

3512 4098 6400

3490 6281 6473

12 1359 6465

4202 5179 6412

3007 3542 4271

2400 3350 6351

7 5490 5716

4695 5231 6266

777 6292 6402

919 4851 6367

6 644 3893

5386 6190 6434

17 169 4896.

[Claim 31]

A data processing apparatus comprising:

an encoding unit configured to encode information bits into an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 28/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

85 314 1602 1728 1929 2295 2729 2924 3779 4054 4276

618 1378 1838 1903 2399 2524 2937 3615 3740 4140 4213

1361 1430 2639 2648 2910 3418 3511 3543 4177 4209 4248
472 1143 1318 1545 1830 2228 2249 2256 3626 3839 3991
226 1401 2154 2318 2851 3317 3468 3944 3983 4047 4093
490 1145 1247 1851 2671 2776 3152 3229 3345 3758 3786
522 1393 1473 2196 2707 3052 3398 3814 3827 4148 4301
417 1982 2176 2336 2459 2806 3005 3771 3870 4080 4243
112 1040 1596 1621 1685 2118 2571 3359 3945 4034 4171
646 1705 2181 2439 2808 2851 2987 3044 3494 4049 4312
6 11 115 245 663 1773 2624 3444 3601 3952 4246
11 541 1020 1326 2259 2347 2750 2861 3328 3428 4126
515 941 1233 1804 2295 2528 3263 3826 4002 4022 4224
46 484 679 1349 2342 2929 3555 3860 3918 4068 4113
1832 2023 2279 2376 2965 3278 3318 3549 3640 3843 3910
241 943 1222 1583 1637 2743 3335 4080 4086 4203 4300
11 1419 1841 2398 2920 3409 3703 3768 3878 4052 4254
878 2049 2123 2431 2657 2704 3135 3342 3728 4141 4162
16 937 1267 1410 2100 3026 3099 3107 4042 4129 4157
133 646 1367 1394 2118 2311 2676 2956 3195 3536 3657
698 1444 2129 2432 2494 2793 2947 3852 3985 4254 4319
11 1076 1618 1995 2332 2743 2934 3009 3565 4169 4188
14 20 808 2629 2681 3090 3491 3835 4017 4068 4083
433 1386 2416 2570 2950 3611 3869 3969 4248 4251 4316
384 1292 1534 2610 2617 3559 3638 3964 4131 4293 4313
271 564 1719 2288 2597 2674 3429 3435 3793 4074 4286
133 190 815 953 1485 2000 2860 3000 3734 4013 4287

559 771 1762 2537 2764 2816 3186 3806 3933 4224 4271
11 733 1198 1735 1856 2668 2754 3216 4070 4113 4311
4 806 1832 2047 2058 2724 3387 3793 3833 4005 4319
506 1456 2339 3069 3343 3442 3889 3939 4013 4212 4278
2038 3980 4313
64 2373 4080
800 1535 4166
1030 3759 4002
1687 3269 4225
1219 2632 3878
719 2916 4277
1261 1930 3459
777 1568 1914
4 397 3290
10 2451 4115
3629 3885 4155
2652 3668 4026
135 3172 4319
1426 1970 3657
199 1268 2064
570 845 2761
41 1067 3498
1588 2482 2750
1615 2013 2715
121 1812 2588

10 992 1082

1929 4225 4279

6 1967 3760

593 1812 4107

891 2146 4158

924 2282 3585

592 2971 4235

260 3493 4313

2423 3180 3449

2042 3118 3625

2877 3064 3882

7 2139 4316

4 7 2954

1398 3947 4272

3675 4253 4318

1561 1977 2432

2531 4192 4209

1032 1102 4268

75 1718 3438

925 1073 4171

2124 2762 4148

4 3455 4069

3 1279 3382

1277 1746 3369

2727 3127 4230

584 1108 3454
9 2057 3061
1608 4103 4310
2673 3164 3713
1379 4072 4318
950 3447 4146
2509 4295 4296
819 1352 3371
3562 3865 4041
940 1217 3607
114 2544 4310
4 2178 4213
2035 4246 4251
272 1236 2733
953 2762 4115
1853 3496 4309
1119 3740 4318
2051 4058 4317
0 3162 4207
2389 4034 4111
4 3395 4301
3716 4089 4198
6 4272 4311
1 4 1854
4238 4299 4305

7 10 3737

11 3764 4296

297 1912 4117

1087 1796 4056

2153 3882 4030

962 4043 4203

243 3841 4308

2183 3886 4216

943 1974 2897

278 3224 3933

3 4196 4245

3409 4301 4315

2 2176 3214

462 3203 4008

478 2178 4202

3593 3825 4216

115 2796 4225

3827 4196 4251

1375 4301 4306

296 407 2055

688 3913 4281

3446 3840 4314

1073 3444 4146

1556 2761 3391

2 3543 4264

1378 3347 4305

847 1952 2745

1 1743 4042

2087 3048 4254

1910 4073 4132

2610 4129 4152

4106 4120 4313

7 4282 4304

3885 4227 4319

1235 4105 4195

1700 2332 4224

9 3750 4282

1539 4013 4310

3734 3834 4011

1397 2758 3645

7 1000 2984

11 3433 4068

1139 1800 3352

8 546 2561

1 4209 4239

2366 4063 4282

279 2524 2533

637 1913 4006

2322 2623 2960

758 303 2304

9 13 4241
3887 4299 4318
2612 3830 4230
1300 1596 2155
3622 3671 4230
2491 3722 3977
735 3812 4201
3204 3796 4317
2727 4292 4305
1062 2676 4255
2777 3131 4286
2518 3352 3937
4225 4255 4317
3644 3822 4311
1853 3754 4094
599 2608 3276.

[Claim 52]

A data processing method comprising:
an encoding step of encoding information bits into an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 28/30 on the basis of a parity check matrix of the LDPC code, wherein
the LDPC code includes information bits and parity bits,
the parity check matrix includes an information matrix portion corresponding to the information bits and a parity

matrix portion corresponding to the parity bits,

the information matrix portion is represented by a
parity check matrix initial value table, and

the parity check matrix initial value table is a table
showing positions of elements of 1 in the information matrix
portion in units of 360 columns, including

85	314	1602	1728	1929	2295	2729	2924	3779	4054	4276
918	1378	1838	1903	2399	2524	2937	3615	3740	4140	4213
1361	1430	2639	2648	2910	3418	3511	3543	4177	4209	4248
472	1143	1313	1545	1830	2228	2249	2256	3626	3839	3991
226	1401	2154	2313	2851	3317	3468	3944	3983	4047	4093
490	1145	1247	1851	2671	2776	3152	3229	3345	3758	3786
522	1393	1473	2196	2707	3052	3398	3814	3827	4148	4301
417	1982	2176	2336	2459	2806	3005	3771	3870	4080	4243
112	1040	1596	1621	1685	2113	2571	3359	3945	4034	4171
646	1705	2181	2439	2808	2851	2987	3044	3494	4049	4312
6	11	115	245	663	1773	2624	3444	3601	3952	4246
11	541	1020	1326	2259	2347	2750	2861	3328	3428	4126
515	941	1233	1864	2295	2528	3265	3826	4002	4022	4224
46	484	679	1349	2342	2929	3555	3860	3918	4068	4113
1932	2023	2279	2376	2965	3278	3318	3549	3640	3843	3910
241	943	1222	1533	1637	2745	3338	4080	4086	4203	4300
11	1419	1841	2398	2920	3409	3703	3766	3878	4052	4254
878	2049	2123	2431	2657	2704	3135	3342	3728	4141	4162
16	837	1267	1410	2100	3026	3099	3197	4042	4129	4157

133 646 1367 1394 2118 2311 2676 2956 3195 3536 3657
698 1444 2129 2432 2494 2793 2947 3852 3985 4254 4319
11 1076 1618 1995 2332 2743 2934 3009 3565 4169 4188
14 20 808 2629 2681 3090 3491 3835 4017 4068 4083
433 1386 2416 2570 2950 3611 3869 3969 4248 4251 4316
384 1292 1534 2610 2617 3559 3638 3964 4131 4293 4313
271 564 1719 2288 2597 2674 3429 3455 3793 4074 4286
133 190 815 955 1485 2000 2860 3000 3734 4013 4287
559 771 1762 2537 2764 2816 3186 3806 3933 4224 4271
11 733 1198 1735 1856 2668 2754 3216 4070 4113 4311
4 806 1832 2047 2058 2724 3387 3793 3833 4005 4319
506 1456 2339 3069 3343 3442 3889 3939 4013 4212 4278
2038 3980 4313
64 2373 4080
800 1535 4166
1030 3759 4002
1687 3269 4225
1219 2632 3878
719 2916 4277
1263 1930 3459
777 1568 1914
4 397 3290
10 3451 4115
3629 3885 4155
2652 3668 4026

135 3172 4319
1426 1970 3657
199 1268 2064
570 845 2761
41 1067 3498
1588 2482 2750
1615 2013 2715
121 1812 2588
10 992 1082
1929 4225 4279
6 1967 3760
593 1812 4107
891 2146 4153
924 2282 3585
592 2971 4235
260 3493 4313
2423 3180 3449
2042 3118 3625
2877 3064 3882
7 2139 4316
4 7 2954
1398 3947 4272
3675 4253 4318
1561 1977 2432
2531 4192 4209

1032 1102 4268

75 1718 3438

925 1073 4171

2124 2762 4148

4 3455 4069

3 1279 3382

1277 1746 3969

2727 3127 4230

584 1108 3454

9 2057 3061

1608 4103 4310

2673 3164 3713

1379 4072 4318

950 3447 4146

2509 4255 4296

819 1352 3371

3562 3865 4041

940 1217 3607

114 2544 4310

4 2178 4213

2035 4246 4251

272 1236 2733

953 2762 4115

1253 3496 4309

1119 3740 4318

2051 4058 4317

0 3162 4207

2389 4034 4111

4 3395 4301

3716 4089 4198

6 4272 4311

1 4 1854

4238 4299 4305

7 10 3737

11 3764 4296

297 1912 4117

1087 1796 4056

2153 3882 4030

962 4043 4203

243 3841 4308

2183 3896 4216

943 1974 2897

278 3224 3933

3 4196 4245

3409 4301 4315

2 2176 3214

462 3203 4008

478 2178 4202

3593 3825 4218

115 2796 4225

3827 4196 4251

1375 4301 4306

296 407 2055

688 3913 4281

3446 3840 4314

1073 3444 4146

1556 2761 3391

2 3543 4264

1378 3347 4305

847 1952 2745

1 1743 4042

2087 3048 4254

1010 4073 4132

2610 4129 4152

4106 4120 4313

7 4282 4304

3985 4227 4319

1235 4105 4195

1700 2332 4224

9 3759 4282

1539 4013 4310

3734 3834 4011

1397 2758 3645

7 1000 2984

11 3433 4068

1139 1800 3352

8 546 2561

1 4209 4239

2366 4063 4282

279 2524 2533

657 1913 4006

2322 2623 2960

758 803 2304

9 13 4241

3887 4299 4318

2612 3830 4230

1300 1596 2155

3622 3671 4230

2491 3722 3977

735 3812 4201

3204 3796 4317

2727 4292 4305

1062 2676 4255

2777 3131 4286

2518 3352 3937

4225 4255 4317

3644 3822 4311

1853 2754 4094

599 2608 3276.

[Claim 53]

A data processing apparatus comprising:

a decoding unit configured to decode an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 28/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

85	314	1602	1728	1929	2295	2729	2924	3779	4054	4276	
918	1378	1838	1903	2399	2524	2937	3615	3740	4140	4213	
1361	1430	2639	2649	2910	3418	3511	3543	4177	4209	4248	
472	1143	1318	1545	1830	2228	2249	2256	3626	3839	3991	
226	1401	2154	2318	2831	3317	3463	3944	3983	4047	4093	
490	1145	1247	1851	2671	2776	3152	3229	3345	3758	3786	
522	1393	1473	2196	2707	3052	3398	3814	3827	4148	4301	
417	1982	2176	2336	2459	2806	3005	3771	3870	4080	4243	
112	1640	1596	1621	1685	2118	2571	3359	3945	4034	4171	
646	1705	2181	2439	2808	2851	2987	3044	3494	4049	4312	
6	11	115	245	663	1773	2624	3444	3601	3952	4246	

11 541 1020 1326 2259 2347 2750 2861 3328 3428 4126
515 941 1233 1804 2295 2528 3265 3826 4002 4022 4224
46 484 679 1949 2342 2929 3555 3860 3918 4068 4113
1832 2023 2279 2376 2965 3278 3318 3549 3640 3843 3910
241 943 1222 1583 1637 2745 3338 4080 4086 4203 4300
11 1419 1841 2398 2920 3409 3703 3768 3878 4052 4254
878 2049 2123 2431 2657 2704 3135 3342 3728 4141 4162
16 837 1267 1410 2100 3026 3099 3167 4042 4129 4157
133 646 1367 1394 2118 2311 2676 2956 3195 3536 3657
698 1444 2129 2432 2494 2793 2947 3852 3985 4254 4319
11 1076 1618 1995 2332 2743 2934 3009 3565 4169 4188
14 20 808 2429 2681 3090 3491 3835 4017 4068 4083
433 1386 2416 2570 2950 3611 3869 3969 4248 4251 4316
384 1292 1534 2610 2617 3559 3638 3964 4131 4293 4313
271 564 1719 2288 2597 2674 3429 3455 3793 4074 4286
133 190 815 955 1485 2000 2860 3009 3734 4013 4287
559 771 1762 2537 2764 2816 3186 3806 3933 4224 4271
11 733 1198 1735 1856 2668 2754 3216 4070 4113 4311
4 806 1832 2047 2058 2724 3387 3743 3833 4005 4319
506 1456 2339 3069 3343 3442 3889 3939 4013 4212 4278
2038 3980 4313
64 2373 4080
800 1535 4166
1030 3759 4002
1687 3264 4225

1219 2632 3873

719 2916 4277

1261 1930 3459

777 1568 1914

4 397 3290

10 3451 4115

3629 3885 4155

2652 3668 4026

135 3172 4319

1426 1970 3657

199 1268 2064

570 845 2761

41 1067 3498

1588 2482 2750

1615 2013 2715

121 1812 2588

10 992 1082

1929 4225 4279

6 1967 3760

593 1812 4107

891 2146 4158

924 2282 3585

592 2971 4235

260 3493 4313

2423 3180 3449

2042 3118 3625

2877 3064 3862

7 2139 4316

4 7 2954

1398 3947 4272

3675 4253 4318

1561 1977 2432

2531 4192 4209

1032 1102 4268

75 1718 3438

925 1073 4171

2124 2762 4148

4 3455 4069

3 1279 3382

1277 1746 3969

2727 3127 4230

584 1108 3454

9 2057 3061

1608 4103 4310

2673 3164 3713

1379 4072 4318

950 3447 4146

2509 4255 4296

819 1352 3371

3562 3865 4041

940 1217 3607
114 2544 4310
4 2178 4213
2035 4246 4251
272 1236 2733
953 2762 4115
1853 3496 4309
1119 3740 4318
2051 4058 4317
0 3162 4207
2389 4034 4111
4 3395 4301
3716 4089 4198
6 4272 4311
1 4 1854
4238 4299 4305
7 10 3737
11 3764 4296
297 1912 4117
1087 1796 4056
2153 3882 4030
962 4043 4203
243 3841 4308
2183 3686 4216
943 1974 2897

278 3224 3933

3 4196 4245

3409 4301 4315

2 2176 3214

462 3203 4008

478 2178 4202

3593 3825 4216

115 2796 4225

3827 4196 4251

1375 4301 4306

296 407 2055

628 3913 4281

3446 3840 4314

1073 3444 4146

1556 2761 3391

2 3543 4264

1378 3347 4305

847 1952 2745

1 1743 4042

2087 3048 4254

1010 4073 4132

2010 4129 4132

4106 4120 4313

7 4282 4304

3885 4227 4319

1235 4105 4195

1700 2332 4224

9 3750 4282

1539 4013 4310

3734 3834 4011

1397 2758 3645

7 1000 2984

11 3433 4068

1139 1800 3352

8 546 2561

1 4209 4239

2366 4063 4282

279 2524 2533

657 1913 4006

2322 2623 2960

758 803 2304

9 13 4241

3387 4299 4318

2612 3830 4230

1300 1596 2155

3622 3671 4230

2491 3722 3977

735 3812 4201

3204 3796 4317

2727 4292 4305

1062 2676 4255

2777 3131 4286

2518 3352 3937

4225 4255 4317

2644 3822 4311

1853 3754 4094

599 2608 3276.

[Claim 54]

A data processing method comprising:

a decoding step of decoding an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 28/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

85 314 1692 1728 1929 2295 2723 2924 3779 4054 4276

918 1378 1838 1903 2399 2524 2937 3615 3740 4140 4213

1361 1430 2639 2648 2910 3418 3511 3543 4177 4209 4248

472 1143 1318 1545 1830 2228 2249 2256 3626 3839 3991
226 1401 2154 2318 2851 3317 3468 3944 3983 4047 4093
490 1145 1247 1851 2671 2776 3152 3229 3345 3758 3786
522 1393 1473 2195 2707 3052 3398 3814 3827 4148 4301
417 1982 2176 2336 2459 2806 3005 3771 3870 4080 4243
112 1040 1596 1621 1685 2118 2571 3359 3945 4034 4171
646 1705 2181 2439 2808 2851 2987 3044 3494 4049 4312
6 11 115 245 663 1773 2624 3444 3601 3952 4246
11 541 1020 1326 2259 2347 2750 2861 3328 3428 4126
515 941 1233 1804 2295 2528 3265 3826 4002 4022 4224
46 484 679 1949 2342 2929 3555 3860 3918 4068 4113
1932 2023 2279 2376 2965 3278 3318 3549 3640 3843 3910
241 943 1222 1583 1637 2745 3338 4080 4086 4203 4300
11 1419 1841 2398 2920 3409 3703 3768 3878 4052 4254
878 2049 2123 2431 2657 2704 3135 3342 3728 4141 4162
16 837 1267 1410 2100 3026 3099 3107 4042 4129 4157
133 616 1367 1394 2118 2311 2676 2956 3195 3536 3657
698 1444 2129 2432 2494 2793 2947 3852 3985 4254 4319
11 1076 1618 1995 2332 2743 2934 3009 3565 4169 4188
14 20 408 2629 2681 3090 3491 3835 4017 4068 4083
433 1386 2416 2570 2950 3611 3869 3969 4248 4251 4316
384 1292 1534 2610 2617 3559 3638 3964 4131 4293 4313
271 564 1719 2288 2597 2674 3429 3455 3793 4074 4286
135 190 815 955 1485 2000 2860 3000 3734 4013 4287
559 771 1762 2537 2764 2816 3186 3806 3933 4224 4271

11 733 1198 1735 1856 2668 2754 3216 4070 4113 4311
4 806 1832 2047 2058 2724 3387 3793 3833 4005 4319
506 1456 2339 3069 3343 3442 3889 3939 4013 4212 4278
2038 3980 4313
64 2373 4080
800 1535 4166
1030 3759 4002
1687 3269 4225
1219 2632 3878
719 2916 4277
1261 1930 3459
777 1568 1914
4 397 3290
10 3451 4113
3629 3885 4155
2652 3668 4026
135 3172 4319
1426 1970 3657
199 1268 2064
570 845 2761
41 1067 3438
1588 2482 2750
1615 2013 2715
121 1812 2588
10 992 1082

1929 4225 4279

6 1967 3760

593 1812 4107

891 2146 4158

924 2282 3585

592 2971 4235

260 3493 4313

2423 3180 3449

2042 3118 3625

2877 3064 3882

7 2139 4316

4 7 2954

1398 3947 4272

3675 4251 4318

1561 1977 2432

2531 4192 4209

1032 1102 4268

75 1718 3438

925 1073 4171

2124 2762 4148

4 3455 4069

3 1279 3382

1277 1746 3969

2727 3127 4230

184 1108 3454

9 2057 3061

1608 4103 4310

2673 3164 3713

1379 4072 4318

950 3447 4146

2509 4255 4296

819 1352 3371

3562 3865 4041

940 1217 3607

114 2544 4310

4 2178 4213

2035 4246 4251

272 1236 2733

953 2762 4115

1853 3496 4309

1119 3740 4318

2051 4058 4317

0 3162 4207

2389 4034 4111

4 3395 4301

3716 4089 4198

6 4272 4311

1 4 1854

4238 4299 4305

7 10 3737

11 3764 4296
297 1912 4117
1087 1796 4056
2153 3882 4030
962 4043 4203
243 3841 4308
2183 3886 4216
943 1974 2897
278 3224 3933
3 4196 4245
2409 4301 4315
2 2176 3214
462 3203 4008
478 2178 4202
3593 3825 4216
115 2796 4225
3827 4196 4251
1375 4301 4306
296 407 2055
688 3913 4281
3446 3840 4314
1073 3444 4146
1556 2761 3391
2 3543 4264
1378 3347 4306

847 1952 2745
1 1743 4042
2087 3048 4254
1010 4073 4132
2610 4129 4152
4106 4120 4313
7 4282 4304
3985 4227 4319
1235 4105 4195
1700 2332 4224
9 3750 4282
1539 4013 4310
3734 3834 4011
1397 2758 3645
7 1000 2984
11 3433 4068
1139 1800 3352
6 546 2561
1 4209 4239
2366 4063 4282
279 2524 2533
657 1913 4006
2322 2623 2960
758 803 2304
9 13 4241

3887 4299 4318
2612 3830 4230
1300 1596 2155
3622 3671 4230
2491 3722 3977
735 3812 4201
3204 3796 4317
2727 4292 4305
1062 2676 4255
2777 3131 4286
2518 3352 3937
4225 4255 4317
3644 3822 4311
1853 3754 4054
599 2608 3276.

[Claim 55]

A data processing apparatus comprising:

an encoding unit configured to encode information bits into an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 29/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

212 499 911 940 1392
316 563 1527 2006 2077
2 1906 2043 2112 2123
937 901 1582 1812 1955
5 978 1280 1933 2145
5 2035 2044 2108 2121
5 939 1874 1974
4 1069 1758
694 2096 2106
1129 1511 1659
1564 2089 2159
2 1605 2004
474 1341 2003
103 2128 2150
1656 1993 2153
1981 2122 2138
1083 1968 2141
1 298 2073
1042 1724 2137
1253 1758 2145

1209 1566 2123

1466 2116 2155

43 2006 2049

592 1806 1865

3 143 2149

1158 1448 2002

1422 2152 2157

485 2119 2150

371 1831 2086

204 2042 2151

174 544 974

1469 1795 1995

13 708 1683

5 1144 2030

486 1309 1576

165 2030 2147

504 2073 2126

263 565 1798

239 861 1861

862 1610 1716

1346 1971 2128

5 804 1399

2139 2144 2155

4 2136 2159

1485 2059 2158

50 1091 1332
373 1730 2092
59 1086 1401
1166 1781 2065
213 2080 2154
492 1905 2110
1 1517 2126
722 1427 2146
885 991 1842
3 278 1806
067 1354 1907
1697 2047 2156
684 1924 2151
2077 2122 2157
978 2054 2135
435 2034 2150
136 1997 2125
1504 1850 2153
1404 1989 2119
109 1601 2152
780 1473 2150
198 1723 2062
927 2087 2138
1 666 2018
1293 1960 2141

1648 2033 2144

681 1578 1999

1342 2022 2157

949 1907 1994

138 1261 2135

3 608 982

1211 1501 2150

201 229 1186

1295 2089 2132

267 556 2142

801 2052 2122

1382 2135 2155

572 1503 1704

346 1183 2129

1926 2090 2149

1337 2133 2140

5 1806 2125

1383 1628 2068

1193 1626 2138

1999 2115 2146

217 274 2021

3 816 2024

1380 2138 2157

607 1385 2110

184 1195 2063

C 1767 2108

C 2081 2097

1135 2036 2128

1748 2001 2125

797 1552 1926

1046 1890 2128

291 1859 2131

1075 1214 1762

60 549 1943

581 1197 1232

1009 2026 2136

884 2002 2117

1 576 1449

519 1968 2114

5 1489 1630

1926 2037 2158

2 1249 2159

0 811 2114

2055 2152 2159

892 1911 2120

204 1033 2033

1840 2012 2037

1746 2111 2155

1098 1835 2157

2 1492 1831

353 1537 1830

375 1264 2036

2 1628 2035

1096 1971 2021

950 1809 1884

253 467 1600

5 379 1833

4 1698 1970

37 1637 2136

1174 1460 2157

612 1827 2134

1783 1802 1949

2029 2113 2151

1984 2030 2141

2 347 462

862 1693 2121

2 895 1401

4 1901 2100

1183 1674 2069

1575 1940 2158

5 1904 2097

1044 2029 2092

1441 1943 2150

0 3 1300

2 516 1735

503 1342 2019
1421 1914 2131
28 986 1467
1270 1851 1988
481 1265 2016
530 546 909
653 1909 2158
1805 2002 2149
2 1359 1518
1640 2104 2129
1656 2109 2155
1307 1762 2114
565 1647 2118
1690 2081 2156
1 300 1995
5 1681 2151
1602 2050 2156
1 1960 2153
2061 2070 2138
1581 1673 2142
1048 1142 2101
1867 1991 2050
856 1640 1878
251 561 966
343 1816 2114

3 966 2045
1885 1922 2158
57 556 2059
732 1724 2147.

[Claim 56]

A data processing method comprising:

an encoding step of encoding information bits into an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 29/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

212 499 911 940 1392
316 563 1527 2006 2077
2 1906 2043 2112 2123
537 901 1582 1812 1955
5 978 1280 1933 2145
5 2035 2044 2108 2121

5 939 1874 1974

4 1069 1758

694 2096 2106

1129 1511 1659

1564 2089 2159

2 1605 2004

474 1341 2003

103 2129 2150

1656 1993 2153

1881 2122 2138

1088 1968 2141

1 298 2073

1042 1724 2137

1253 1758 2145

1209 1566 2123

1466 2116 2155

43 2006 2049

592 1806 1865

3 143 2149

1158 1448 2002

1422 2152 2157

485 2119 2156

371 1831 2086

204 2042 2151

174 544 974

1469 1795 1995

13 708 1683

5 1144 2030

486 1309 1576

165 2030 2147

504 2073 2126

263 565 1798

239 861 1861

862 1610 1716

1346 1971 2128

5 804 1399

2139 2144 2155

4 2136 2159

1485 2059 2158

50 1091 1332

373 1730 2092

59 1086 1401

1166 1781 2065

213 2080 2154

492 1905 2110

1 1517 2126

722 1427 2146

885 991 1842

3 278 1806

967 1354 1907

1697 2047 2156

684 1924 2151

2077 2122 2157

978 2054 2135

435 2034 2150

136 1997 2125

1504 1850 2153

1404 1989 2119

109 1001 2152

780 1473 2150

198 1723 2062

927 2087 2138

1 666 2018

1293 1960 2141

1648 2033 2144

681 1578 1999

1342 2022 2157

949 1907 1994

138 1261 2135

3 608 982

1211 1501 2150

201 228 1186

1295 2089 2132

267 556 2142

801 2052 2122

1382 2135 2155

572 1503 1704

346 1183 2129

1926 2090 2149

1337 2133 2140

5 1806 2125

1383 1628 2068

1193 1626 2138

1999 2115 2146

217 274 2021

3 816 2024

1380 2138 2157

607 1385 2110

184 1195 2063

0 1767 2108

0 2081 2097

1135 2036 2128

1748 2001 2125

797 1552 1926

1046 1890 2128

291 1859 2131

1075 1214 1762

60 549 1943

581 1197 1232

1009 2026 2136

884 2002 2117

1 576 1449

519 1968 2114

5 1489 1630

1926 2037 2158

2 1249 2159

0 811 2114

2055 2152 2159

802 1911 2120

204 1033 2033

1840 2012 2037

1746 2111 2155

1098 1835 2157

2 1492 1831

353 1537 1830

375 1264 2036

2 1638 2035

1096 1971 2021

950 1809 1884

253 467 1600

5 379 1833

4 1698 1970

37 1637 2136

1174 1460 2157

612 1827 2134

1783 1802 1949

2029 2118 2151

1984 2030 2141

2 347 462

862 1693 2121

2 895 1401

4 1901 2100

1183 1674 2069

1575 1940 2158

5 1904 2097

1044 2029 2092

1441 1943 2150

0 3 1300

2 516 1735

503 1342 2019

1421 1914 2131

28 986 1467

1270 1851 1988

481 1265 2016

520 546 909

653 1909 2158

1805 2002 2140

2 1250 1518

1640 2104 2129

1656 2109 2155

1307 1762 2114

565 1647 2118

1690 2081 2156

1 300 1995

5 1681 2151

1602 2050 2156

1 1960 2153

2061 2070 2138

1581 1673 2142

1048 1142 2101

1867 1991 2055

856 1610 1878

251 561 966

343 1816 2114

3 966 2045

1885 1922 2158

57 556 2059

732 1724 2147.

[Claim 57]

A data processing apparatus comprising:

a decoding unit configured to decode an LDPC (Low Density Parity Check) code having a code length of 64800 bits and a code rate of 29/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

212	499	911	940	1392
316	563	1527	2006	2077
2	1906	2043	2112	2123
537	901	1582	1812	1955
5	978	1280	1933	2145
5	2035	2044	2108	2121
5	939	1874	1974	
4	1069	1758		
694	2096	2106		
1129	1511	1659		
1564	2089	2159		
2	1605	2004		
474	1341	2003		
103	2128	2150		
1656	1993	2153		
1881	2122	2138		
1088	1968	2141		

1 298 2073
1042 1724 2137
1253 1758 2145
1209 1566 2123
1466 2116 2155
43 2006 2049
592 1806 1865
3 143 2149
1158 1448 2062
1422 2152 2157
485 2119 2150
371 1831 2086
204 2042 2151
174 544 974
1469 1795 1995
13 708 1683
5 1144 2079
486 1309 1576
165 2030 2147
504 2073 2126
263 565 1798
239 861 1861
862 1610 1716
1346 1971 2128
5 304 1399

2139 2144 2155

4 2136 2159

1485 2059 2158

50 1091 1332

373 1730 2092

59 1086 1401

1166 1781 2065

213 2080 2154

492 1905 2110

1 1517 2126

722 1427 2146

885 991 1842

3 278 1806

967 1354 1907

1697 2047 2156

684 1924 2151

2077 2122 2157

978 2054 2135

435 2034 2150

136 1997 2125

1504 1850 2153

1404 1989 2113

109 1001 2152

730 1473 2150

198 1723 2062

927 2087 2138

1 666 2018

1293 1960 2141

1648 2033 2144

681 1578 1999

1342 2022 2157

949 1907 1994

138 1261 2135

3 608 982

1211 1501 2150

201 228 1186

1295 2089 2132

267 556 2142

801 2052 2122

1382 2135 2155

572 1503 1704

346 1183 2129

1926 2090 2149

1337 2133 2140

5 1806 2135

1383 1628 2068

1193 1626 2138

1999 2115 2146

217 274 2021

3 816 2024

1380 2138 2157

607 1385 2110

184 1195 2063

0 1767 2108

0 2081 2097

1135 2036 2128

1748 2001 2125

797 1552 1926

1046 1890 2128

291 1859 2131

1075 1214 1762

60 549 1943

581 1197 1232

1009 2026 2136

884 2002 2117

1 576 1449

519 1968 2114

5 1489 1630

1906 2037 2158

2 1249 2159

0 811 2114

2055 2152 2159

802 1911 2120

204 1033 2033

1840 2012 2037

1746 2111 2155

1098 1835 2157

2 1492 1831

353 1537 1830

375 1264 2036

2 1638 2035

1096 1971 2021

950 1809 1884

253 467 1609

5 379 1823

4 1698 1970

37 1637 2136

1174 1460 2157

612 1827 2134

1783 1802 1949

2029 2118 2151

1984 2030 2141

2 347 462

862 1693 2121

2 895 1401

4 1901 2190

1183 1674 2069

1575 1940 2158

5 1904 2097

1044 2029 2092

1441 1943 2150

0 3 1300

2 516 1735

503 1342 2019

1421 1914 2131

28 986 1467

1270 1851 1989

481 1265 2016

530 546 909

653 1909 2158

1805 2002 2149

2 1359 1518

1640 2104 2129

1656 2109 2155

1307 1762 2114

565 1647 2118

1690 2081 2156

1 300 1995

5 1681 2151

1602 2050 2156

1 1960 2153

2061 2070 2138

1581 1673 2142

1048 1142 2101

1867 1991 2055

856 1640 1878

251 561 966

343 1816 2114

3 966 2045

1885 1922 2158

57 556 2059

732 1724 2147.

[Claim 58]

A data processing method comprising:

a decoding step of decoding an LDPC (Low Density Parity Check) code having a code length of 54800 bits and a code rate of 29/30 on the basis of a parity check matrix of the LDPC code, wherein

the LDPC code includes information bits and parity bits,

the parity check matrix includes an information matrix portion corresponding to the information bits and a parity matrix portion corresponding to the parity bits,

the information matrix portion is represented by a parity check matrix initial value table, and

the parity check matrix initial value table is a table showing positions of elements of 1 in the information matrix portion in units of 360 columns, including

212 499 911 946 1392

316 563 1527 2006 2077

2 1966 2643 2112 2123

537 901 1582 1812 1955

5 978 1280 1934 2145

5 2035 2044 2108 2121

5 939 1874 1974

4 1069 1758

694 2096 2106

1129 1511 1659

1564 2089 2159

2 1605 2004

474 1341 2603

103 2128 2150

1656 1993 2153

1881 2122 2138

1988 1968 2141

1 298 2073

1042 1724 2137

1253 1758 2145

1209 1566 2123

1466 2116 2155

43 2006 2049

592 1806 1865

3 143 2149

1158 1448 2002

1422 2152 2157

485 2119 2159

371 1831 2086
204 2042 2151
174 544 974
1469 1795 1995
13 708 1683
5 1144 2030
486 1309 1576
165 2030 2147
504 2073 2126
263 565 1798
239 861 1861
862 1610 1716
1346 1971 2128
5 904 1399
2139 2144 2155
4 2136 2159
1485 2059 2158
50 1091 1332
373 1730 2092
59 1086 1401
1166 1781 2065
213 2080 2154
492 1905 2110
1 1517 2126
722 1427 2146

885 991 1842

3 278 1806

967 1354 1907

1697 2047 2156

684 1924 2151

2077 2122 2157

978 2054 2135

435 2034 2150

136 1997 2125

1504 1850 2153

1404 1989 2119

109 1001 2152

780 1473 2150

198 1723 2062

927 2087 2138

1 666 2018

1293 1960 2141

1648 2033 2144

681 1578 1999

1342 2022 2157

949 1907 1994

138 1261 2135

3 608 982

1211 1501 2150

201 223 1186

1295 2089 2132

267 556 2142

801 2052 2122

1382 2135 2155

572 1503 1704

346 1183 2129

1926 2090 2149

1337 2133 2140

5 1806 2125

1383 1628 2068

1193 1626 2138

1999 2115 2146

217 274 2021

3 816 2024

1380 2138 2157

607 1385 2110

184 1195 2063

0 1767 2108

0 2081 2097

1135 2036 2129

1748 2001 2125

797 1552 1926

1046 1890 2128

291 1859 2131

1075 1214 1762

60 549 1943

581 1197 1232

1009 2026 2136

884 2002 2117

1 576 1449

519 1968 2114

5 1489 1630

1926 2037 2158

2 1249 2159

0 811 2114

2055 2152 2159

802 1911 2120

204 1033 2033

1840 2012 2037

1746 2111 2155

1098 1835 2157

2 1492 1831

353 1537 1830

375 1264 2036

2 1638 2035

1096 1971 2021

950 1809 1884

253 467 1600

5 379 1833

4 1698 1970

37 1637 2136
1174 1460 2157
612 1827 2134
1783 1802 1949
2029 2118 2151
1984 2030 2141
2 347 462
862 1693 2121
2 895 1401
4 1901 2100
1183 1674 2069
1575 1940 2158
5 1904 2097
1044 2029 2092
1441 1943 2150
0 3 1300
2 516 1735
503 1342 2019
1421 1914 2131
28 986 1467
1270 1851 1988
481 1265 2016
530 546 909
653 1909 2158
1805 2002 2149

2 1359 1518

1640 2104 2129

1656 2109 2155

1307 1762 2114

565 1647 2118

1690 2081 2156

1 300 1995

5 1681 2151

1602 2050 2156

1 1960 2153

2061 2070 2138

1591 1673 2142

1048 1142 2101

1867 1991 2055

856 1640 1878

251 561 966

343 1816 2114

3 966 2045

1885 1922 2158

57 556 2059

732 1724 2147.