BOARD-ON-CHIP PIN-GRID ARRAY SEMICONDUCTOR PACKAGE AND METHOD OF CONSTRUCTION

ABSTRACT OF THE INVENTION

A pin-grid array semiconductor package is disclosed. The pin-grid array semiconductor package (14) includes a housing (20) having a first surface (22) and a second surface (24). A semiconductor die (64) having a number of conductive wires (68) is disposed within the housing (20). Each conductive wire (68) is coupled to a lateral conductor (32) contained within the housing (20). Each lateral conductor (32) is coupled to a pin (16). Each pin (16) has a first end (72) and a second end (74). The first end (72) of each pin (16) protrudes beyond the first surface (22) of the housing (20). The second end (74) of each pin (16) forms a receptacle (76) at the second surface (24) of the housing (20). In a particular embodiment, a second pin-grid array semiconductor package (114) is coupled to the pin-grid array semiconductor package (14) to form a three-dimensional semiconductor stack (80).

Figure 3