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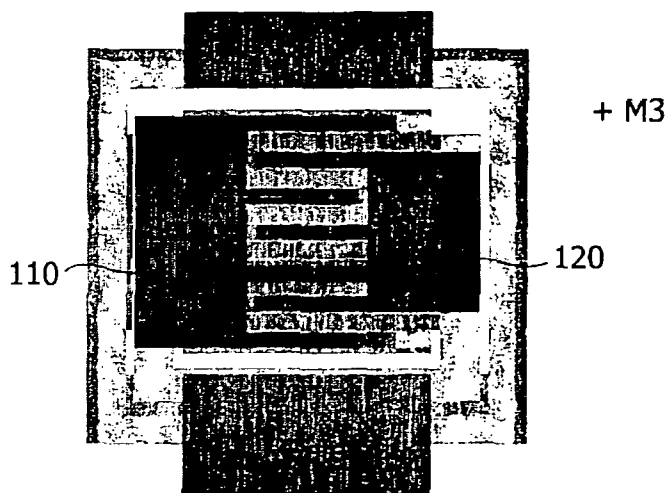
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(54) Title: HIGH FREQUENCY TRANSISTOR LAYOUT FOR LOW SOURCE DRAIN CAPACITANCE



(57) Abstract: An RF field effect transistor has a gate electrode, and comb shaped drain and source electrodes, fingers of the comb shaped drain being arranged to be interleaved with fingers of the source electrode, the source and drain electrodes having multiple layers (110,120,130,140). An amount of the interleaving is different in each layer, to enable optimization, particularly for low parasitic capacitance without losing all the advantage of low current density provided by the multiple layers. The interleaving is reduced for layers further from the gate electrode by having shorter fingers. The reduction in interleaving can be optimised for minimum capacitance, by a steeper reduction in interleaving, or for minimum lateral current densities in source and drain fingers, by a more gradual reduction in interleaving. This can enable operation at higher temperatures or at higher input bias currents, while still meeting the requirements of electro-migration rules.

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