## Abstract

**ESD PARASITIC BIPOLAR TRANSISTORS WITH HIGH RESISTIVITY REGIONS IN THE COLLECTOR**

A method and a structure for a parasitic bipolar silicided ESD device that has high resistivity regions within the collector of the parasitic NPN. The device has the structure of a N-MOS transistor and a substrate contact. The device preferably has silicide regions over the doped regions. The invention has two types of high resistivity regions: 1) isolation regions (e.g., oxide shallow trench isolation (STI)) and 2) undoped or lightly doped regions (e.g., channel regions). The channel regions can have gates thereover and the gates can be charged. Also, optionally a n⁻ well (n minus well) can be formed under the collector. The high resistivity regions increase the collector resistivity thereby improving the performance of the parasitic bipolar ESD device.

**(FIGURE 1A IS SUGGESTED FOR PUBLICATION)**