ABSTRACT

"a bus cycle signature system"

A bus cycle signature system for testing CPU based boards comprising a data shift register and a general shift register which receive test signals from the board under test, the signals received by the shift registers being sampled by clock signals associated with bus cycle operations performed by a CPU on the board under test. The sampled signals form a board signature which can be compared with a similarly obtained signal from a known good board to detect faults in the board under test.

This Sheet Has Been Replaced

