

A Protection Circuit

5 This invention relates to circuits for use with voltages substantially higher than normal operating voltages and particularly, though not exclusively to EPROM (erasable programmable read-only memory) circuits and EEPROM (electrically erasable programmable read-only memory) circuits.

10 In order to be able to program an EEPROM memory cell, a high voltage is needed to obtain a Fowler-Nordheim tunneling effect in the cell. However, when there is a high voltage between the drain and the gate and source electrodes of an 'off' EEPROM transistor, a breakdown can occur, creating a leakage current
15 between the drain junction and the bulk of the transistor. Such breakdown is known as BVDSS breakdown.

It is known to use additional transistors coupled between series transistors and gated with a voltage approximately half that applied to the series transistors in order to prevent
20 breakdown in the series transistors. However, in known circuits utilising such protection transistors it is still possible breakdown to occur or for data to be lost if the protection transistors are not gated with the required protection voltage at exactly the right time.

25 It is an object of the present invention to provide a circuit for use with high voltage wherein the above disadvantages may be overcome or at least alleviated.

In accordance with the present invention a protection circuit comprises:

30 first transistor means of a first conductivity type;

second transistor means of a second conductivity type opposite to that of the first transistor means and coupled to the first transistor means;

35 first and second transistor protection means respectively comprising transistors of opposite conductivity types and coupled between the first and second transistor means; and application means for applying to the first and second transistor means a first voltage which

changes between a high level and a low level and for
applying to one of the transistor protection means a second
voltage which changes from a datum level to a predetermined
level between the high and low levels as the first voltage
5 changes from the low level to the high level,

characterized in that

the application means comprises: detection means for
detecting when the first voltage rises by a predetermined
amount above the predetermined level; and switching means
10 for causing the second voltage to change from the datum
level to the predetermined level in response to detection
by the detection means.

Three circuits in accordance with the present
invention will now be described, by way of example only,
15 with reference to the accompanying drawings, in which:

Figure 1 shows a voltage translator circuit for use
with EEPROM memory;

Figure 2 shows a timing diagram illustrating various
voltages occurring in the circuit of Figure 1;

20 Figure 3 shows a latch circuit for use with EEPROM
memory; and

Figure 4 shows a circuit for use in the circuits of
Figures 1 and 3 to control the application of PMOS
transistor protection voltage.

25 Referring now to Figure 1, a voltage translator
circuit for use in an EEPROM memory includes two parallel
arrangements of field effect transistors (FETs) 1, 5, 7, 3
and 2, 6, 8, 4, the transistors of each group having their
current electrodes connected in series between a datum
30 potential VSS and a supply line having a potential VPP or
VDD as required. The transistors 1, 2, 5, 6 are PMOS
transistors all having their bulks connected to the supply
line, while the transistors 3, 4, 7, 8 are NMOS transistors
all having their bulks connected to ground. The gate
35 electrodes of PMOS transistors 5 and 6 are connected to a
line HVPP. The gate electrodes of NMOS transistors 7 and 8
are connected to a line HVPN. The gate electrodes of
transistors 1 and 2 are connected respectively to the

junctions between the current electrodes of the transistors 6, 8 and 5, 7, these junctions are connected to differential outputs (OUT+, OUT-) of the circuit. The gate electrodes of transistors 3 and 4 are connected to
5 differential inputs (IN+, IN-) of the circuit.

The purpose of the circuit of Figure 1 is to convert low voltage input data (at IN+, IN-) into high voltage output data (at OUT+, OUT-) when the supply line connected to the gate electrodes of transistors 1 and 2 is at its
10 high voltage VPP (typically 20 volts) rather than its low voltage VDD (typically 5 volts).

In order to avoid BVDSS breakdown problems on transistors 1, 2, 3, 4, transistors 5, 6, 7, 8 are added and are gated with a mid-range voltage VHN (typically 10
15 volts) applied to the lines HVPP and HVPN when the supply line voltage is high (VPP) so that transistors 1, 2, 3, 4 are not subjected to voltages between their drain and source electrodes sufficiently high to cause breakdown.

As the circuit must also function when the supply
20 line voltage is low (VDD), in this condition the gate electrodes of transistors 7, 8 can remain at potential VHN so that these NMOS transistors are 'on', but the gate electrodes of transistors 5, 6 must be grounded so that these PMOS transistors are also 'on'. Thus, for the PMOS
25 transistors 5, 6 the protecting voltage applied to the line HVPP must be switched from VSS to VHN when the supply line voltage changes from VDD to VPP for programming. This must be done when the supply line voltage reaches a critical level between VDD and VPP for the following reasons:

30 1) if the HVPP line is switched too early, one of the outputs (OUT+, OUT-) can be floating, because the gate of one of the protecting PMOS transistors will reach the mid-range potential VHN before its source;

2) conversely, if the HVPP line is switched too late,
35 leakage due to BVDSS breakdown can still occur because the transistors 1, 2, 3, 4 are not protected.

Referring now also to Figure 2, it can be seen that as the supply line voltage rises from VDD to VPP (line 9), there are two time periods in which switching the HVPP line gives rise to the above problems: the first time period 10 (corresponding to problem 1) above) begins as soon as the HVPP line has a potential greater than the supply line (as the supply line rises) and ends when the supply line voltage reaches a level equal to voltage VHN plus the PMOS transistor threshold voltage, and the second time period 11 (corresponding to problem 2) above) begins shortly before the supply line voltage reaches voltage VPP and lasts until the HVPP line is switched to level VHN. Thus, if the HVPP line is switched to voltage VHN in the first time period 10 the outputs (OUT+, OUT-) can be floating, and if the HVPP line is switched to voltage VHN in the second time period 11 BVDSS breakdown may occur in the PMOS transistors.

In order to ensure that the HVPP line is switched in the 'safe' time between the two time periods 10 and 11, a detector 12 and a switching circuit 13 are employed. The detector 12 monitors the supply line voltage and produces an output when the supply line voltage rises above the mid-range voltage VHN by more than the threshold voltage of the PMOS transistors 1, 2, 5, 6. When the detector 12 produces its output, the switching circuit 13 switches the voltage on the line HVPP from datum voltage VSS to mid-range voltage VHN. In this way the PMOS transistors will never be 'off', and the possibility of BVDSS breakdown due to late switching is avoided.

Referring now to Figure 3, a latch circuit is of similar structure to the translator circuit of Figure 1, FETs 21, 22, 23, 24, 25, 26, 27, 28 being the same, respectively, as the FETs 1, 2, 3, 4, 5, 6, 7, 8. The latch circuit of Figure 3 differs from the translator circuit of Figure 1 only in that the gate electrodes of the transistors 23, 24 are now connected respectively to the gate electrodes of the transistors 21, 22, and the junctions between the current electrodes of the transistors 26, 28 and 25, 27 now form inverse polarity I/O nodes.

Transistors 21, 22, 23, 24 form the cross inverter of a typical static CMOS RAM cell. The latch circuit of Figure 3 may be used to drive data into EEPROM arrays. However, the latch circuit suffers from the same problem as the voltage translator circuit of Figure 1: the switching of the HVPP line relative to the supply line when the supply line goes high.

In the latch circuit the consequence is the possible loss of data latched when VPP is rising, because the PMOS transistors 25, 26 will be off if HVPP rises before VPP. In the same way as in the translator circuit of Figure 1, a detector 29 monitors the supply line voltage and produces an output when the supply line voltage rises above the mid-range voltage VHN by more than the threshold voltage of the PMOS transistors 1, 2, 5, 6. When the detector 29 produces its output, a switching circuit 30 switches the voltage on the line HVPP from datum voltage VSS to mid-range voltage VHN. In this way the possible loss of data referred to above is avoided.

Referring now to Figure 4, detecting and switching circuitry for use in the circuit of Figure 1 as 12, 13 or in the circuit of Figure 3 as 29, 30 four PMOS FETs B1, V3, V4, B3 each having one current electrode connected to the line HVPPN. The other current electrodes of the transistors B1, V3, V4, B3 are connected respectively via NMOS transistors B2, V1, V2, B4 to ground. The gate electrode of transistor V4 is connected to the gate electrodes of transistors B1, B2 and to the junction E between the current electrodes of transistors V3, V1. The gate electrode of transistor V3 is connected to the gate electrodes of transistors B3, B4 and to the junction F between the current electrodes of transistors V4, V2. The junctions between the current electrodes of the transistors B1, B2 and B3, B4 are connected respectively to lines HVPPB and HVPP.

The gate electrodes of transistors V1, V2 are connected respectively to the outputs C, D of a RS latch constituted by NOR gates 32, 34. The inputs to the RS

latch are connected respectively to the output of a NOR gate 36 and to a line ENVPPN. One input of NOR gate 36 is connected to a node A and the other input is connected to the line ENVPPN. PMOS FETs 38, 40 are connected in parallel with their current electrodes connected between a source of potential VDD and the node A. The gate electrode of transistor 38 is connected to the line ENVPP via an inverter 42 which forms the inverse of the signal on line ENVPPN, and the gate electrode of transistor 40 is connected to ground. Node A is connected via an NMOS FET 44 to ground. A PMOS FET 46 and NMOS FETs 48, 50, 52 are connected in series between the supply line and ground. The gate electrodes of FETs 46, 48 are connected to the line HVPN, and the gate electrode of FET 50 is connected to the output C of the RS latch. The gate electrodes of FETs 44, 52 are connected to the junction between the current electrodes of transistors 50, 52.

The circuit of Figure 4 is designed to work with a charge pump (not shown) producing the high voltage VPP on the supply line. In such a case, it is highly desirable that the power consumption on the charge pump should also be limited as the detection of the voltage on the supply line requires a current.

In use the PMOS transistor 46 receives voltage VHN on line HVPN at its gate and voltage VPP at its source. As long as the supply line voltage is less than VHN, transistor 46 is 'off' and no current is supplied to transistors 48, 50, 52, 44, and the node A remains at potential VDD with transistors 38, 40 'on'. The supply line ramp from VDD to VPP is generated by the charge pump being enabled from the line ENVPP which changes from a '0' state to a '1' state. The RS latch does not change at this time.

When the supply line voltage exceeds voltage VHN (on line HVPN) by a PMOS transistor threshold voltage, transistor 46 is turned 'on' and a current flows through transistors 46, 48, 50, 52 and is amplified by transistor 44. The voltage at node A falls and causes the RS latch to

change state. The output of the RS latch is applied to transistors B1-B4 and V1-V4 which act as a voltage translator and buffer for supplying the mid-range voltage VHN to the HVPP line. A complementary voltage is generated
5 on the line HVPPB for use in other parts of the EEPROM circuit (not shown).

The output of the RS latch is applied back to transistor 50 so as to cut off the current flowing from the supply line (at Vpp), minimizing power consumption on the
10 charge pump. It may also be noted that due to the current mirror formed by the transistors 44, 52, most of the energy needed to turn the RS latch comes from the supply line VDD and not from the charge pump.

As soon as the transistor 50 is switched off, no
15 current flows into transistor 52 nor into transistor 44. As PMOS transistor 40 has its gate electrode at level VSS, the transistor is on, and node A rises to level VDD, causing the output of NOR gate 36 to change state and release the RS latch to change state as soon as ENVPPN
20 changes.

At the end of an EEPROM write operation, the line ENVPPN goes low, the charge pump is disabled by the line ENVPP which goes low (returns to its '1' state) and discharges the supply line to VDD. The detecting and
25 switching circuit of Figure 4 thus awaits the next write operation in its original state.

CLAIMS

- 5 1. A protection circuit comprising:
first transistor means of a first conductivity type;
second transistor means of a second conductivity type
opposite to that of the first transistor means and coupled to the
first transistor means;
- 10 first and second transistor protection means respectively
comprising transistors of opposite conductivity types and
coupled between the first and second transistor means; and
application means for applying to the first and second transistor
means a first voltage which changes between a high level and a
15 low level and for applying to one of the transistor protection
means a second voltage which changes from a datum level to a
predetermined level between the high and low levels as the first
voltage changes from the low level to the high level,
characterized in that
- 20 the application means comprises: detection means for
detecting when the first voltage rises by a predetermined
amount above the predetermined level; and switching means for
causing the second voltage to change from the datum level to the
predetermined level in response to detection by the detection
25 means.
2. A circuit according to claim 1 wherein said one of the
transistor protection means comprises PMOS transistors and the
predetermined amount is substantially equal to the PMOS
30 transistor threshold voltage.
3. A circuit according to claim 1 or 2 wherein the circuit
comprises a voltage translator.
- 35 4. A circuit according to claim 1, 2 or 3 wherein the circuit
comprises a latch.



5. A circuit according to any preceding claim wherein the circuit is adapted for use with an EEPROM circuit.

6. A circuit substantially as hereinbefore described with
5 reference to Figure 1, 3 or 4 of the accompanying drawings.



* C L M S *