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(54) IMPROVEMENTS IN OR RELATING TO CIRCUIT ARRANGEMENTS FOR ELIMINATING THE EFFECTS OF SWITCH CHATTER

(71) We, KABUSHIKI KAISHA SUWA SEIKOSHA, a Japanese company, of 3—4, 4-chome, Ginza, Chuo-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to circuit arrangements for eliminating the effects of switch chatter and seeks to provide improved circuits which will produce a switched signal which is substantially free of the contact chatter which almost inevitably accompanies actuation of a mechanical switch the operation of which controls the switched signal. The invention seeks to provide improved circuits which will produce switched signals free from the chatter effects accompanying operation of a signal-producing mechanical switch or relay, and which will be such as to give time coincidence between the switched signals and the operating of the mechanical switch.

With the improvement and development of semiconductor circuit techniques such circuits have become of excellent reliability. However, mechanical parts, such as mechanical switches and relays, are often used in connection with such circuits because of the relatively high cost of eliminating them altogether and substituting purely electronic non-mechanical switches throughout. However such mechanical devices are a frequent source of trouble because of contact chatter ("bounce" as it is sometimes called). At present contact chatter is commonly reduced by resorting to filtering but this expedient is far from completely satisfactory.

Figures 1 and 2 of the accompanying drawings show circuits which are commonly used for reducing the effects of switch contact "chatter". In Figure 1, S_{13} is a change over switch. The "set" and "reset" terminals of an R/S type flip-flop (R/S FF) consisting for example of OR gates 11 and

12, are respectively connected to the change-over contacts of the switch S_{13} and a signal, from which "chatter" has been largely eliminated by reason of the self-maintaining action of the R/S FF 11—12 when changed over, is taken as output from the said R/S FF. In Figure 2, in which the switch S_{22} is an on-off switch instead of a change-over one, what may be termed the "chatter signal" produced by the switch will consist of relatively high frequency signal components and these are filtered out by means of a time constant circuit comprising a resistor R_{23} and a capacitor C_{23} , and a largely chatter-free signal is taken out through a buffer circuit or amplifier 21 which may comprise, for example, a high input impedance MOS element. The resistors R_{14} , R_{15} of Figure 1 and the resistor R_{24} of Figure 2 are input current reducing resistors. In these two figures $V+$ and $V-$ are, respectively, the positive and negative terminals of a power supply source.

The arrangement of Figure 1 will not adequately eliminate chatter unless a high quality switch is used for S_{13} , while the arrangement of Figure 2 necessarily involves the provision of a resistor element and a capacitor element and the latter must be of relatively large capacity if adequate elimination of chatter is to be obtained. The need for a high quality switch in Figure 1 is an obvious practical disadvantage. So also is the need for a relatively high value capacitance in Figure 2, for in practice this means the provision of a separate capacitor (i.e. not a self-capacitance). Both these defects are serious handicaps, offering an obstacle to miniaturisation and tending to increase cost and lower reliability.

The present invention seeks to avoid these defects and to provide improved chatter eliminating circuit arrangements the circuit elements of which can easily be incorporated in integrated circuit semi-conductor structures.

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According to this invention there is provided a circuit arrangement for eliminating chatter effects produced by a signal-controlling contact switch said arrangement comprising a non-synchronous memory and a synchronous memory, means for applying the output of said switch to a "set" terminal of said non-synchronous memory, means for applying a "re-set" input to a reset terminal of said non-synchronous memory, means for applying output from said non-synchronous memory as input to said synchronous memory, means for taking chatter-free switched output from said synchronous memory, the settable period of said non-synchronous memory and the write-in period of said synchronous memory being periodically repeated with the same periodicity.

As will be more clearly seen later, one of the two memories is a non-synchronous memory which holds its state regardless of the existence of an input until signals which are opposite to each other are fed in to the two input terminals whereupon the set or reset signal will register in said non-synchronous memory. The other is a synchronous memory which is changed over to the write-in condition or to the state-holding condition synchronously with a clock input to said synchronous memory. The output from the contact switch is connected to the "set" input of the non-synchronous memory, and the output from the non-synchronous memory is connected to the write-in input of the synchronous memory. If the reset period of the non-synchronous memory, and the write-in period of the synchronous memory are generated alternately without overlapping, and if the end of the reset period, i.e. the beginning of the settable period of the non-synchronous memory precedes the beginning of the next write-in period of the synchronous memory by a predetermined time, even if the signal fed in to the "set" input of the non-synchronous memory breaks off half-way along during this preceding predetermined time, it will be held by the action of the non-synchronous memory till the commencement of the write-in period of the synchronous memory. Further, in the period in which the non-synchronous memory is reset, the previous state is held by the state-holding action of the synchronous memory. Accordingly, if the operating frequency of the two memories is suitably selected, the low frequency component and the high frequency component (the chatter) can be combined so as to remove the high frequency component (of the signal from the contact switch), leaving only the low frequency component (of said signal). In other words, the chatter signal can be removed.

Since the repeating period of the chatter signal (about 4 milli-seconds for a typical

contact) corresponds in general to several hundreds Hz or several thousands Hz (which differs in accordance with the used contact), an above-mentioned preceding time of about 10 milliseconds or more is good enough to ensure that at least one chatter pulse is encountered.

The settable period of the non-synchronous memory may be controlled by an input timing switch circuit inserted between said contact switch and the "set" input of said non-synchronous memory.

The arrangement may be such that the reset period of the non-synchronous memory and the write-in period of the synchronous memory do not overlap. This, however, is not essential to the invention and overlap may occur: indeed the said write-in period may be wholly within the said reset period.

The end of the settable period of the non-synchronous memory may precede the beginning of the write-in period of the synchronous memory by a predetermined interval of time, a chatter-free output signal correctly timed with relation to the beginning and end of the signal from the contact switch being obtained by combining the output signal from the non-synchronous memory and the output signal from the synchronous memory.

The arrangement may be such that the periodical reset period of the non-synchronous memory precedes, by a predetermined time, the periodical write-in period of the synchronous memory, said write-in period occurring during a time interval different from that in which the periodical reset period of the non-synchronous memory occurs, a chatter-free output from the synchronous memory being obtained by eliminating a signal occurring outside a fixed period determined by the timing of the signal from the contact switch.

Incorrect operating due to simultaneous application to the non-synchronous memory of a "set" input and a "reset" input may be prevented by inhibiting the "set" input timing circuit inserted between the contact switch and "set" input of said non-synchronous memory.

The invention is illustrated in and further explained in connection with Figures 3 and 4 and Figures 7 and 17 inclusive of the accompanying drawings. Figures 5 and 6 of the drawings refer to a known arrangement, these figures being provided, like Figures 1 and 2, for explanatory purposes only.

Figure 3 shows one embodiment of the invention and Figure 4 is a graphical figure explanatory of the action of Figure 3.

Referring to Figures 3 and 4, the circuit includes an R/S FF consisting of NAND gates 33 and 34 and acting as a non-syn-

chronous memory. When the switch S_{36} is closed, the "set" terminal, i.e. the input terminal of the NAND gate 33, assumes the low potential $V-$, so that the R/S FF is set. Resistor R_{37} is a bias resistor which is used because the switch S_{36} is a single contact and which, when the switch S_{36} is opened, raises the input terminal of NAND gate 33 to the high potential $V+$ so that, after the reset period next following the opening switch, the R/S FF assumes the non-set state. A periodic reset signal R_{38} is applied to the reset terminal, i.e. to the input side of the NAND gate 34. The output from the R/S ff 33-34 is fed in as a "write-in" half-bit input signal W_{39} to a delay type flip-flop (D-FF) 35. The D-FF 35 is actuated by an input clock WE_{30} , and Q output of this D-FF is taken out at OUT_{40} as a signal from which chatter has been eliminated. A half-bit signal is used for the D-FF 35 because a half-bit is sufficient to actuate this D-FF as a memory. This memory action could be obtained by using instead a master-slave type of D-FF as well known per se. The signal at the output contact of S_{36} includes chatter. Unless a special switch such as a reed switch is used for S_{36} , the duration time t_{42} (see Figure 4) of the chatter will, in general, be several tens up to several hundreds of milliseconds. The periodic time t_{41} (see Figure 4) of the chatter is likely to be several hundreds of microseconds up to several milliseconds (or, expressed in terms of frequency, between several hundred Hz to several thousand Hz).

Referring to Figure 4, when the reset signal RS_{38} of the R/S FF 33-34 falls away at the first time T_{43} , the said R/S FF returns to the settable state. The said R/S FF is then set by the signal S_{36} (which includes chatter) from the switch. Moreover, despite this chatter, the R/S FF 33-34 holds the set signal obtained at the first time T_{43} , but, because this falls outside the write-in period of the clock signal WE_{30} applied to the D-FF 35, the potential at terminal W of said D-FF cannot register until time T_{44} , when the "set" signal is written in to the said D-FF. When the R/S FF has been reset again, and even if the "set" signal then no longer exists, the D-FF having been already returned to its state-holding action, still holds the set signal which was previously written in to it. As will be seen, when the R/S FF 33-34 becomes settable at time T_{43} , if there has been a "set" signal from the output contact of switch S_{36} in the write-in period of the D-FF 35 beginning at the previous time T_{44} , the output at OUT_{40} will continue unchanged. On the other hand, if no "set" signal has been set during the above period of time, the D-FF 35 will not set at the

said following time T_{44} , and the output at OUT_{40} will return to the no-signal state.

In this way a regular chatter-free output signal can be obtained even if the signal from the switch includes chatter. Also the duration of the time T_{43} between the "fall" time T_{43} of the reset signal of the R/S FF to the "rise" time T_{44} of the next write-in period of the D-FF may be restricted to suit the periodic time of the chatter. It is, in general, good enough in practice to make the duration of T_{43} about 4 milliseconds or a little more. Owing to its principle of action, the circuit arrangements operate well to eliminate chatter however long the duration of the chatter.

The arrangement is not only a very effective one for eliminating chatter but it has the great practical advantage that all the component circuit elements (except the switch itself) can be incorporated in an integrated circuit structure. Furthermore, the number of circuit elements required is relatively so small as to involve only a very small or insignificant increase in the cost of large scale integrated circuits (LSI). The practical advantages are great, not only because of the high degree of chatter elimination and the inexpensive cost of manufacture, but also because the absence of circuit elements (such as relatively large capacitors) which cannot be incorporated in an integrated circuit structure, results in improved reliability while the elimination of the need for high quality switches without loss of good chatter elimination is a further advantage.

In some cases in which use is made of a contact signal from a switch, it is required that the ON and OFF times of the switch determine the signal times. An example of this is provided by a circuit which is required to display the instant when a switch is actuated regardless of the time taken to actuate it. Figure 5 of the accompanying drawings shows a conventional known circuit arrangement in such a case and Figure 6 of the accompanying drawings is a graphical figure explanatory of its operation. The circuit consists of a half bit D-FF 80 acting synchronously under the control of a clock signal WE_{84} , and a NAND gate 81. It produces a timing output signal DD_{83} by detecting the timing of the rise of an input signal D_{82} synchronous with the clock signal WE_{84} . The pulse width of the timing output signal DD_{83} is determined by the amount of delay in the D-FF 80, i.e. the pulse width of the clock signal WE_{84} . It is possible, in similar manner, to take out and utilise the timing of the fall of the input signal D_{82} . In the above-mentioned example, the input signal D_{82} is a signal synchronous with the clock. If the signal to be handled is an irregularly timed one not synchronous with the controlling clock signal provided in the

circuit, it is necessary to provide a synchronising circuit to make it synchronous with the clock signal. This is an obvious disadvantage making for extra cost. Another generally used conventional way of taking out the timing of an input signal is by means of a differentiating circuit including a resistor element and a capacity element. This has disadvantages similar to those of the known arrangement of Figure 2. In general, whichever of the two methods above described is employed, a circuit for detecting the timing independently of a circuit for eliminating chatter must be provided in order to detect the timing of a switch signal which includes chatter. This necessity is a serious disadvantage as regards circuit integration and cost and reliability.

The present invention makes it possible to produce a signal with complete elimination of chatter and to time the rise or fall of a switch signal in a very simple manner indeed, the timing being effected merely by the addition of a simple gate to a chatter eliminating circuit in accordance with the invention. Figure 7 shows an embodiment of the invention of this nature.

Referring to Figure 7, an R/S FF consisting of NAND gates 121 and 122 constitutes a non-synchronous memory, and half bit D-FF 123 forms a synchronous memory synchronised by a clock signal input WE 129. An input timing circuit SE₁₂₃ is inserted between the output contact of a switch S₁₂₄ and the R/S FF 121—122. For convenience of drawing the input timing circuit SE₁₂₃ is shown as incorporating a mechanical switch but in practice it would be composed of a switching element such as a MOS transistor or a bipolar transistor, controlled by an input timing control signal SC₁₂₀. The input end of the switch S₁₂₄ is connected to the low potential supply V—. R₁₂₇ is a bias resistor for the "set" input circuit of the R/S FF. RS₁₂₈ is the "reset" input signal. The output from the R/S FF 121—122 and

the negative output $\bar{Q}$ from the D-FF 123 (the write-in input terminal of which is referenced W and which has a clock signal input WE 129) are applied respectively to the input terminals of a NOR gate 140. The output SD₁₃₀ from the NOR gate 140 is a chatter free timing signal corresponding with the time during which the switch S₁₂₄ is ON.

The action is shown in Figure 8. The switch signal S₁₂₄ is fed in to the "set" input of the R/S FF 121—122 by the input timing circuit SE₁₂₃ from time T₁₃₁ to time T₁₃₂. From time T₁₃₁ to time T₁₃₃, the R/S FF is reset by the reset signal RS₁₂₈. As shown in Figure 7, when the output from the R/S FF is produced from the reset preference side, the actually effective

set input period is the period from time T₁₃₃ to time T₁₃₂. Here, where the possible period (T₁₃₁ to T₁₃₂) of the "set" input of the R/S FF overlaps the reset period (T₁₃₁ to T₁₃₃) as shown in Figure 8, the "noise" stored in the self-capacity of the wiring after the switch S₁₂₄ has been closed will be discharged by the resistor R₁₂₇ during the "reset" period. This is an advantage from the point of view of obtaining an improved signal/noise ratio. The pulse width t₁₃₆ of the output timing signal SD₁₃₀ obtained by the gate 140 from the output of the R/S FF 121—122 and the output from the D-FF 123, is the time duration between time T₁₃₅ and the write-in time T₁₃₄. The time interval between the times T₁₃₃ and T₁₃₄ may currently be selected to be about 1/4 of a second. This selection of time interval also satisfies the previously mentioned limitation due to the period of repetition of the chatter signal.

By connecting the output terminal of the switch S₁₂₄ to the high potential supply terminal V+, constituting the R/S FF by two NOR gates, constituting the gate 140 by an AND gate, and connecting the bias resistor R₁₂₇ with the low potential supply terminal V—, there is obtained a modification of Figure 7 which will produce the same output (at SD₁₃₀) which is given by Figure 7.

Figure 9 shows another embodiment of the invention, in which a somewhat simpler R/S FF, constituted by an inverter 90 and a NAND gate 91, is used. Since the "set" input is combined with the output from the inverter 90, no input bias resistor is necessary.

In other respects Figure 9 is similar to Figure 7. The output terminal of the switch S₉₅ is fed in to the "set" input of the R/S FF 90—91 through an input timing circuit SE₉₄ controlled by an input timing signal SC₉₃. RS₉₆ is a reset signal for the R/S FF. The output from the R/S FF is fed in to the write-in input W of a D-FF 92 which receives a clock signal WE₉₇. The

negative $\bar{Q}$ output from the D-FF 92 and the output from the R/S FF (and the inverter 90) are fed respectively to the inputs of a NAND gate 93 and an output timing signal free from chatter is obtained at SD₉₉. Figure 10 shows the operation of the circuit of Figure 9. The output pulse width of the timing signal SD₉₉ corresponds with the interval between time T₁₀₂ and the write-in time T₁₀₃ of the clock signal WE₉₇. As will be seen from Figure 10, the width of the output pulse SD₉₉ is ensured to be at least the predetermined time interval between the fall time T₁₀₅ of the input timing signal SC₉₃ and the write-in time T₁₀₃ of the clock signal WE₉₇. Furthermore, it is

possible to make the timing signal SD_{99} nearly coincident with the input timing of the switch signal S_{99} .

It is thus possible to take out the switch signal timing with precision as a signal from which chatter has been completely eliminated, without having to provide a special synchronising circuit for the switch signal provided that the input timing control signal, the reset signal of the non-synchronous memory and the clock signal of the synchronous memory are of equal periodicity.

Figure 11 shows another embodiment of the invention. The signal from the outer terminal of a switch S_{53} having its input terminal connected to the high potential side $V+$ of the power supply is connected to the output side of an inverter 50 forming part of an R/S FF consisting of the said inverter 50 and a NAND gate 51. When the switch is closed the output of the inverter 50, which is maintained at a low potential during the "non-set" time of the R/S FF is raised forcibly to high potential and the R/S FF assumes the "set" state. In order to reset the R/S FF, a reset signal RS_{54} is fed in to the "reset" input terminal, i.e. to the input of the NAND gate 51. The output from the R/S FF is fed into the write-in input terminal W of a half bit D-FF 52 which receives a clock input WE_{55} . A chatter free output OUT_{56} is taken from the output terminal of the D-FF 52.

Figure 12 shows the operation of the circuit shown in Figure 11. In principle the action is similar to that above described with reference to Figures 3 and 4. The switch signal from the switch S_{53} having been fed in during the interval between the time T_{57} at which the R/S FF can be set to the time T_{58} at which the D-FF 52 becomes in the write-in state is held by the said D-FF while the R/S FF is in the reset state, and the said switch signal, having been once fed in, is held by the said R/S FF until it is reset. Consequently, any chatter signal included in the switch signal is eliminated.

The circuit of Figure 11 has the advantage that the bias resistor R_{57} of Figure 3 is unnecessary because the output of the inverter 50 is connected to the low potential terminal $V-$ when there is no "set" input. This is an advantage from the point of view of integrating and simplifying the circuit.

Figure 13 shows a further embodiment of this invention. The action is generally similar to that above described with reference to Figures 3 and 4, but the circuit has the advantage of preventing incorrect action which might be caused by feeding in a "set" input and a "reset" input to the non-synchronous memory in the same period. The input timing circuit SE_{63} prevents this. The timing circuit SE_{63} is represented, for

simplicity of drawing, as including a mechanical switch but, as in the case of Figure 7, it would in practice include a switching element such as a MOS transistor or a bipolar transistor. In Figure 13 it is best to use, for SE_{63} , a P-channel MOS transistor because the input side is connected to the high potential terminal $V+$.

If a "set" signal and a "reset" signal are fed in simultaneously to the R/S FF 60—61 erroneous action could be caused if means were not provided to prevent it. Such action cannot occur with Figure 13. In Figure 13 the "reset" signal RS_{65} is on the low potential side and the output from the NAND gate 61 is on the high potential side, so that the output from the inverter 60 is on the low potential side. If the contact S_{64} is closed simultaneously with the application of a "reset" signal and a "set" signal is therefore fed in, the output from the inverter 60 will be connected to the high potential side. However, due to the provision of the input timing circuit SE_{63} controlled by an input timing control signal SC_{67} , the "set" input is inhibited while the R/S FF is in the reset state so that, even though the "set" and "reset" signals appear simultaneously, this will not cause current to flow through the inverter 60. Figure 14 shows the action. As will be seen the "set" input is inhibited by the input timing circuit SE_{63} during the period between T_{69} and T_{68} when the reset signal RS_{65} is fed in to the R/S FF. The action of eliminating chatter is similar to that of the circuits described with reference to Figures 3 and 4, and Figures 7 and 8.

The circuit of Figure 13 is a very useful one for switches in watches or other time keepers and in electronic table calculators as well as in other cases of apparatus which are required to be very compact. In order to reduce the power consumption, it is advantageous to construct a circuit as shown in Figure 13 as a complementary MOS (CMOS) circuit. Figure 15 shows in some detail the input timing circuit and the input portion of the R/S FF of an arrangement in which this is done. In Figure 15 the inverter 60 of Figure 13 is constituted by a P-channel MOS transistor T_{72} and an N-channel MOS transistor T_{73} the two transistors being connected to form a CMOS inverter by connecting the two drains together and the two gates together. It is satisfactory to use a P-channel transistor SE_{75} as the input timing switch (SE_{63} of Figure 13) because the input side of this switch is at the high potential $V+$ when switch SE_{76} is closed. In Figure 15 the input timing switch is opened and closed by a control input SC_{77} . The output point of the CMOS inverter is the common drain connection D_{74} of the P-channel and N-channel transistors. This common drain

D_{74} is connected to the input of a NAND gate (not shown in Figure 15) formed with a CMOS element, and the common gate connection is connected to the output of said NAND gate. When the potential of the common drain is raised to $V+$ side by closing the switch SE_{74} , the transition potential is determined by the ratio of the conductive impedances of the transistors T_{73} and SE_{75} . This drain potential must be raised high by an amount sufficient to actuate the NAND gate. In order to ensure this, the "ON" impedance of the P-channel MOS transistor SE_{75} must be sufficiently small in relation to that of the N-channel MOS transistor T_{73} —in practice 1/5th or less. This is also necessary to shorten the period of the current flowing transionally between the above two transistors.

If overlap between the reset signal and the set signal is eliminated completely by using, as above described, an input timing circuit SE_{63} , there is the possibility that the generation of large noise will introduce a problem of poor signal/noise ratio when the inverter 60 is inverted even if the switch SE_{76} is opened. Improved resistance to noise can be obtained, for example, by the method graphically illustrated in Figure 16. Here, as will be apparent, noise is absorbed over the interval of time when the "reset" signal RS_{96} extends beyond the input timing signal SC_{98} . In Figure 16 the line I_{100} represents the drain current of the inverter at this time. When the switch 76 is closed, the current flowing during the time t_{101} is that occurring in the overlap portion of the reset signal RS_{96} beyond the input timing signal SC_{98} . As will be seen, duration of this current flow is quite short and accordingly the effect on the total current consumption is small enough to be ignored.

Figure 17 illustrates another way of improving the resistance to noise. In Figure 17 the floating self capacity C_{113} between the input timing circuit SE_{110} and the switch S_{111} is discharged by connecting a resistor R_{112} between the output side of switch S_{111} and $V-$.

As will now be seen the invention provides simple, reliable and economical circuits which will completely eliminate switch chatter and which are such that all its circuit elements (except the troublesome switch itself, of course) can be incorporated in an integrated circuit structure. Furthermore, the number of the circuit elements required is relatively so small as to involve only small or negligible increase of cost in large scale manufacture; the switch itself does not have to be of high quality and can therefore be cheap and small; the circuitry lends itself admirably to miniaturisation and the attainment of relatively low current consumption; and reliability is improved by reason of the

avoidance of externally connected separate circuit elements and simplification of the switch.

The invention is of wide application but its advantages make it especially advantageous for the elimination of chatter effects from switches used in electronic timepieces, electronic calculators and arrangements for separating multiple digital signals.

WHAT WE CLAIM IS:—

1. A circuit arrangement for eliminating chatter effects produced by a signal-controlling contact switch said arrangement comprising a non-synchronous memory and a synchronous memory, means for applying the output of said switch to a "set" terminal of said non-synchronous memory, means for applying a "re-set" input to a re-set terminal of said non-synchronous memory, means for applying output from said non-synchronous memory as input to said synchronous memory, means for taking chatter-free switched output from said synchronous memory, the settable period of said non-synchronous memory and the write-in period of said synchronous memory being periodically repeated with the same periodicity.

2. An arrangement as claimed in claim 1, wherein the settable period of the non-synchronous memory is controlled by an input timing switch circuit inserted between said contact switch and the "set" input of said non-synchronous memory.

3. An arrangement as claimed in claim 1 or 2, wherein the re-set period of the non-synchronous memory and the write-in period of the synchronous memory do not overlap.

4. An arrangement as claimed in claim 1 wherein the end of the settable period of the non-synchronous memory precedes the beginning of the write-in period of the synchronous memory by a predetermined interval of time, a chatter-free output signal correctly timed with relation to the beginning and end of the signal from the contact switch being obtained by combining the output signal from the non-synchronous memory and the output signal from the synchronous memory.

5. An arrangement as claimed in claim 1, wherein the periodical reset period of the non-synchronous memory precedes, by a predetermined time, the periodical write-in period of the synchronous memory, said write-in period occurring during a time interval different from that in which the periodical reset period of the non-synchronous memory occurs, a chatter-free output from the synchronous memory being obtained by eliminating a signal occurring outside a fixed period determined by the timing of the signal from the contact switch.

6. An arrangement as claimed in claim



$D_{7,4}$ is connected to the input of a NAND gate (not shown in Figure 15) formed with a CMOS element, and the common gate connection is connected to the output of said NAND gate. When the potential of the common drain is raised to $V+$ side by closing the switch $SE_{7,6}$, the transition potential is determined by the ratio of the conductive impedances of the transistors $T_{7,3}$ and $SE_{7,5}$. This drain potential must be raised high by an amount sufficient to actuate the NAND gate. In order to ensure this, the "ON" impedance of the P-channel MOS transistor $SE_{7,5}$ must be sufficiently small in relation to that of the N-channel MOS transistor $T_{7,3}$ —in practice 1/5th or less. This is also necessary to shorten the period of the current flowing transitionally between the above two transistors.

If overlap between the reset signal and the set signal is eliminated completely by using, as above described, an input timing circuit $SE_{6,3}$, there is the possibility that the generation of large noise will introduce a problem of poor signal/noise ratio when the inverter 60 is inverted even if the switch $SE_{7,6}$ is opened. Improved resistance to noise can be obtained, for example, by the method graphically illustrated in Figure 16. Here, as will be apparent, noise is absorbed over the interval of time when the "reset" signal $RS_{0,6}$ extends beyond the input timing signal $SC_{0,6}$. In Figure 16 the line $I_{1,00}$ represents the drain current of the inverter at this time. When the switch 76 is closed, the current flowing during the time $t_{1,01}$ is that occurring in the overlap portion of the reset signal $RS_{0,6}$ beyond the input timing signal $SC_{0,6}$. As will be seen, duration of this current flow is quite short and accordingly the effect on the total current consumption is small enough to be ignored.

Figure 17 illustrates another way of improving the resistance to noise. In Figure 17 the floating self capacity $C_{1,12}$ between the input timing circuit $SE_{1,10}$ and the switch $S_{1,11}$ is discharged by connecting a resistor $R_{1,12}$ between the output side of switch $S_{1,11}$ and $V-$.

As will now be seen the invention provides simple, reliable and economical circuits which will completely eliminate switch chatter and which are such that all its circuit elements (except the troublesome switch itself, of course) can be incorporated in an integrated circuit structure. Furthermore, the number of the circuit elements required is relatively so small as to involve only small or negligible increase of cost in large scale manufacture; the switch itself does not have to be of high quality and can therefore be cheap and small; the circuitry lends itself admirably to miniaturisation and the attainment of relatively low current consumption; and reliability is improved by reason of the

avoidance of externally connected separate circuit elements and simplification of the switch.

The invention is of wide application but its advantages make it especially advantageous for the elimination of chatter effects from switches used in electronic timepieces, electronic calculators and arrangements for separating multiple digital signals.

WHAT WE CLAIM IS:—

1. A circuit arrangement for eliminating chatter effects produced by a signal-controlling contact switch said arrangement comprising a non-synchronous memory and a synchronous memory, means for applying the output of said switch to a "set" terminal of said non-synchronous memory, means for applying a "re-set" input to a re-set terminal of said non-synchronous memory, means for applying output from said non-synchronous memory as input to said synchronous memory, means for taking chatter-free switched output from said synchronous memory, the settable period of said non-synchronous memory and the write-in period of said synchronous memory being periodically repeated with the same periodicity.

2. An arrangement as claimed in claim 1, wherein the settable period of the non-synchronous memory is controlled by an input timing switch circuit inserted between said contact switch and the "set" input of said non-synchronous memory.

3. An arrangement as claimed in claim 1 or 2, wherein the re-set period of the non-synchronous memory and the write-in period of the synchronous memory do not overlap.

4. An arrangement as claimed in claim 1 wherein the end of the settable period of the non-synchronous memory precedes the beginning of the write-in period of the synchronous memory by a predetermined interval of time, a chatter-free output signal correctly timed with relation to the beginning and end of the signal from the contact switch being obtained by combining the output signal from the non-synchronous memory and the output signal from the synchronous memory.

5. An arrangement as claimed in claim 1, wherein the periodical reset period of the non-synchronous memory precedes, by a predetermined time, the periodical write-in period of the synchronous memory, said write-in period occurring during a time interval different from that in which the periodical reset period of the non-synchronous memory occurs, a chatter-free output from the synchronous memory being obtained by eliminating a signal occurring outside a fixed period determined by the timing of the signal from the contact switch.

6. An arrangement as claimed in claim



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5 wherein incorrect operation due to simultaneous application to the non-synchronous memory of a "set" input and a "reset" input is prevented by inhibiting the "set" input for the resetting period of said non-synchronous memory by an input timing circuit inserted between the contact switch and "set" input of said non-synchronous memory.

10 7. Chatter eliminating circuit arrangements substantially as herein described with reference to Figures 3 and 4 of the accompanying drawings; or with reference to Figures 7 and 8 of the accompanying drawings; or

with reference to Figures 9 and 10 of the accompanying drawings; or with reference to Figures 11 and 12 of the accompanying drawings; or with reference to Figures 13 and 14 of the accompanying drawings; or with reference to Figure 15, Figure 16 or Figure 17 of the accompanying drawings.

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