CLAIMS

We Claim:

1. A wafer scale active thermal interposer (ATI) device for use in testing a wafer device under test (DUT), said ATI device comprising:

a formation comprising one or more layers and comprising a plurality of thermal zones configured to apply thermal energy to a plurality of dice of said wafer DUT during said testing thereof and wherein said plurality of thermal zones corresponds to a die layout of said wafer DUT;

a first thermal zone of said plurality of thermal zones configured to apply thermal energy to a first thermal region of said wafer DUT;

a second thermal zone of said plurality of thermal zones configured to apply thermal energy to a second thermal region of said wafer DUT;

an EMI shield layer for addressing signal interference caused by said plurality of thermal zones,

wherein said second thermal zone is configured to control a temperature of said second thermal region of said wafer DUT independently of a temperature of said first thermal region,

wherein said first thermal zone is configured to control a temperature of said first thermal region of said wafer DUT independently of a temperature of said second thermal region, and

wherein said formation further comprises a plurality of thermal resistance structures located between said plurality of thermal zones, said plurality of thermal resistance structures configured to limit conductance of thermal energy between said plurality of thermal zones,

wherein said plurality of thermal resistance structures comprises a plurality of substantially similar holes formed in said ATI device,

wherein said EMI shield layer comprises conductive elements disposed in areas between said plurality of substantially similar holes.

2. The ATI device of Claim 1 wherein said plurality of thermal zones covers said plurality of dice of said wafer DUT.

3. The ATI device of Claim 1 wherein said first thermal zone corresponds to more than one die of said plurality of dice of said wafer DUT and less than said plurality of dice of said wafer DUT.

4. The ATI device of Claim 1 wherein said first thermal zone corresponds to a single die of said plurality of dice of said wafer DUT.

5. The ATI device of Claim 1 wherein said first thermal zone corresponds to a portion a single die of said plurality of dice of said wafer DUT.

6. The ATI device of Claim 1 wherein said plurality of thermal resistance structures comprises a plurality of trenches formed in said formation and disposed between said plurality of thermal zones.

7. The ATI device of Claim 6 wherein said plurality of trenches is formed completely through of said one or more layers of said formation.

8. The ATI device of Claim 6 wherein said plurality of trenches is formed partially through said one or more layers of said formation.

9. The ATI device of Claim 1 wherein said plurality of thermal resistance structures comprises a plurality of structures raised above a surface of said formation and disposed between said plurality of thermal zones.

10. The ATI device of Claim 9 wherein said plurality of thermal resistance structures comprises a same material as a surface of said formation.

11. The ATI device of Claim 1 wherein said plurality of thermal resistance structures comprises a plurality of substantially similar holes formed in said formation and disposed between said plurality of thermal zones.

12. The ATI device of Claim 1 wherein said EMI shield layer comprises conductive elements disposed in areas between a plurality of holes having non-circular cross sections.

13. A system for testing circuits of an integrated circuit semiconductor wafer, the system comprising:

a tester system for testing said circuits of said wafer; and

a test stack coupled to said tester system, said test stack comprising:

a wafer probe for contacting a first surface of said wafer and for probing individual circuits of said circuits of said wafer;

a thermal interposer device operable to contact a second surface of said wafer and comprising a plurality of heating zones corresponding to a die layout of said wafer and operable to selectively heat a plurality of regions of said wafer during said testing,

wherein said thermal interposer device comprises a plurality of thermal resistance structures disposed between said plurality of heating zones and configured to limit conductance of thermal energy between said plurality of heating zones, wherein said plurality of thermal resistance structures comprises a plurality of substantially similar holes formed in said thermal interposer device,

wherein said thermal interposer device comprises an EMI shield layer for addressing signal interference caused by said plurality of heating zones and wherein said EMI shield layer comprises conductive elements disposed in areas between said plurality of substantially similar holes;

a cold plate disposed adjacent to a surface of said thermal interposer device and operable to cool said wafer; and

a thermal controller for selectively heating and maintaining temperatures of said plurality of regions of said wafer by controlling cooling of said cold plate and by controlling selective heating of said plurality of heating zones of said thermal interposer device.

14. The system of Claim 13 wherein said plurality of thermal resistance structures comprises a plurality of trenches formed in said thermal interposer device, said plurality of trenches disposed between said plurality of heating zones of said thermal interposer device.

15. The system of Claim 14 wherein said thermal interposer device comprises one or more layers and wherein said plurality of trenches is formed completely through said one or more layers of said thermal interposer device.

16. The system of Claim 14 wherein said thermal interposer device comprises one or more layers and wherein said plurality of trenches is formed partially through said one or more layers of said thermal interposer device.

17. The system of Claim 14 wherein said plurality of thermal resistance structures comprises a plurality of structure elements raised above a surface of said thermal interposer device, said plurality of structure elements disposed between said plurality of heating zones of said thermal interposer device.

18. The system of Claim 17 wherein said plurality of thermal resistance structures comprises a same material as a surface of said thermal interposer device.

19. A system for testing circuits of an integrated circuit semiconductor wafer, the system comprising:

a tester system for testing said circuits of said wafer; and

a test stack coupled to said tester system, said test stack comprising:

a wafer probe for contacting a top surface of said wafer and for probing individual circuits of said circuits of said wafer;

a thermal interposer device operable to contact a bottom surface of said wafer and comprising a plurality of discretely controllable thermal zones, wherein each thermal zone of said plurality of discretely controllable thermal zones is operable to be discretely and selectively heated to selectively heat a corresponding area of said wafer,

wherein said thermal interposer device comprises a plurality of thermal resistance structures operable to limit thermal energy conductance between said plurality of discretely controllable thermal zones,

wherein said plurality of thermal resistance structures comprises a plurality of substantially similar holes formed in said thermal interposer device,

wherein said thermal interposer device comprises an EMI shield layer for addressing signal interference caused by said plurality of thermal zones and wherein said EMI shield layer comprises conductive elements disposed in areas between said plurality of substantially similar holes; and

a cold plate disposed under said thermal interposer device and operable to cool said wafer; and

a thermal controller for selectively heating and maintaining temperatures of areas of said wafer by controlling cooling of said cold plate and by controlling heating of said plurality of discretely controllable thermal zones of said thermal interposer device.

20. A system as described in Claim 19 wherein said wafer comprises a die layout comprising a plurality of dice and wherein further positions and shapes of said plurality of discretely controllable thermal zones are customized to said die layout of said wafer and wherein further said plurality of thermal resistance structures is disposed between said plurality of discretely controllable thermal zones.

21. A system as described in Claim 20 wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to multiple dice of said die layout of said wafer.

22. A system as described in Claim 20 wherein each thermal zone of said plurality of discretely controllable thermal zones corresponds to a single die of said die layout of said wafer.

23. A system as described in Claim 20 wherein each die of said die layout of said wafer corresponds to multiple thermal zones of said plurality of discretely controllable thermal zones of said thermal interposer device.

24. The system as described in Claim 20 wherein said thermal interposer device comprises a plurality of traces traversing said thermal interposer device and operable to selectively heat and maintain temperatures of said plurality of discretely controllable thermal zones of said thermal interposer device responsive to said thermal controller.

25. A method for testing circuits of an integrated circuit semiconductor wafer, the method comprising:

testing said circuits of said wafer using a tester system; and

in conjunction with performing said testing, selectively heating and maintaining temperatures of a plurality of areas of said wafer by using a thermal controller controlling a thermal interposer and a cold plate, both disposed in proximity of said wafer and wherein dimensions of said thermal interposer are customized for said wafer, and

wherein said thermal interposer comprises a plurality of separately controllable thermal zones wherein each thermal zone of said plurality of separately controllable thermal zones is operable to be selectively heated and temperature maintained by said thermal controller, and

wherein said thermal interposer further comprises a plurality of thermal resistance structures located between said plurality of separately controllable thermal zones, said plurality of thermal resistance structures is configured to limit conductance of thermal energy between said plurality of separately controllable thermal zones,

wherein said plurality of thermal resistance structures comprises a plurality of substantially similar holes formed in said thermal interposer device,

wherein said thermal interposer device comprises an EMI shield layer for addressing signal interference caused by said plurality of thermal zones and wherein said EMI shield layer comprises conductive elements disposed in areas between said plurality of substantially similar holes.

26. A method as described in Claim 25 wherein said wafer comprises a die layout and wherein further positions and shapes of said plurality of separately controllable thermal zones of said thermal interposer are customized to said die layout.