

18
CLOCK RE-TIMING APPARATUS
WITH CASCADED DELAY STAGES

ABSTRACT

A video clock input signal (MCK) is applied to a delay line (30) comprising a cascade connection of a plurality (T1-T19) of delay elements for providing a plurality of delayed clock signals at respective taps (T1-T15) of the delay line. A selection circuit (6), responsive to a horizontal synchronizing signal (HS) supplied thereto, couples a selected one of the taps to an output for providing a delayed output clock signal (YCK) that is edge-aligned with the synchronizing signal (HS). For reducing the number of taps required to provide a given minimum delay step resolution and a given minimum total delay for delay elements which may vary in delay, from one integrated circuit to another, the taps are spaced one element apart for a first group (T1-T13) of the delay elements and are spaced more than one element apart for at least one (T13-T16; T17-T18; T19) second group of the elements.

Figure 2