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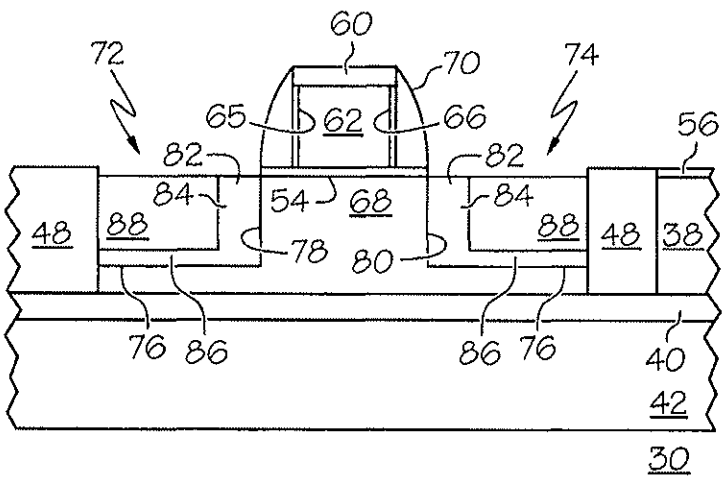
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(54) Title: STRESS ENHANCED MOS TRANSISTOR AND METHODS FOR ITS FABRICATION



(57) Abstract: A stress enhanced MOS transistor [30] and methods for its fabrication are provided. In one embodiment the method comprises forming a gate electrode [62] overlying and defining a channel region [68] in a monocrystalline semiconductor substrate [38]. A trench [72, 74] having a side surface [78, 80] facing the channel region is etched into the monocrystalline semiconductor substrate adjacent the channel region. The trench is filled with a second monocrystalline semiconductor material [82, 90] having a first concentration of a substitutional atom and with a third monocrystalline semiconductor material [88, 100] having a second concentration of the substitutional atom. The second monocrystalline semiconductor material [82, 90] is epitaxially grown to have a wall thickness along the side surface sufficient to exert a greater stress on the channel region [68] than the stress that would be exerted by a monocrystalline semiconductor material having the second concentration if the trench was filled by the third monocrystalline material alone.

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