

CLAIMS

1. A computer-implemented method, comprising:
 - receiving, at a function processing service, a request to execute source code, wherein the request is received from a requesting entity, and wherein the source code comprises instructions to perform a function;
 - determining that a hardware acceleration condition has been satisfied for the function;
 - translating the instructions in the source code into hardware-specific code corresponding to a hardware circuit;
 - configuring the hardware circuit based on the hardware-specific code;
 - causing the hardware circuit to perform the function; and
 - providing a result obtained from the hardware circuit to the requesting entity.
2. The computer-implemented method of claim 1, wherein:
 - the hardware circuit comprises a field programmable gate array (FPGA); and
 - the hardware-specific code comprises hardware description language (HDL) code corresponding to the FPGA.
3. The computer-implemented method of claim 1, wherein:
 - the hardware circuit comprises at least one of a graphics processing unit (GPU) or a digital signal processor (DSP); and
 - the hardware-specific code comprises at least one of GPU code or DSP code.
4. The computer-implemented method of claim 1, wherein:
 - the hardware circuit comprises an application specific integrated circuit (ASIC);
 - and
 - the hardware-specific code comprises hardware description language (HDL) code.
5. The computer-implemented method of claim 1, wherein determining that the hardware acceleration condition has been satisfied comprises:
 - counting a number of requests to perform the function that the function processing service receives within a time interval; and
 - determining that the number of requests exceeds a threshold value.
6. The computer-implemented method of claim 1, wherein the function belongs to a family of functions, and wherein determining that the hardware acceleration condition has been satisfied comprises:
 - counting a number of requests to perform any function within the family of functions that the function processing service receives within a time interval; and

determining that the number of requests exceeds a threshold value.

7. The computer-implemented method of claim 1, wherein determining that the hardware acceleration condition has been satisfied comprises:

determining an estimated cost savings associated with performing the function via the hardware circuit compared to performing the function via a general-purpose processor; and

determining that the estimated cost savings exceeds a threshold value.

8. The computer-implemented method of claim 1, wherein determining that the hardware acceleration condition has been satisfied comprises determining that the function is included in a function library, and further comprising adding new functions to the function library.

9. A computer-implemented method, comprising:

determining that a hardware acceleration condition has been satisfied for a first function;

configuring a hardware circuit to perform the first function;

adding the first function to a function library that is implemented in hardware circuits;

receiving, at a function processing service, a request to execute source code, wherein the source code comprises instructions to perform the first function; and causing the first function to be performed via the hardware circuit.

10. The computer-implemented method of claim 9, wherein:
 - the hardware circuit comprises a field programmable gate array (FPGA); and
 - the method further comprises translating the source code into hardware description language (HDL) code corresponding to the FPGA.

11. The computer-implemented method of claim 9, wherein:
 - the hardware circuit comprises a graphics processing unit (GPU); and
 - the method further comprises translating the source code into GPU code.

12. The computer-implemented method of claim 9, wherein:
 - the hardware circuit comprises a programmable application specific integrated circuit (ASIC); and

the method further comprises using a customer compiler to translate the source code into machine code corresponding to the programmable ASIC.

13. The computer-implemented method of claim 9, wherein:
 - the hardware circuit comprises a digital signal processor (DSP); and

the method further comprises translating the source code into DSP code.

14. The computer-implemented method of claim 9, wherein determining that the hardware acceleration condition has been satisfied comprises:

counting a number of requests to perform the first function that the function processing service receives within a time interval; and

determining that the number of requests exceeds a threshold value.

15. The computer-implemented method of claim 9, wherein the first function belongs to a family of functions, and wherein determining that the hardware acceleration condition has been satisfied comprises:

counting a number of requests to perform any function within the family of functions that the function processing service receives within a time interval; and

determining that the number of requests exceeds a threshold value.