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(54) Title: **AREA EFFICIENT REALIZATION OF COEFFICIENT ARCHITECTURE FOR BIT-SERIAL FIR, IIR FILTERS AND COMBINATIONAL/SEQUENTIAL LOGIC STRUCTURE WITH ZERO LATENCY CLOCK OUTPUT**

(57) Abstract

The invention relates to area efficient realization of coefficient block [A] or architecture [A] with hardware sharing techniques and optimizations applied to this block. The block [A] is connected to coefficient lines CLin_0, CLin_1...CLin_n and BLin_0, BLin_1,... BLin_n coming from block [E] and/or [F], to be connected to perform filtering operation or a mathematical computing operation with optimization in hardware and provides a zero latency output. The invention also gives the area minimal realization of digital filters based on coefficient block [A], when operated in bit serial fashion. The optimization techniques and structure of the present invention are good for linear digital filters typically a finite impulse response (FIR) filter, infinite impulse response filter (IIR) and for other filters and applications based on combinational logic consisting of delay element (T), multiplier (M), adder (SA) and subtractor (SS).

