

(12) 特許協力条約に基づいて公開された国際出願

(19) 世界知的所有権機関
国際事務局

(43) 国際公開日
2012 年 9 月 13 日(13.09.2012)



(10) 国際公開番号
WO 2012/120785 A1

- (51) 国際特許分類:
H01L 21/304 (2006.01) *B24B 37/24* (2012.01)
- (21) 国際出願番号: PCT/JP2012/000856
- (22) 国際出願日: 2012 年 2 月 9 日(09.02.2012)
- (25) 国際出願の言語: 日本語
- (26) 国際公開の言語: 日本語
- (30) 優先権データ:
特願 2011-048852 2011 年 3 月 7 日(07.03.2011) JP
- (71) 出願人(米国を除く全ての指定国について): 信越半導体株式会社 (Shin-Etsu Handotai Co., Ltd.) [JP/JP]; 〒1000004 東京都千代田区大手町二丁目 6 番 2 号 Tokyo (JP).
- (72) 発明者; および
- (75) 発明者/出願人(米国についてのみ): 佐々木 拓也(SASAKI, Takuya) [JP/JP]; 〒9618061 福島県西白河郡西郷村大字小田倉字大平 1 5 0 番地信越半導体株式会社 白河工場内 Fukushima (JP). 橋本浩昌(HASHIMOTO, Hiromasa) [JP/JP]; 〒9618061 福島県西白河郡西郷村大字小田倉字大平 1 5 0 番

地信越半導体株式会社 白河工場内 Fukushima (JP). 佐藤 一弥(SATO, Kazuya) [JP/JP]; 〒9618061 福島県西白河郡西郷村大字小田倉字大平 1 5 0 番地信越半導体株式会社 半導体白河研究所内 Fukushima (JP). 佐藤 歩(SATO, Ayumu) [JP/JP]; 〒9420193 新潟県上越市頸城区城野腰 5 9 6 番地 2 直江津電子工業株式会社内 Niigata (JP).

(74) 代理人: 好宮 幹夫(YOSHIMIYA, Mikio); 〒1100005 東京都台東区上野 7 丁目 6 番 1 1 号第一下谷ビル 8 F Tokyo (JP).

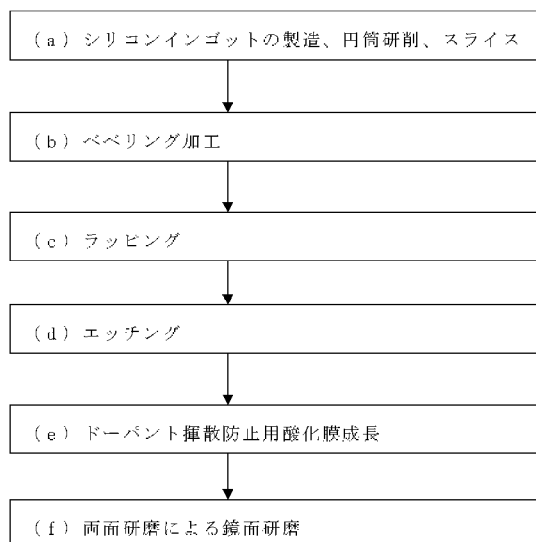
(81) 指定国(表示のない限り、全ての種類の国内保護が可能): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

[続葉有]

(54) Title: PROCESS FOR PRODUCING SILICON WAFER

(54) 発明の名称: シリコンウェーハの製造方法

【図1】



- (a) Production of silicon ingot, grinding into cylinder, and slicing
(b) Beveling
(c) Lapping
(d) Etching
(e) Deposition of oxide film for preventing dopant volatilization
(f) Mirror polishing by double-side polishing

(57) Abstract: The present invention is a process for producing a silicon wafer, characterized by including, after deposition of an oxide film on one surface of a raw silicon wafer by chemical vapor deposition, a step in which both surfaces of the raw silicon wafer are polished using, for the oxide-film surface side, a polishing cloth which is either a polishing suede cloth obtained by applying a urethane resin and then subjecting the applied urethane resin to wet-process solidification to foam the resin or a polishing velour cloth obtained by impregnating nonwoven fabric with a urethane resin and which has an Asker-C rubber hardness of 50° or higher but less than 90°, and using, for the side which has no deposited oxide film, a polishing cloth which is either a polishing cloth constituted of foam of a urethane alone or a polishing velour cloth obtained by impregnating nonwoven fabric with a urethane resin and which has an Asker-C rubber hardness of 90° or higher. Thus, by the process for silicon wafer production, a silicon wafer having a high degree of flatness can be produced while inhibiting the oxide film from suffering scratches or being reduced in thickness by polishing and while thereby maintaining the quality of the oxide film as a protective film for preventing dopant volatilization.

(57) 要約:

[続葉有]

WO 2012/120785 A1