TITLE: COMPLEMENTARY METAL OXIDE SEMICONDUCTOR TRANSISTOR TECHNOLOGY USING SELECTIVE EPITAXY OF A STRAINED SILICON GERMANIUM LAYER

ABSTRACT

A process for fabricating CMOS devices, featuring a channel region comprised with a strained SiGe layer, has been developed. The process features the selective growth of a composite silicon layer on the top surface of N well and P well regions. The composite silicon layer is comprised of a thin, strained SiGe layer sandwiched between selectively grown, undoped silicon layers. The content of Ge in the SiGe layer, between about 20 to 40 weight percent, allows enhanced carrier mobility to exist without creation of silicon defects. A thin silicon dioxide gate insulator is thermally grown from a top portion of the selectively grown silicon layer, located overlying the selectively grown SiGe layer.

Fig. 6

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