

CLAIMS:

1. A computer system, comprising:
a configuration comprising a core configurable between a single thread (ST) mode and a multithreading (MT) mode, the ST mode addressing a primary thread and the MT mode addressing the primary thread and one or more secondary threads on shared resources of the core;
and
a multithreading facility configured to control the configuration to perform a method comprising:
executing, in the primary thread in the ST mode, an MT mode setting instruction;
obtaining a number of threads requested from a location specified by the MT mode setting instruction; and
based on determining that the number of threads requested indicates multiple threads, enabling the MT mode to execute the multiple threads comprising the primary thread and the one or more secondary threads.
2. The computer system according to claim 1, wherein the MT mode setting instruction is a signal processor (SIGP) instruction from an operating system, the SIGP instruction comprising a set-MT order and a program specified maximum thread-id (PSMTID) associated with the number of threads requested.
3. The computer system according to claim 2, further comprising:
enabling the MT mode based on executing the set-MT order with a non-zero value of the PSMTID; and
remaining in the ST mode and preventing enablement of the MT mode based on executing the set-MT order with a zero value of the PSMTID.
4. The computer system according to claim 3, wherein an error indication is provided and enablement of the MT mode is prevented based on determining that the set-MT order was issued with one or more of: an invalid order, an incorrect state, and an invalid parameter.

5. The computer system according to claim 2, wherein the MT mode is disabled based on a reset or a deactivation of the configuration, and one or more secondary thread contexts and a last-set PSMTID are retained for a non-clearing reset or zeroed for a clearing reset.

6. The computer system according to claim 5, wherein the configuration defaults to the ST mode upon the reset or the deactivation or activation of the configuration.

7. The computer system according to claim 1, wherein an executing program is provided with an indication of a maximum thread-id based on a response to a service call (SERVC) instruction or a store system information (STSI) instruction.

8. The computer system according to claim 1, further comprising a plurality of configurations, wherein each of the configurations of the computer system is configurable with a different number of maximum thread-ids to support a simultaneously enabled different number of threads at each of the configurations.

9. A computer-implemented method for dynamic enablement of multithreading in a configuration comprising a core configurable between a single thread (ST) mode and a multithreading (MT) mode, the ST mode addressing a primary thread and the MT mode addressing the primary thread and one or more secondary threads on shared resources of the core, the method comprising:

executing in the primary thread in the ST mode, an MT mode setting instruction;

obtaining a number of threads requested from a location specified by the MT mode setting instruction; and

based on determining that the number of threads requested indicates multiple threads, enabling the MT mode to execute the multiple threads comprising the primary thread and the one or more secondary threads.

10. The method according to claim 9, wherein the MT mode setting instruction is a signal processor (SIGP) instruction from an operating system, the SIGP instruction comprising a

set-MT order and a program specified maximum thread-id (PSMTID) associated with the number of threads requested.

11. The method according to claim 10, further comprising:
enabling the MT mode based on executing the set-MT order with a non-zero value of the PSMTID; and
remaining in the ST mode and preventing enablement of the MT mode based on executing the set-MT order with a zero value of the PSMTID.
12. The method according to claim 11, wherein an error indication is provided and enablement of the MT mode is prevented based on determining that the set-MT order was issued with one or more of: an invalid order, an incorrect state, and an invalid parameter.
13. The method according to claim 10, wherein the MT mode is disabled based on a reset or a deactivation of the configuration, and one or more secondary thread contexts and a last-set PSMTID are retained for a non-clearing reset or zeroed for a clearing reset.
14. The method according to claim 9, wherein an executing program is provided with an indication of a maximum thread-id based on a response to a service call (SERVC) instruction or a store system information (STSI) instruction.
15. The method according to claim 9, further comprising a plurality of configurations, wherein each of the configurations of the computer system is configurable with a different number of maximum thread-ids to support a simultaneously enabled different number of threads at each of the configurations.
16. A computer program product for implementing dynamic enablement of multithreading in a configuration comprising a core configurable between a single thread (ST) mode and a multithreading (MT) mode, the ST mode addressing a primary thread and the MT mode addressing the primary thread and one or more secondary threads on shared resources of the core, the computer program product comprising:

a computer readable storage medium having program instructions embodied therewith, wherein the computer readable storage medium is not a signal, the program instructions readable by a processing circuit to cause the processing circuit to perform a method comprising:

executing in the primary thread in the ST mode on the core of the configuration, an MT mode setting instruction;

obtaining a number of threads requested from a location specified by the MT mode setting instruction; and

based on determining that the number of threads requested indicates multiple threads, enabling the MT mode to execute the multiple threads comprising the primary thread and the one or more secondary threads.

17. The computer program product according to claim 16, wherein the MT mode setting instruction is a signal processor (SIGP) instruction from an operating system, the SIGP instruction comprising a set-MT order and a program specified maximum thread-id (PSMTID) associated with the number of threads requested.

18. The computer program product according to claim 17, further comprising: enabling the MT mode based on executing the set-MT order with a non-zero value of the PSMTID; and

remaining in the ST mode and preventing enablement of the MT mode based on executing the set-MT order with a zero value of the PSMTID.

19. The computer program product according to claim 18, wherein an error indication is provided and enablement of the MT mode is prevented based on determining that the set-MT order was issued with one or more of: an invalid order, an incorrect state, and an invalid parameter.

20. The computer program product according to claim 17, wherein the MT mode is disabled based on a reset or a deactivation of the configuration, and one or more secondary thread contexts and a last-set PSMTID are retained for a non-clearing reset or zeroed for a clearing reset.