



Semiconductor memory having an arrangement of memory cells

The invention relates to a semiconductor memory having an arrangement of memory cells which are connected to first
5 lines, which run parallel to one another, and to second lines, which run parallel to one another and perpendicular to the first lines, and each have a storage capacitor and a vertical selection transistor, within the arrangement of memory cells a memory cell being connected to each
10 crossover point between a first line and a second line. In particular, DRAMS (dynamic random access memories) or other volatile semiconductor memories are constructed in this way. They have a memory cell array, whose memory cells each have a storage capacitor for storing charges
15 and a selection transistor. Each memory cell is addressed by a first line (for example a bit line) and a second line (e.g. a word line) running perpendicular to the first line over the semiconductor substrate. By altering the electrical potentials on the first and/or the second line,
20 it is possible to switch the selection transistor, so that a certain quantity of charge can flow into or out of the storage capacitor.

Selection transistors are usually designed as MOSFETs
25 (metal oxide semiconductor field-effect transistors), the



first source/drain electrode of which is connected to a bit line and the gate electrode of which is connected to a word line. The second source/drain electrode leads to the storage capacitor. In view of the increasing integration density of future semiconductor memories, the selection transistors are preferably designed as vertical transistors whose two source/drain electrodes are arranged one above the other vertically with respect to the substrate surface. As a result, the selection transistor requires only a minimal substrate base area. In the case of vertical selection transistors the gate electrode is arranged in a manner only slightly offset laterally and at a central level between the two source/drain electrodes of the transistor. Planar selection transistors by contrast, whose electrodes are arranged laterally next to one another on the substrate surface require a significantly larger substrate base area.

Despite the use of vertical selection transistors, the integration density of a semiconductor memory cannot be increased arbitrarily since a minimum width of bit lines and word lines is necessary on account of defraction phenomena during lithographic patterning and since, moreover, the storage capacitor for example a trench capacitor, requires a certain substrate base area in order

to be able to store sufficiently high quantities of charge. Although the storage capacitors that are usually designed in the form of a deep trench have a very high aspect ratio and extend very deep into the substrate, leakage currents nonetheless lead to a rapid escape of stored quantities of charge precisely in the case of volatile semiconductor memories, so that, in order to increase the capacitance, the largest possible base area is chosen for a buried storage capacitor in the lateral direction as well. Therefore, the base area of the trench capacitors concomitantly determines the integration density of a semiconductor memory.

In the cell array of a semiconductor memory, storage capacitors are arranged, with regard to the base area of the semiconductor substrate, in direct proximity to the crossover point between the bit line and the word line which address the relevant memory cell. In accordance with the network-type arrangement of mutually parallel bit lines and mutually parallel word lines running perpendicular to the bit lines over or in the substrate base area, the memory cells and thus also the storage capacitors are arranged for example in chessboard-like fashion on the substrate. Terminals for the word lines crossing the bit lines are provided at at least one edge

of the cell array. In a real cell array architecture, by contrast, the bit lines no longer cross all the word lines, but rather only some of them, in order to keep down the bit line capacitance and to facilitate a read-out of an item of information from a memory cell. Various groups of word lines therefore cross different groups of bit lines, so that a plurality of cell blocks are produced instead of a single cell array. Word lines and bit lines require complicated driver circuits, i.e. word line drivers or evaluation circuits for bit lines.

Conventionally, the size and number of these circuits can be altered only if the number of word and bit lines is simultaneously altered.

15 In a conventional semiconductor memory, the widths of the bit and word lines and their distances from one another are chosen to be as small as possible in accordance with the wavelength used for the lithographic exposure. The trench capacitors are made as wide as possible in order to be able to store large quantities of charge. In order to utilize the available substrate base area in the best possible manner, a memory cell, that is to say a storage capacitor, is provided in direct proximity at each crossover point between a bit line and a word line. In order to read out stored information, provision is made of

evaluation circuits e.g. with dummy cells in order to be able to assign a read-out memory information item to a digital value zero or one.

5 With the arrangement of memory cells at each crossover point between bit line and word line in a conventional semiconductor memory described above, it is no longer possible to accommodate further structures in the cell array between the mutually adjacent bit lines or mutually
10 adjacent word lines, since their distance from one another and their width have already been optimized in accordance with the respective optical resolution limit.

The object of the present invention is to provide a
15 semiconductor memory in which, without altering the lateral distance between adjacent storage capacitors, it is possible to form additional structures, for instance control lines between adjacent first or second lines.
Furthermore, the object of the invention is to alter the
20 number of memory cells which are addressed in a connected manner per word line or per bit line, and thus to create the potential for a saving of area on a semiconductor substrate.

In the case of a semiconductor memory of the type mentioned in the introduction, this object is achieved by virtue of the fact that each of the second lines connects together memory cells whose storage capacitors are
5 arranged alternately on both sides of the respective second line in a manner laterally offset relative to said respective second line.

According to the invention, the storage capacitors are
10 arranged in the form of a grid in which, unlike conventional practice, capacitors that are the most closely adjacent to one another are not offset with respect to one another in the direction of a bit line or a word line, but rather obliquely, preferably diagonally
15 with respect to the course of said directions. The distance between the storage capacitors that are the most closely adjacent to one another is intended to remain unchanged since it has a determining influence on the cell spacing. The diagonal arrangement of trench capacitors
20 that are the most closely adjacent to one another enables a novel geometry in the arrangement of the memory cells. According to the invention, each of the second lines connects together memory cells whose storage capacitors are arranged alternately on both sides of the respective
25 second line in a manner laterally offset relative to said

respective second line. Whereas conventionally one row of memory cells is arranged centrally below a second line, according to the invention each individual line of the second lines is connected to memory cells whose storage capacitors are arranged alternately on the left of said line and on the right of said line in a laterally offset manner. In this manner, a single second line can be used to address two rows of memory cells whose storage capacitors are at the same distance from one another as in a conventional semiconductor memory. The number of second lines required can thus be reduced. Since the cell density has remained unchanged on account of the unchanged distance between storage capacitors that are the most closely adjacent to one another, the distances between the second lines are greater in the case of the semiconductor memory according to the invention than is conventionally the case. This has the advantage, on the first one hand, that fewer drivers are necessary for driving the second lines; on the other hand, insofar as is permitted by the lithographic resolution limit for the first and second lines, it is possible to arrange additional lines, for instance control lines or auxiliary lines, between mutually adjacent second lines. By way of example, it is conceivable to equip the word lines in each case with an additional parallel line in order to increase their

conductivity. The number of drivers required for the second lines is not increased as a result.

In the semiconductor memory according to the invention,
5 the number of memory cells which are connected to a word line or to a bit line is altered compared with a conventional semiconductor memory. The altered linear ratio of the two dimensions of the memory cell array achieved by virtue of the arrangement according to the
10 invention creates an additional potential for saving area on a semiconductor substrate. Moreover, an alteration - according to the invention - of the number of memory cells connected per word or bit line affords the possibility of optimizing the length and the capacitance of word lines
15 and bit lines. By way of example, precisely in the context of decreasing feature sizes, circuits may be dimensioned for evaluating extremely weak signals. In conjunction with a reduction of the capacitor spacing itself, the arrangement according to the invention affords more
20 complex optimization possibilities.

It is preferably provided that any two memory cells whose storage capacitors are the most closely adjacent to one another are always connected to two mutually adjacent
25 first lines. Although the storage capacitors that are the

most closely adjacent to one another are connected to the same second line and are laterally offset with respect thereto in opposite directions perpendicular to the course of these second lines, the memory cells of these storage
5 capacitors are still connected to different first lines, so that individual memory cells can be addressed.

It is preferably provided that any two memory cells which are connected to the same first line and whose storage
10 capacitors are adjacent to one another along said first line are always connected to two mutually adjacent second lines, preferably ones that are the most closely adjacent to one another. Although every second line addresses two rows of memory cells, of which, by way of example, one row
15 is arranged on the left of said line and the other row is arranged on the right of said line each memory cell of one of these rows is connected to a respectively different first line. Although two rows of memory cells always lie between adjacent second lines on account of the diagonally
20 arranged chessboard-like pattern of storage capacitors that are the most closely adjacent to one another, those memory cells which are connected to the same first line and are adjacent along said first line are connected to second lines that are directly adjacent to one another.

It is preferably provided that mutually adjacent second lines are arranged in a manner offset with respect to one another by twice as large a distance as first lines that are the most closely adjacent to one another. This

5 embodiment exploits the fact that the second lines which connect together two rows of memory cells according to the invention are required in a smaller number than in the case of a conventional semiconductor memory. As a result, it is possible to increase their distances from one

10 another. Preferably, additional lines for instance control lines or auxiliary lines can be arranged between the second lines that are now arranged at a greater distance from one another. Provided that the distance between storage capacitors that are the most closely adjacent

15 remains unchanged relative to a conventional semiconductor memory, the distance between the first lines is correspondingly reduced. For the first lines and their distance from one another, an additional reduction of the resolution limit is necessary in order to pattern the

20 additional lines between the mutually adjacent second lines. The distance between the storage capacitors that are the most closely adjacent to one another remains unchanged however. In the case of a chessboard-like arrangement of the memory cells with a square memory cell

25 base area and a cell grid rotated diagonally, i.e. for

instance through 45° , the distance between second lines that are the most closely adjacent is exactly twice as large as the distance between first lines that are the most closely adjacent; therefore, an additional line can
5 in each case be patterned between the second lines.

It is preferably provided that the first lines are bit lines and the second lines are word lines. A single word line can then address twice as many memory cells per
10 lines. This fits in very well with the trend toward making the bit line significantly shorter than the word lines anyway. In this way, cell blocks which have significantly more bit lines than word lines can be arranged on a rectangular base area whose edge ratio (the ratio of the
15 edge lengths of the longer to the short edge) is significantly smaller than in the case of a conventional semiconductor memory.

It is preferably provided that the storage capacitors of
20 the memory cells connected to a single word line are arranged alternately on one side of said word line and on the other side of said word line. Accordingly, the memory cells connected to a single word lines are offset alternately on the left and right with respect to the word
25 line. Consequently, the word line runs in the center

between two rows of memory cells which are both addressed by this single word line.

As an alternative, it is provided that the first lines are word lines and the second lines are bit lines. In this embodiment additional lines running parallel to the bit lines can be patterned between mutually adjacent bit lines.

It is preferably provided that storage capacitors that are the most closely adjacent to one another form a diagonal grid relative to the course of the first lines and relative to the course of the second lines. The distances between the word lines and between the bit lines are chosen such that they have different magnitudes for word lines and for bit lines, as a result of which the storage capacitors can be shifted such that their positions form a square diagonal grid with respect to the course of the word lines and of the bit lines.

20

The storage capacitors are preferably trench capacitors buried in a semiconductor substrate. The capacitors arranged in a deep trench are fabricated by a procedure in which firstly the capacitor dielectric is deposited into a deep trench, on the trench wall, and a filling is

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subsequently introduced as inner capacitor electrodes. The outer electrode is formed by an indiffused layer in the doped semiconductor substrate surrounding the deep trench.

- 5 As an alternative to this, film capacitors stacked above the semiconductor substrate may be provided.

The selection transistors are preferably MOSFETs; their gate electrodes are usually connected to the word lines.

- 10 The upper source/drain electrodes of the vertical selection transistors are connected to the bit lines; the lower source/drain electrodes are conductively connected to the inner electrode of the capacitor.

- 15 The semiconductor memory is preferably a volatile semiconductor memory, in particular a DRAM.

The invention is described below with reference to figures 1 to 5, in which:

20

Figure 1 shows a plan view of a semiconductor memory in a schematic illustration,

- Figure 2 shows a cross section through a memory cell of a
25 semiconductor memory,

Figure 3 shows a conventional semiconductor memory,

Figure 4 shows a first embodiment of a semiconductor
5 memory according to the invention, and

Figure 5 shows a second embodiment of a semiconductor
memory according to the invention.

10 Figure 1 shows a semiconductor memory having a
multiplicity of memory cells 5, which are connected to one
another in a rowwise by first lines, for instance bit
lines 1, and second lines for instance, word lines. An
evaluation circuit region 7 is illustrated schematically
15 outside the memory block 15. An evaluation circuit
evaluates the signal read from a memory cell as a digital
1 or 0 and may have, for example, a dummy bit line 9 with
dummy memory cells 8. When reading from a memory cell 5,
it is possible to effect the evaluation of the read-out
20 quantity of charge with a digital bit value for example by
means of the comparison with a data value read from a
dummy cell 8. In this case, an evaluation unit (not
illustrated) drives the dummy bit line 9 and the
respective driving bit line 1.

Figure 2 shows the typical construction of a memory cell, which has a storage capacitor arranged in a deep trench, i.e. trench capacitor 3. In the trench, the selection transistor 4 of the memory cell 5 is arranged above the storage capacitor 3. If the selection transistor is a MOSFET, it has an upper and a lower source/drain electrode 11, 12, between which a channel region is arranged. A word line 2, forming the gate electrode of the selection transistor, runs laterally beside the channel region. A thin insulator layer is arranged between the gate electrode and the channel region; through electrical induction it is possible to form a channel which opens the transistor and charges or discharges the capacitor 3.

The upper electrode 11 is connected to a bit line 1 running perpendicular to the word line 2 over the substrate surface.

A semiconductor memory has a large number of the memory cell illustrated in the cross-sectional view in figure 2. Figure 3 shows a schematic plan of a conventional semiconductor memory whose bit lines 1 and word lines 2 cross one another. A memory cell 5 in accordance with figure 2 or in a different embodiment known from the prior art is arranged at each point of intersection. In the case

of trench capacitors, the storage capacitors 3 are usually situated centrally below the respective word line or always offset in the same direction (upward in figure 3) with respect to the word line.

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Figure 4 shows a schematic plan of a semiconductor memory according to the invention in a first embodiment, in which the first lines are bit lines and the second lines are word lines. The semiconductor memory has a grid of storage
10 capacitors 3 in which the path between trench capacitors 3 that are the most closely adjacent to one another is rotated through 45° with respect to the course, i.e. the direction, of the bit lines 1 and word lines 2, but is of the same size in terms of its magnitude as in figure 3.

15 Therefore, the memory cell density is of the same size as in figure 3. However, the way in which the memory cells are connected up to one another is different in the two figures. In figure 4, each word line 2 is connected to two rows of memory cells 5 parallel to the word line. The
20 memory cells 3 connected to a single word line 2 in each case are arranged in the form of a zigzag line alternately above and below the word line in figure 3, i.e., with regard to the substrate surface, on the left and on the right of the word line 2 in a manner offset with respect
25 thereto, as a result of which, with the quantity of word

lines remaining the same, a word line can address more memory cells than in the case of a conventional semiconductor memory. As in the case of a conventional semiconductor memory, in figure 4, too, two memory cells 5 which are connected to the same bit line 1b and are adjacent to one another along said bit line 1b are connected to different word lines 2a that are the most closely adjacent to one another so that a preferably individual driving of in each case only a single memory cell is also possible with the semiconductor memory according to the invention. The storage capacitors 3c of the memory cells 5a connected to a single bit line are arranged in an offset manner either all on the right or all on the left of the word line. Consequently, storage capacitors 3a and 3b, respectively, that are the most closely adjacent to one another are always connected to two bit lines 1a that are the most closely adjacent. The grid dimension of the word lines 2 is twice as large as that of the bit lines 1, so that an additional line can in each case be patterned between the word lines in order, for example in the case of very long word lines, to increase the conductivity thereof.

Figure 5 shows a further embodiment of a semiconductor memory according to the invention in schematic plan view,

in which word lines and bit lines are interchanged with one another with regard to the arrangement of the memory cells. Although the bit lines are still connected to the upper source/drain electrodes of the memory cells 5 and the word lines also still form the gate electrodes of the selection transistors, the bit lines are nonetheless connected to a larger number of memory cells 5 per bit line quantity in the case of the block of memory cells illustrated in figure 5 than in the case of a convention semiconductor memory in accordance with figure 3. The trench capacitors 3 are situated alternately on the right and on the left, i.e. offset upward and downward with respect to the bit line 2 in figure 5, so that each bit line 2 addresses two rows of memory cells. The word lines 1 are connected to a smaller number of memory cells.

Compared with the semiconductor memory in accordance with figure 4, the embodiment in accordance with figure 5 has the advantage that, given a predetermined number of memory cells to be connected to a bit line, the bit line can be made particular short. On the other hand, the embodiment in accordance with figure 4 has the advantage that only few word lines are required, so that only a small number of word line drivers are necessary as well, as a result of

which base area is saved on the semiconductor substrate
16.

Reading from a semiconductor memory in accordance with
5 figure 4 or figure 5 is effected with the aid of
evaluation circuits as in a conventional semiconductor
memory.

In particular, volatile semiconductor memories such as
10 preferably DRAMs can be designed in the manner according
to the invention.

List of reference symbols

	1	first line
	2	second line
5	3	storage capacitor
	4	selection transistor
	5	memory cell
	7	evaluation circuit region
	11	upper source/drain electrode
10	12	lower source/drain electrode
	13	gate electrode
	15	memory cell array
	16	semiconductor substrate

Patent claims

1. A semiconductor memory having an arrangement of memory cells (5) which are connected to first lines (1),
5 which run along a first direction, and to second lines (2), which run along a second direction and which cross the first lines (1), and each have a storage capacitor (3) and a vertical selection transistor (4), within the arrangement of memory cells a memory cell (5) being
10 connected to each crossover point between a first line (1) and a second line (2),
characterized in that
each of the second lines (2) connects together memory cells (5) whose storage capacitors (3b) are arranged
15 alternately on both sides of the respective second line (2) in a manner laterally offset relative to said respective second line (2).

2. The semiconductor memory as claimed in claim 1,
20 characterized in that
any two memory cells (5) whose storage capacitors (3a) are the most closely adjacent to one another are always connected to two mutually adjacent first lines (1a).

25 3. The semiconductor memory as claimed in claim 1 or 2,

characterized in that

any two memory cells (5a) which are connected to the same
first line (1b) and whose storage capacitors (3c) are
adjacent to one another along said first line (1b) are
5 always connected to two mutually adjacent second lines
(2a).

4. The semiconductor memory as claimed in one of claims
1 to 3,

10 characterized in that

mutually adjacent second lines (2) are arranged in a
manner offset with respect to one another by twice as
large a distance (d2) as first lines (1) that are the most
closely adjacent to one another.

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5. The semiconductor memory as claimed in one of claims
1 to 4,

characterized in that

the first lines (1) are bit lines and the second lines (2)
20 are word lines.

6. The semiconductor memory as claimed in claim 5,
characterized in that

the storage capacitors (3) of the memory cells (5)

25 connected to a single word line (2) are arranged

alternately on one side of said word line (2) and on the other side of said word line (2).

7. The semiconductor memory as claimed in one of claims
5 1 to 4,

characterized in that

the first lines (1) are word lines and the second lines
(2) are bit lines.

10 8. The semiconductor memory as claimed in one of claims
1 to 7,

characterized in that

storage capacitors (3b) that are the most closely adjacent
to one another form a diagonal grid relative to the course
15 of the first lines (1) and relative to the course of the
second lines (2).

9. The semiconductor memory as claimed in one of claims
1 to 8,

20 characterized in that

the storage capacitors (3) are trench capacitors buried in
a semiconductor substrate (8).

10. The semiconductor memory as claimed in one of claims
25 1 to 9,

characterized in that

the selection transistors (4) are MOSFETs whose gate electrodes (6) are connected to the word lines (2).

5 11. The semiconductor memory as claimed in one of claims 1 to 10,

characterized in that

the semiconductor memory is a dynamic random access memory.