

ADIABATIC FLIP-FLOP AND MEMORY DESIGN**CROSS REFERENCE TO RELATED APPLICATION**

[0001] This application claims priority to United States Provisional Patent Application No. 63/626,904, filed January 30, 2024, the disclosure of which is hereby incorporated by reference in its entirety.

BACKGROUNDField of the Invention

[0002] The present invention relates to resonators, and the methods of reducing dissipation to heat called Adiabatic Logic. Specifically, the present invention relates to using Bennett clocking to supply energy to digital circuits.

Description of Related Art

[0003] In Bennett clocking, a sequence of ramping clocks supply energy to the circuit. The system starts in the Null state where all phases are low. Each phase ramps up sequentially to its active state over a time period, t_o , delivering energy to the reversible logic. When all the phases are ramped up, the system is in its Active State. Next, each phase ramps back down over a period, t_o , recovering energy from the reversible logic. When all the phases have ramped down, the system is back in its Null state. Information regarding Adiabatic Logic can be found in U.S. Patent No. 11,488,660 and International Publication No. WO 2023/250007, the contents of both of which are incorporated herein by reference.

[0004] In order to realize a large over-all system power savings in a computational system the power dissipation of the Bennett clocking circuit must also be considered. Reversible logic offers the possibility of reusing the energy used in computation, but the Bennett power clock circuit must provide energy to the logic circuit(s) during the rising edge of the clock, then take back energy at the falling edge of the clock. In this way the energy is stored in the clock generator until it is given out to the logic circuit(s) again on the next clock cycle, so that the energy can be reused multiple times instead of being dissipated to heat in just one clock cycle as in conventional Complementary MOSFET logic (CMOS).

[0005] One way to implement a system that can perform the sequence of taking energy in, storing it, and then outputting energy is to use a resonant circuit or resonator. Herein, the terms "resonant circuit" and "resonator" may be used

interchangeably. A resonator can be viewed as a system that moves energy between two storage elements in a periodic fashion. The most commonly understood electrical resonator is the LC resonator where energy is alternately stored in the inductor in a magnetic field and in the capacitor as an electric field. In the ideal parallel resonator, at the resonant frequency, the impedance of the combination of the inductor and capacitor goes to infinity, and at steady state, no energy is drawn from the AC power supply. In reality, there are resistors or resistances associated with the circuit that lead to dissipation to heat of some of the energy moving through the elements of the LC resonator. A simple set of parasitic resistances includes the output resistance of the power supply, R_1 , which dissipates some of the energy leaving the supply, and the parasitic resistance of the inductor, R_2 , which dissipates some of the energy stored in the inductor.

[0006] At resonance, R_2 dissipates some energy to heat as the energy moves between the inductor and the capacitor. To quantify the effect of this dissipation, a figure of merit, the quality factor $Q=E_L/E_d$ is introduced which is the ratio of the total energy stored in the inductor, E_L , over the energy dissipated in each cycle, E_d . In an ideal resonator with $R_2 = 0\Omega$ the quality factor Q is infinite. For the realistic resonator some energy is still drawn from the power supply at steady state resonance since the impedance of the resonator does not go to infinity due to the losses in R_2 .

[0007] In an adiabatic reversible computing system using a resonant clock, the logic circuit becomes part of the resonator. The logic circuit forms a capacitive load comprised of the gate capacitances of the transistors making up the logic gates. The combined capacitance of all of these gates may be represented by the capacitor C of the resonator, and the parasitic resistance of the interconnect on the logic chip may be lumped together and represented by the resistance R_2 . With this model of the logic circuit, the Q of the resonator includes not just losses in the inductor but also losses in the logic chip as well. At resonance this resonator takes on a high impedance as energy is moved between the logic circuit represented by the capacitor C and the inductor L . The only energy that is drawn from the power supply is that necessary to make up the energy lost in the resonator on each cycle due to resistive losses that impose a finite Q . In this way the overall system energy dissipation is reduced as compared to a conventional CMOS system.

SUMMARY OF THE INVENTION

[0008] Provided herein is a circuit that uses four quadrature resonators, Res 1- Res 4, each delayed by a phase of $\pi/2 = 90^\circ$, to generate the nested set of both positive and negative going ramps.

[0009] Also provided herein is a circuit that uses an array of resonators to construct an arbitrary waveform using the principle of the Fourier series.

[0010] Further non-limiting embodiments are set forth in the following numbered clauses:

[0011] 1. A method, comprising:

[0012] (a) in a circuit with at least four quadrature resonators delayed by a phase of $\pi/2 = 90^\circ$, wherein the at least four quadrature resonators generate a set of both positive and negative going ramps, holding an output clock line initially at zero;

[0013] (b) connecting the output clock line to at least one of the at least four quadrature resonators as the output clock line crosses zero;

[0014] (c) disconnecting the output clock line from the at least one resonator after the at least one resonator ramps up to maximum voltage;

[0015] (d) holding the output clock line constant for a number of resonator periods; and

[0016] (e) reconnecting the output clock line to the at least one resonator when the at least one resonator ramps down.

[0017] 2. A method, comprising: forming a Bennett phase based on Fourier components, wherein approximately ten harmonics are used to construct an arbitrary waveform, and wherein the ten harmonics comprise:

[0018] at least one resonator for each of the ten harmonics; and

[0019] a control circuit that generates master waveforms to drive the resonators.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] FIG. 1 shows a resonator output and desired Bennett clock waveform for a single positive-going phase.

[0021] FIG. 2 shows a block diagram of a resonator based clocking system.

[0022] FIG. 3 shows a block diagram of a delay-locked loop.

[0023] FIG. 4 shows an embodiment of distribution circuitry for one Bennett clock phase, comprised of a transmission gate and two transistors.

[0024] FIG. 5 shows a timing diagram of the signals needed to operate the Control Logic.

[0025] FIG. 6 shows a block diagram of the Control Logic for the Distribution Circuit.

[0026] FIG. 7 shows a diagram of phase control circuitry used to generate the signals needed for the distribution circuits.

[0027] FIG. 8a shows a 10-harmonic waveform that is suitable to serve as the positive Bennett phase 1.

[0028] FIG. 8b shows an example of a 12 phase Bennett clock formed with 10 harmonics.

[0029] FIG. 9a shows a Bennett clock generator with 10 harmonics comprised of 10 resonators and 10 master oscillators.

[0030] FIG. 9b shows a simplified circuit having 10 resonators but only one master waveform generator.

[0031] FIG. 10a shows a top view of a multispectral piezoelectric contour mode resonator.

[0032] FIG. 10b shows a cross-section of a multispectral piezoelectric contour mode resonator.

[0033] FIG. 10c shows a schematic view of the energy reflectors placed at the end of each anchor.

[0034] FIG. 11a shows a Phase Control circuit.

[0035] FIG. 11b shows an output waveform.

DETAILED DESCRIPTION

[0036] This disclosure details two implementations of circuits to use resonators to generate energy recovering Bennett clocks. In the first implementation, four quadrature resonators Res1 – Res4, each delayed by a phase of $\pi/2 = 90^\circ$, are used to generate the nested set of both positive and negative going ramps. The fundamental principle is to use portions of a sinusoidal waveform as the rising and falling ramps of the Bennett clock. FIG. 1 shows the sinusoidal output of a resonator, dotted line. To form a Bennett clock phase shown the output clock line is initially held at zero and then connected to the resonator as its output crosses zero on its rising edge. The Bennett clock line remains connected to resonator as it ramps up to its maximum voltage and is then disconnected. The Bennett clock line is held constant for some number of resonator periods, then is reconnected to the resonator as it ramps down, then is disconnected at zero and held at zero as the resonator output crosses zero. With this sequence the resonator provides energy as it ramps up and receives energy as it ramps down. FIG. 2 shows a schematic block diagram of the system having eight

bipolar Bennett phases $\Phi 1$ through $\Phi 8$. Using the approach in FIG. 1, the eight positive going and eight negative going phases can be generated using four resonators.

[0037] A Master Digital Clock sets the timing for the clocking system. The period of the Master Digital Clock (T_{MC}) is equal to the time of the ramp phase, t_0 and/or t_1 . The full period of the Bennett clock is given in Equation 1:

$$T_{Bennett} = (2N_{Phase} + N_{Active} + N_{Null})T_{MC} \quad (1)$$

where $T_{Bennett}$ is the total period, N_{Phase} is the number of Bennett phases, N_{Active} is the number of clock cycles that the system is held in the active state, N_{Null} is the number of clock cycles that the system is held in the Null state. The period of the Master Digital Clock (T_{MC}) sets the time step of the clocking system, and is the ramping time of each Bennett clock phase, and is $\frac{1}{4}$ of the period T_{osc} of the resonators.

$$T_{osc} = 4T_{MC} \quad (2)$$

[0038] A delay-locked loop (DLL) is used to generate a four-phase master clock, $M\Phi 1 - M\Phi 4$, where each phase is shifted by 90° . The outputs of the DLL are digital signals, but with simple filtering to the fundamental frequency they can be used to drive the resonators, Res1 – Res4. The Control Logic block contains a counter and decoder circuitry that comprise a simple state machine that generates the signals to step through a sequence using the Distribution Circuit to connect each Bennett clock phase to the appropriate resonator at the appropriate time. The details of each block are given below.

[0039] The delay-locked loop (DLL) is a well-known circuit that is used most commonly to synchronize clock signals and to generate multi-phase clocks. A schematic block diagram for a DLL is shown in FIG. 3, wherein a four-stage voltage controlled delay line is used to introduce a delay in the signal from the input, which in the present disclosure is the Master Digital Clock (MDC). A phase detector (PD) then measures the phase difference between the input and the delayed signal, and produces a signal that is used to adjust the delay of the delay line. In a simple explanation, the DLL locks when there is a phase difference of 0° between input and output meaning that the delay is set to exactly one clock period, 360° . To produce a multi-phase clock, the delay line is implemented using a number of series connected delay elements or amplifiers D , each of which introduces some delay D_i . In an example, the delay line will be implemented with four, or a multiple of four, delay

elements or amplifiers D. In the locked condition, the delay line represents a total delay of 360° , so by tapping the line at four equally spaced points, replicas of the clock may be produced separated by 90° of phase. These are the four clock phases needed to drive the four resonators.

[0040] With continuing reference to FIGS. 1-2, to specify the Control Logic and the Distribution Circuit, consider a single Bennett phase, wherein each Bennett phase comprises four parts: 1. The clock line is held at 0V, the null state. 2. The clock ramps to the active state. 3. The clock is held in the active state. 4. The clock ramps back down to the null state where it is again held at 0V.

[0041] A detailed schematic of an example distribution circuitry of the Distribution Circuit for one Bennett clock phase, e.g., Φ_{1+} and Φ_{1-} , is shown in FIG. 4, wherein when the Bennett phase is in Ramp state a transmission gate, T1, formed by parallel connected p-channel and n-channel transistors M1 and M2, connects the Resonator, e.g., resonator Res1 shown in FIG. 2, to the Φ_{1+} line, and a transmission gate T2 connects resonator Res3 to Φ_{1-} . When the Bennett phase is not in the Ramp state T1 and T2 isolate Φ_{1+} and Φ_{1-} from the resonators Res1 and Res3. When the Bennett phase is in the active state Transistor M1 connects Φ_{1+} to V_{DD} and transistor

[0042] M8 connects Φ_{1-} to V_{SS} . In the null state Transistors M4 and M7 connect Φ_{1+} and Φ_{1-} to Ground (0V). FIG. 5 shows the timing of the control signals for the distribution circuitry of FIG. 4. In order to create the Bennett clock signal shown in the top trace of FIG. 5, the Control Logic block generates three control signals, namely, Ramp, Stay Up, Stay Down, along with their logical inverses, for each Bennett clock phase, 16 clock phases, Φ_{1+} through Φ_{8-} , total in the example of FIG. 2. The Distribution Circuit may include other instances of the distribution circuitry shown in FIG. 4 for the other Bennett clock phases, e.g., one instance of the distribution circuitry for each Bennett clock phase. The timing of transitions in the Ramp signals output by the Control Logic to the Distribution Circuit for the phases of the Bennett clock are desirably synchronized with the oscillation in the resonators Res1 – Res4. This is possible because the phases of the resonators Res1 – Res4 is set by the master oscillators $M\Phi_1$ - $M\Phi_4$ for the resonators Res1 – Res4 which are set by the DLL, which in turn is set by the Master Digital Clock input into the DLL, which Master Digital Clock also sets the timing of the Ramp signals output by the Control Logic.

[0043] With continuing reference to FIGS. 1-5, during the Ramp state the Ramp control signal is asserted (Ramp is set to a logic 1 and $\overline{\text{Ramp}}$ is set to a logic 0) which

turns on the transmission gates T1 and T2 connecting $\Phi1+$ and $\Phi1-$ to the resonators Res1 and Res3.

[0044] Considering the example of Bennett phase $\Phi1+$, Ramp is activated when the output of resonator 1 (Res1) is crossing zero volts with a rising slope. This connects the Bennett phase $\Phi1+$ to Res1 while the resonator voltage is ramping from 0V to V_{DD} , supplying energy to the Adiabatic Logic to drive the computation of the Adiabatic Logic. When Res1 reaches V_{DD} , the Ramp signal is deactivated and Res1 is disconnected from the Bennett phase. At the same time transmission gate T2 and transistors M7 and M8 make connections from $\Phi1-$ to the resonator R3 which ramps from 0V to V_{SS} .

[0045] When transmission gates T1 and T2 have been turned off at the end of the Ramp state, the clock outputs $\Phi1+$ and $\Phi1-$ and the Adiabatic Logic being driven by them in FIG. 5 are left floating. If leakage currents in this Adiabatic Logic are small, the voltage will remain at V_{DD} and V_{SS} since the Adiabatic Logic represents a capacitive load. However, if there is significant leakage, the voltage of $\Phi1+$ and $\Phi1-$ in FIG. 5 line will droop, which will lead to an undesirable power spike when the clock line is reconnected to the resonator, e.g., Res1 in the Ramp down state. To avoid or eliminate this voltage droop, when the Ramp signal deactivates the Stay Up signal may be asserted which turns on the p-channel transistor M3 and n-channel transistor M8 and connects the Bennett clock lines $\Phi1+$ and $\Phi1-$, to V_{DD} and V_{SS} .

[0046] When it is time to ramp down the Bennett clock phase, Stay Up deactivates, and Ramp is reasserted, turning on T1 and T2 reconnecting $\Phi1+$ and $\Phi1-$ to the resonators, e.g., Res1 and Res3. This occurs when the resonator Res1 is at V_{DD} and about to drop back to 0V. As the voltage of the resonator drops, energy is drawn back from the Adiabatic Logic into the resonator where it is stored to be reused. When the voltage of the resonator has reached 0V the Ramp signal is deactivated, disconnecting the $\Phi1+$ and $\Phi1-$ and, hence, the Adiabatic Logic from the resonator, and the Stay Down line is asserted. This turns on the transistors M4 and M7, which connect the $\Phi1+$ and $\Phi1-$ to 0V, holding them in the Null state.

[0047] To generate the required control signals, i.e., Ramp, Stay Up, Stay Down, and their inverses, for each Bennett phase, the Control Logic implements a simple state machine. The ordering of the sequence of the control signals is set by the nature of the Bennett clock timing: $\Phi1$ ramps to the active state ($\Phi1+$ and $\Phi1-$), then $\Phi2$ ramps up and so on until the last phase ΦN has ramped up. When all phases have

ramped up, the system is in the Active State where is held for the number of clock cycles N_{Active} . Then, the Bennett clock phases ramp back to 0V in reverse order.

[0048] A block diagram of the Control Logic is shown in Figure 6. The bit length required for the counter is:

$$N_{Bits} = 1 + \text{int}(\log_2(2N_{Phase} + N_{Active} + N_{Null} - 1)) \quad (3)$$

For the example of FIG. 2, with $N_{Phase}=8$ and choosing $N_{Active} = N_{Null} = 1$, a 5 bit counter will be required. The counter is a standard count-up counter which repeatedly counts from zero with a reset at the number $N_{Reset} = 2N_{Phase} + N_{Active} + N_{Null} - 1$. The outputs of the counter feed into a decoder that has a number of outputs equal to the number of steps, $N_{Reset} + 1$. As the counter counts up, each output of the decoder is asserted, with a Logic 1, in turn from Out_0 to $Out_{N_{Reset}}$. The decoder outputs are routed to Phase Control blocks Phase Ctl 1 – Phase Ctl N, one for each Bennett phase.

[0049] The circuitry of a single phase control block in FIG. 6 (e.g., Phase Ctl1), having two input Up and Down, is shown in FIG. 7. For the eight Bennett Phase example of FIG. 2 with $N_{Active} = 1$, the decoder output Out_0 is connected as the Up input of Phase Ctl1, and Out_9 is connected as the Down input, as shown in FIG. 6. The other phase control circuits are connected in a similar fashion, with Phase Ctl8 having decoder output Out_7 as its Up input and Out_{16} as its Down input. All of the flip-flops F1-F4 have reset inputs, omitted for clarity, which is asserted when power is applied so that all of the flip-flops F1 – F4 start with Q=0. The inputs Up and Down are outputs from the decoder and are set to a logic 1 when it is time for the ramp up and ramp down respectively. Note that in FIG. 7 the logical inverses of the output signals are not shown for clarity but are provided to the distribution circuitry of FIG. 4.

[0050] There is a one MCLK cycle delay as the Up signal is clocked into flip-flop F1, whereupon the Ramp signal is asserted. On the next MCLK cycle, Ramp goes to a logic 0 (from a logic 1), whereupon flip-flop F3 changes state asserting Stay Up to hold the Bennett clock lines in the active state. Flip-flop F3 keeps Stay Up asserted until the Down signal is sent from the Decoder. On the next MCLK cycle Stay Up is de-asserted, whereupon flip-flop F2 causes Ramp to be asserted to connect the Bennett clock line and, hence, the Adiabatic Logic to the resonator (e.g., Res1) to recover energy. After all the Bennett phases have ramped down, the counter (FIG. 6) resets back to zero, and the cycle begins again. The circuitry of the other phase control blocks in FIG. 6 is similar to that shown in FIG. 7. The phase control blocks in FIG. 6 are

operated in a manner to generate the Bennett clock signals need to drive the Adiabatic Logic.

[0051] The Bennett clocks may also be generated using an array of resonators building on the well-known principle of the Fourier series to construct an arbitrary waveform. Simulations show that approximately 10 harmonics are sufficient to produce a trapezoidal waveform that is sufficiently close to the desired one, as shown in FIG. 8. FIG. 8a shows the waveform of Bennett phase 1 constructed of 10 harmonics, and FIG. 8b shows 12 Bennett phases, each of which comprises 10 harmonics. A simplified implementation of one Bennett clock generator is shown in FIG. 9a. As before, the resonators Res1 – Res10 drive the Adiabatic Logic, but switches, e.g., transmission gate T1 in FIG. 4, to connect and disconnect the Adiabatic Logic from the resonators are not needed as the composite waveform of the resonators has the correct shape for the Bennett phase, as shown in FIG. 8a. To construct the Bennett phase based on Fourier components, a resonator is needed for each harmonic, wherein the resonator needed for each harmonic may be driven by a dedicated oscillator, e.g., Osc1 driving Res1 in FIG. 9a, at the frequency and amplitude set by the needed Fourier component. The outputs of the resonators, e.g., Res1 – Res10, are combined, by connecting them in parallel, and applied to the Adiabatic Logic. If ten harmonics are needed to construct the desired waveform, then ten resonators and ten master oscillators are needed, as shown in FIG. 9(a).

[0052] However, a simplification may be possible by combining master oscillators and resonators. Specifically, if an array of oscillators is driven by a waveform that is the shape of the desired Bennett clock waveform, then from Fourier series theorem, that Bennett clock waveform contains all the Fourier components at the proper harmonics and amplitudes. Piezoelectric resonators also act as frequency selectors, so when this waveform is applied to the array of resonators, each resonator responds only to its own resonant frequency and ignores all the other frequency components. Thus, the oscillators Osc1 – Osc10 in FIG. 9a may be replaced by a Master Waveform generating circuit, as shown in FIG. 9b.

[0053] To simplify the array of resonators, instead of implementing one piezoelectric resonator for each required component, multiple harmonics may be implemented a single piezoelectric resonator structure in the nature of a piezoelectric contour mode resonator. Referring to FIG. 10, in a typical piezoelectric contour mode resonator, the resonator is formed using a rectangular, suspended, plate of piezoelectric material

held in place by anchors. Metal electrodes are fabricated on the top surface of the material and an optional metal ground plane can be formed on the back of the material as shown and a sinusoidal voltage is applied. The electric fields formed by the electrodes excite a mechanical oscillation in the piezoelectric material, and resonance occurs when the mechanical oscillations from each electrode are in phase and fit with the boundary conditions imposed by the shape of the plate of piezoelectric material. In this way resonant frequency of oscillation is set by the spacing of the electrodes and the properties of the material. A multi-spectral resonator can be formed by fabricating electrodes on the piezoelectric material with multiple spacings, thereby exciting oscillations at multiple frequencies. For example, the resonator as shown in FIG. 10a in top view, with electrode fingers at a spacing of A , $A/2$, and $A/4$, would produce resonances at f_0 , $2f_0$, and $4f_0$. Note that all the electrode fingers are connected together and driven with a common voltage, with a ground plane on the back of the piezoelectric material. The key feature of this multi-spectral resonator is distance of an electrodes from the edge of the piezoelectric material. Since the mechanical oscillations are in the horizontal direction of FIG. 10a, the edge of the material sets a boundary condition since energy is reflected at the edge, which selects the frequency modes that can be excited by the electrodes. The set of electrodes which have a distance of $\pi/2$, one half the wavelength, from the edge will be selected as the resonant mode. The number of frequency components that can be excited in the resonator is limited by the spacing of the electrodes, which in turn is limited by the lithography method used in the fabrication of the electrodes. To relax the lithography requirements the needed harmonics for the waveform can be broken up between multiple resonators by fabricating the electrodes of some harmonics on one resonator plate and electrodes for other harmonics on another resonator plate. The output of the resonators can then be combined by connecting the resonators in parallel. The resonators are kept in phase by the signal from the master waveform generator driving the resonators.

[0054] In the contour mode resonator shown in FIG. 10a, the suspended plate of piezoelectric material is held in place by anchors. These anchors provide a route through which some of the vibrational energy in the resonator plate can escape. This lost energy has a detrimental effect on the performance of the resonator and should be minimized. This is particularly challenging in a multi-spectral resonator since multiple vibration wavelengths must be prevented from escaping through the anchors.

This can be accomplished by placing energy reflectors at each anchor as shown in FIG. 10a. The energy reflector, shown schematically in FIG. 10c, builds on the principle of a Bragg reflector by using an array of holes etched in the piezoelectric material. By placing the holes at a spatial period of $\pi/4$ reflections of the vibrational waves at the holes produce destructive interference to block the escape of energy. As with the electrodes, in FIG. 10a, multiple periodicities of holes can be fabricated to reflect the intended harmonics of the resonator.

[0055] To implement the full Bennett clock array with N phases, there must be N resonators for the positive phases, and N resonators for the negative phases, and a control circuit that generates a total of 2N master waveforms to drive the resonators. The master waveform generator can be implemented using the same counter and decoder circuit of FIG. 6, with a modified Phase Control circuit, as shown in FIG. 11a, wherein the Up or Down signals are used to trigger a toggle flip-flop F1, and an RC filter is used to spread the output step to approximate the ramp of the Bennett clock, see FIG. 11b. The output Master Waveform may be applied to the multispectral resonator (e.g., FIG. 9b) to excite the needed harmonics to produce the Bennett phase that is applied to the Adiabatic Logic.

CLAIMS

1. A method, comprising:
 - (a) in a circuit with at least four quadrature resonators delayed by a phase of $\pi/2 = 90^\circ$, wherein the at least four quadrature resonators generate a set of both positive and negative going ramps, holding an output clock line initially at zero;
 - (b) connecting the output clock line to at least one of the at least four quadrature resonators as the output clock line crosses zero;
 - (c) disconnecting the output clock line from the at least one resonator after the at least one resonator ramps up to maximum voltage;
 - (d) holding the output clock line constant for a number of resonator periods; and
 - (e) reconnecting the output clock line to the at least one resonator when the at least one resonator ramps down.
2. A method, comprising: forming a Bennett phase based on Fourier components, wherein approximately ten harmonics are used to construct an arbitrary waveform, and wherein the ten harmonics comprise:
 - at least one resonator for each of the ten harmonics; and
 - a control circuit that generates master waveforms to drive the resonators.