RAPID ANNEALING PROCESS FOR WAFERS IN SEMICONDUCTOR MATERIAL

Herein disclosed is the surface treatment of wafers of material intended for use in microelectronics, optics and optoelectronics applications.

It is specified that the wafers relating to embodiments of the invention are made of semiconductor materials.

The particular example described in this text thus concerns an SOI (Silicon On Insulator) type wafer.

Also disclosed is a surface treatment process for a wafer of material chosen among the semiconductor materials, the wafer being obtained via a transfer technique, and the process comprising a rapid annealing stage comprising successively:

- a first ramp of temperature rise intended to initiate heating,
- a first stabilisation halt intended to stabilise the temperature,
- a second ramp of temperature rise.

It is specified that the wafers of semiconductor material relating to embodiments of the invention are wafers obtained via a transfer technique, that meaning wafers of which

one layer (corresponding to all or part of the wafer) has been transferred from a source substrate onto a support.

It is also specified that "rapid annealing" is annealing that brings the wafers to very high temperatures (about 1100°C or more), in a very short time (a few tens of seconds).

This type of annealing is commonly referred to as RTA (Rapid Thermal Annealing).

It allows the surface of the wafers to be smoothed.

RTA as it is practised in the state of the art is skeletally illustrated in Figure 1, which shows the evolution of the temperature T according to the time t.

This figure shows that the RTA comprises ramps of temperature rise, to take the wafers subject to the RTA from a room temperature RT to a high end-of-annealing temperature T2, in a very short time.

By way of example, RT can range between about 20°C and 500°C, and T2 can be about 1200°C.

This figure shows that RTA actually comprises two rectilinear ramps:

- a first ramp taking the wafer from a temperature T1 of about 750°C, and followed by a halt of about 10 seconds at this temperature. This first ramp and the halt that follows it allow:
  - heating to be initiated,
  - the temperature follow-up of the wafer subject to RTA to be started up (this follow-up is ensured by a pyrometer which determines the temperature of the wafer, but the wafer only becomes "readable" by the pyrometer from a certain temperature which depends on the material of the wafer - in the case of a wafer of silicon this temperature is about 400°C),

> the temperature to be stabilised (this is more particularly the role of the halt).

• A second ramp with a slope of about 50°C per second, followed by a halt of about 30 seconds. This second ramp constitutes an important active phase of the RTA.

It has been observed that with such conventional RTA, defaults appear in the wafers, particularly in the case of wafers made from silicon (SOI for example).

These defaults known as slip lines result from the important thermal constraints that the wafer is subject to during RTA.

These thermal constraints are particularly due to the very steep ramps of temperature rise, as well as to a final halt at a very high temperature.

Hence, fewer or more slip lines will be observed on a wafer subjected to conventional RTA, depending on the thermal budget applied to the wafer.

These slip lines are likely to appear over the whole surface of the wafer, and notably on the elements that support the wafer inside the annealing oven. Obviously, such slip lines constitute an inconvenience.

The aim of embodiments of the invention are to reduce this inconvenience.

According to a first aspect of the invention, there is provided a surface treatment process for a wafer of material chosen among the semiconductor materials, the wafer being obtained via a transfer technique, and the process comprising a rapid annealing stage comprising successively :

• a first ramp of temperature rise intended to initiate heating,

- a first stabilisation halt intended to stabilise the temperature,
- a second ramp of temperature rise, characterised in that during the second ramp, the average slope of temperature rise has a first value within a first range of temperatures known as low, and then increases within a range of temperatures known as high.

Here are some preferred yet non-restrictive embodiments of the process according to the invention:

- the wafer is a wafer made from silicon,
- the wafer is an SOI wafer,
- the first halt takes place at a temperature of about 750°C,
- the range of low temperatures extends from about 800 to about 1100°C,
- within the range of high temperatures, the temperature increases in a continuous manner,
- within the range of low temperatures, the temperature increases with an intermediate halt,
- the rapid annealing stage ends with a halt, at a temperature of about 1150 to 1250°C,
- the second ramp ends with a slope of about 25 to 50°C per second.

Other aspects, goals and advantages of the invention will become clearer upon reading the following description of the invention, given in reference to the annexed drawings in which, in addition to Figure 1 which has already been commented on with reference to the state of the art:

- Figures 2a and 2b are graphs showing the evolution of the temperature during two RTA stages carried out respectively in a continuous manner, and according to the invention,
- Figure 3 is a graph showing the effect, on the number of slip lines, of the length of the interval of time passed during RTA within a certain temperature range.

Now with reference to Figures 2a and 2b, they show the evolution of the temperature during two temperature rises for two respective RTA stages, carried out according to knowledge of the state of the art (Figure 2a) and according to the invention (Figure 2b).

It is specified that the figures are described with reference to the RTA annealing of an SOI wafer, issued from a transfer process with detachment along an embrittlement zone (SMARTCUT® type process).

However, the invention also applies to wafers obtained via any type of transfer process (for example ELTRAN® or other), and that do not necessarily have an SOI type structure.

The invention thus applies to wafers in silicon, or to wafers made of other semiconductor materials.

The temperature rises in Figures 2a and 2b correspond, as has already been said, to two RTA stages, one of which (Figure 2b) is carried out according to the invention.

These two temperature rises roughly start in the same way, with a first ramp R1 taking the temperature to a value of about 750°C.

A first constant temperature halt (at a value of about 750°C) follows this first ramp.

The difference between the two annealing stages lies in the second ramp of temperature rise, which follows the first halt.

Indeed, it has been observed that the ramp of Figure 2a is substantially rectilinear, in accordance with what is already known. This second ramp thus has a constant slope of about 50°C per second.

And this conventional annealing ends with a halt of 1 to 30 seconds, during which the temperature is maintained at a constant value of about 1200 to 1230°C.

As for the second ramp R2 of Figure 2b, it is not rectilinear.

On the contrary, this second ramp generally has a concave shape, that meaning that it generally extends below the straight line (represented as a dotted line) joining the point P1 at the start of this ramp (about 750°C) to the point P2 at the end of this ramp (which typically is about 1150-1250°C).

More precisely, during the second ramp, the average slope of temperature rise has a first value with a first range of temperatures known as low, and then increases with a range of temperatures known as high.

In other terms, during the temperature rise of this second ramp, proportionally more time is at first spent for a given temperature rise (first range), than during the latter part of the ramp (second range).

Moreover it is specified that in the case of the invention, this second ramp R2 is associated with a duration $\Delta t2$ of temperature rise which is greater than the duration of the temperature rise of a second conventional ramp, for the same difference in temperature.

It is specified that this duration corresponds in Figure 2b to the time difference between the points P1 (start of the second ramp R2 according to the invention) and P2 (end of the second ramp R2 according to the invention).

For comparative purposes, a second conventional ramp $R_0 2$, as practised according to the state of the art, has also been represented in this figure. This second conventional ramp $R_0 2$ starts at the same point P1, but ends in $P_0 2$, which is distinct from P2 and precedes it in time.

Thus it appears that in comparison with a second conventional ramp, the second ramp R2 according to the invention not only is not rectilinear and has an average slope which increases between two successive ranges, but also corresponds to a temperature rise which is globally slower.

More precisely, in the example represented in Figure 2b, the second ramp has a slope which increases progressively and continuously, this slope having successively the following values: 10-15-25-50°C per second.

The second ramp in Figure 2b thus ends with a maximum slope of about 50°C per second, which corresponds to the second ramps of RTA stages according to the state of the art.

A major characteristic of this ramp is that it allows the time passed by the wafer in a range of low temperatures of this second ramp, which starts around 750°C and ends around 1150-1250°C, to be increased.

The range in question can be identified in the example described here as corresponding to temperatures lying between about 800°C and about 1100°C.

It is noted that according to the invention, the time passed by the wafer subject to RTA in a low range of temperature of the second ramp, is increased.

This increase is "absolute", in the sense that the time actually spent in this range known as low is increased in comparison with conventional RTA.

This increase can also be considered in relation to the second ramp in general: it is noted that according to the invention, during this second ramp, the ratio of the time passed in the so-called low range to the time passed in the so-called high range (which corresponds to the temperatures of the second ramp that are greater than the temperatures of the "low" range), is increased in comparison with what is practised in the state of the art.

In other words, according to the invention, more time is spent in this "low" temperature range of the second ramp, in comparison with the total duration of the second ramp than in annealing stages with a linear ramp as per the state of the art.

Indeed, during the second ramp, the average slope of temperature rise has a first value within a first range of temperatures known as low, and then increases within a range of temperatures known as high.

It is specified that the ranges of "low" and "high" temperatures are defined notably according to the material of the wafer.

Moreover it is possible to implement the invention with another "second ramp", from the moment that the condition regarding the ratio of time passed in the low

and high temperature ranges which is explained above, is respected.

It is for example possible to define an intermediate constant temperature halt in this range of low temperatures (for example a halt at a temperature between 800 and 1100°C in the example described here).

Generally speaking, it is possible to give the second ramp any form which allows this condition to be respected.

Proceeding in such a manner allows the number of slip lines on the wafer after annealing to be substantially reduced.

The applicant has notably observed that the slip lines engendered on the supports of the wafer in the oven are considerably reduced (whether these supports have the form of separate points of support, or of a continuous circular ring, concentric to the wafer).

This effect is explained by the fact that the slip lines observed at the end of RTA originate in defaults engendered during the part of the RTA of the wafer that corresponds to the "low" temperature values.

This effect is illustrated in Figure 3, which represents, for four conditions of RTA carried out on four respective wafers, the number of slip lines produced on the wafer after annealing.

The four annealing stages correspond to the series of points spread out in abscissa - each different abscissa corresponds to an annealing.

Below this graph are lines of data.

The first line of "time" data indicates, for each annealing, the time passed in the range of "low" temperatures of the second ramp - the four annealing

stages having the same first ramp R1, similar to that of Figure 2b.

The second line of "Average" data corresponds to the number of slip lines observed on a population of wafers, after annealing.

The third line of "Count" data indicates the number of wafers on which the slip lines have been counted (this number being limited to one in two cases).

It can be observed that as the "time" increases, the number of slip lines decreases.

Indeed here are the results obtained:

Time passed in the low temperature range (in seconds)	Average number of slip lines observed
7	46.5
14.5	30
19	14
26	6.5

It is specified that in the example of Figure 3, the range of "low temperatures" extended between 800 and 1100°C.

The application of a second progressive ramp of RTA, which corresponds to a high ratio (time passed in the low temperature range/time passed in the high temperature range), is thus beneficial for reducing the number of slip lines.

CLAIMS

1. Surface treatment process for a wafer of material chosen among the semiconductor materials, the wafer being obtained via a transfer technique, and the process comprising a rapid annealing stage comprising successively:

- a first ramp of temperature rise intended to initiate heating,
- a first stabilisation halt intended to stabilise the temperature,
- a second ramp of temperature rise, characterised in that during the second ramp, the average slope of temperature rise has a first value within a first range of temperatures known as low, and then increases within a range of temperatures known as high.

2. Process according to the previous claim, characterised in that the wafer is a wafer made from silicon.

3. Process according to the previous claim, characterised in that the wafer is an SOI wafer.

4. Process according to one of the two previous claims, characterised in that the first halt takes place at a temperature of about 750°C.

5. Process according to one of the three previous claims, characterised in that the range of low temperatures extends from about 800 to about 1100°C.

6. Process according to one of the previous claims, characterised in that within the range of low temperatures, the temperature increases in a continuous manner.

7. Process according to one of claims 1 to 5, characterised in that within the range of low temperatures, the temperature increases with an intermediate halt.

8. Process according to one of the previous claims, characterised in that the rapid annealing stage ends with a halt, at a temperature of about 1150 to 1250°C.

9. Process according to one of the previous claims, characterised in that the second ramp ends with a slope of about 25 to 50°C per second.