

## **Antenna and Receiver Circuit**

### **TECHNICAL FIELD**

**[0001]** The invention relates to an antenna and a receiver circuit.

### **BACKGROUND**

**[0002]** By transmitting signals with low power density through an ultra-wideband (UWB) spectrum, UWB systems can achieve high speed data rate communication with low power consumption.

**[0003]** However, the performance of the UWB systems may be degraded from interference that may exist due to the presence of signals from other existing wireless communication systems. For a 3-5 GHz IR-UWB system, interference sources are for example signals from a 802.11a WLAN system, which occupy the 5-6 GHz spectrum; and signals from a 802.11b/g WLAN system covering the 2.4-2.48 GHz frequency band. In addition, the deployment of WiMax system in the 3.5 GHz frequency band also introduces inband interference. Without proper suppression, a strong interference signal from WLAN or WiMax systems can saturate a UWB RF front-end easily and desensitise the receiver. Hence, robustness to both the in-band/out-band interference is important to a UWB receiver front-end.

**[0004]** In conventional receivers, a band-pass filter is placed between the antenna and the RF front-end to filter out the out-of-band interference signals. In order to block in-band interference, band-pass filters with multiple stop-band function have been proposed. However, these filters are usually implemented on a PCB board, leading to an increase in the circuit size and also resulting in additional pass-band insertion loss. Since this filter is before an amplifier, this insertion loss will directly contribute to the increase of input referred noise figure, leading to degraded receiver sensitivity.

**[0005]** There is thus a need to improve inband and out-of-band interference rejection of receivers and also to provide an integrated system that suppresses inband

and outband interference without system size increase and compromise in system performance for practical UWB application.

## SUMMARY

[0006] According to various embodiments, there is provided an antenna including: a substrate; a conductive layer formed on a portion of a top surface of the substrate; a first slot formed within the conductive layer; a conductive stub disposed within the first slot, the conductive stub tuned to reject a first frequency band; and a second slot formed within the conductive layer, the second slot tuned to reject a second frequency band.

[0007] According to various embodiments, the conductive layer may be a layer capable of receiving and sending signals. The first slot and the second slot may be enclosed areas etched from the conductive layer such that at least a portion of the enclosed area of the first slot and the second slot is devoid of the conductive layer, thereby leaving exposed substrate. The conductive stub may be made of the same material as the conductive layer or the conductive stub may be made of different material which is capable of receiving and sending signals.

[0008] According to various embodiments, the conductive layer may have any one of the following shapes: circular, trapezoidal or elliptical. The first slot may be formed from any one of the following shapes: circular, rectangular or elliptical. The conductive stub may have a rectangular shape or any one of the following other shapes: a square, a triangle, a circle or an ellipse. The second slot may be formed from any one of the following shapes: arc, arrowhead or polygonal.

[0009] In one embodiment, the second slot may partially surround the first slot. In other embodiments, the second slot may not surround the first slot.

[0010] According to various embodiments, there is provided a receiver circuit including an antenna including: a substrate; a conductive layer formed on a portion of a top surface of the substrate; a first slot formed within the conductive layer; a conductive stub disposed within the first slot, the conductive stub tuned to reject a first frequency band; and a second slot formed within the conductive layer, the

second slot tuned to reject a second frequency band; an amplifier connected to the antenna; and a notch filter connected to the amplifier.

[0011] According to various embodiments, there is provided a receiver circuit including a notch filter, wherein the notch filter includes an active element configurable to change a frequency rejection band of the notch filter.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0012] In the drawings, like reference characters generally refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments of the invention are described with reference to the following drawings, in which:

[0013] Figure 1 shows a block level representation of front-end architecture of a receiver circuit built in accordance to an embodiment of the present invention.

[0014] Figure 2 shows a side view of the antenna, built in accordance to an embodiment of the present invention, of Figure 1.

[0015] Figure 3 shows a view of the antenna, built in accordance to an embodiment of the present invention, of Figure 1.

[0016] Figures 3A to 3I each show a view of an antenna built in accordance to an embodiment of the present invention.

[0017] Figure 4 shows a circuit level implementation, built in accordance to an embodiment of the present invention, of the amplifier shown in Figure 1.

[0018] Figure 5A shows a circuit level implementation, built in accordance to an embodiment of the present invention, of the notch filter shown in Figure 1.

[0019] Figure 5B shows an equivalent circuit diagram of the notch filter shown in Figure 1.

[0020] Figure 6 shows the measured normalized receiver front-end transfer function of a receiver circuit built in accordance to an embodiment of the present invention.

## DESCRIPTION

[0021] While embodiments of the invention have been particularly shown and described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The scope of the invention is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced. It will be appreciated that common numerals, used in the relevant drawings, refer to components that serve a similar or the same purpose.

[0022] Figure 1 shows a block level representation of front-end architecture 100 of a receiver circuit 108 built in accordance to an embodiment of the present invention.

[0023] The front-end architecture 100 includes an antenna 102, a notch filter 104 and an amplifier 106. A low noise amplifier (LNA) may be used for the amplifier 106. The LNA 106 is connected to the antenna 102, while the notch filter 104 is connected to the LNA 106.

[0024] In the embodiment shown in Figure 1, the antenna 102 may be a planar UWB (ultra wide band) antenna designed to have a first frequency band rejection at around 5.2 GHz and a second frequency band rejection at around 2.4 GHz. The antenna 102 facilitates out-of-band rejection, i.e. filtering interference that may occur from signals in the 2.4 GHz and 5.2 GHz frequency bands. The LNA 106 is equipped with a fixed rejection frequency band (or notch) at around 1.8 GHz and a tunable notch between the frequencies of about 2 GHz to about 3.6 GHz. The LNA 106 facilitates inband rejection, i.e. filtering interference that may occur from signals between the 2.4 GHz and 5.2 GHz frequency bands.

[0025] Consider a known UWB receiver structure (not shown) which includes a conventional antenna coupled to an on-board band pass filter, which is used to facilitate out-of-band frequency rejection. Comparing the front-end architecture 100 with the known UWB receiver structure, the front-end architecture 100 eliminates

the need of having an on board band pass filter. This leads to a reduced system size. Further, by eliminating the need for an on-board band pass filter, insertion loss is reduced, thereby improving receiver sensitivity.

**[0026]** The front-end architecture 100 has the following advantages over the known UWB receiver structure. By combining the antenna 102 and the LNA 106 frequency band rejection ability, the rejection specification of each block (104 and 106) will be alleviated, reducing the design difficulty of the LNA 106 and the notch filter 104. Usually, the band-notch antenna 102 alone can provide 8-10 dB attenuation in the 2.4 GHz band, hence the LNA 106 only needs to provide 10 dB attenuation in the 2.4 GHz band. Furthermore, by tuning the notch frequency of LNA 106 using a varactor, the total notch bandwidth in the range of 2.4 GHz can be increased. On the other hand, the 5.2 GHz attenuation of the LNA 106 is around 5 dB, with the antenna 102 contributing another 10-15 dB attenuation to meet design specifications.

**[0027]** Another advantage of the front-end architecture 100 is the elimination of bulky pre-select and band-notch filters by embedding the out-of-band frequency rejection function into the antenna 102 (without increasing the size of the antenna 102) and on-chip in the integrated circuit, hence reducing the system size.

**[0028]** Figure 2 shows a side view of the antenna 102 of Figure 1. The antenna 102 has a substrate 202 having a top surface 202t and a bottom surface 202b opposite the top surface 202t. Conductive layers 204 and 206 are formed on each of the top and bottom surfaces 202t and 202b respectively.

**[0029]** Figure 3 shows a view of the substrate 202 where both the conductive layer 204 on the top surface 202t and the conductive layer 206 on the bottom surface 202b are shown. It will be appreciated that the view shown in Figure 3 does not mean that both conductive layers 204 and 206 are on a common surface. Rather, Figure 3 serves to illustrate how the conductive layer 206 on the bottom surface 202b is positioned relative to the conductive layer 204 on the top surface 202t.

**[0030]** From Figure 3, it can be seen that the antenna 102 includes the substrate 202. The conductive layer 204 is formed on a portion of the top surface 202t of the substrate 202. A first slot 302 is formed within the conductive layer 204. A

conductive stub 306 is disposed within the first slot 302, the conductive stub 306 tuned to reject a first frequency band. A second slot 304 is also formed within the conductive layer 204, the second slot 304 tuned to reject a second frequency band.

[0031] In the embodiment shown in Figure 3, the antenna 102 has a planar monopole structure with band-notch function at around 2.4 and around 5.2 GHz.

[0032] The substrate 202 has a dielectric constant  $\epsilon_r$  of around 2.33 and a thickness T of around 0.63 mm. The substrate 202 has a length L of around 40 mm and a width W of around 30 mm. It will be appreciated that for other dielectric constant  $\epsilon_r$  values, the length L and width W values will vary accordingly.

[0033] The conductive layer 204 is disposed within the substrate 202, so that the conductive layer 204 is surrounded by an area of exposed substrate. The conductive layer 204, is capable of receiving and sending signals (i.e. is also a radiating element). Within the conductive layer 204, the conductive stub 306 is connected to a segment 308 of the first slot 302 via a conductive strip 310. In this manner, the conductive stub 306 and the conductive strip 310 form a T-shaped conductor, accommodated within the space provided by the first slot 302.

[0034] The T-shaped conductor has a length  $L_1$  ( $L_1$  is also the length of the conductive strip 310 within the first slot 302) of around 6 mm. The conductive strip 310 extends linearly beyond the segment 308 to form a feed line 312 of the antenna 102. A signal received by the antenna 102 is transmitted to the LNA 106 and the notch filter 104 via the feed line 312. Signals to be transmitted by the antenna 102 are also sent through the feed line 312.

[0035] The second slot 304 is adjacent to a portion of a perimeter of the conductive layer 204 and has a curved slot shape corresponding to the perimeter of the conductive layer 204. As shown in Figure 3, the second slot 304 does not extend to cover the entire portion adjacent to the perimeter of the conductive layer 204. In the embodiment shown in Figure 3, the second slot 304 has an arc length  $L_{\text{slot}}$  of around 32 mm and partially surrounds the first slot 302.

[0036] The conductive layer 204 has a circular shape and the first slot 302 has a circular shape with a radius r smaller than a radius R of the conductive layer 204. In this manner, the conductive layer 204 forms a ring monopole, with an outer radius R

of length around 10.5 mm and an inner radius  $r$  of length around 5 mm. The circular shape of the conductive layer 204 provides the antenna 102 with a wideband characteristic.

[0037] There is an offset  $L_D$  of length around 4mm along a  $z$  axis 314 (i.e. along the plane of the top surface 202t of the substrate 202) between the centers of the circular shaped conductive layer 204 and the circular shaped first slot 302. Varying this offset  $L_D$  provides a means to control antenna matching of the antenna 102.

[0038] The conductive layer 206 (formed on a portion of the bottom surface 202b of the substrate 202) serves as a ground plane 316 of the antenna 102. The finite ground plane 316, having length  $L_2$  of around 12 mm is printed to only cover the microstrip feed line 312. The ground plane 316 does not have a conventional rectangular shape, but rather a trapezoidal shape (as shown in Figure 3), so as to minimize ground plane effect. It will be appreciated that other shapes for the ground plane 316 include a semi-circular shape (see ground planes 316a to 316i of Figures 3A to 3I respectively). A gap 208 (see Figure 2) exists between the ground plane 316 and a portion on the bottom surface 202b of the substrate 202 corresponding to where the conductive layer 204 is formed on the portion of the top surface 202t of the substrate 202.

[0039] The ground plane 316 is formed on a portion of the bottom surface 202b of the substrate 202 in such way not to overlap with the conductive layer 204 on the top surface 202t of the substrate 202. Accordingly, electromagnetic waves can be radiated or received by the conductive layer 204 without being shielded by the ground plane 316. In this manner, an omnidirectional radiating pattern similar to that of a general monopole antenna can be obtained.

[0040] Given that the ground plane 316 does not have a straight profile edge (due to the trapezoidal shape of the ground plane 316), the gap 208 ranges over distances of around 0.3 mm to around 1 mm.

[0041] The feed line 312 is a  $50\Omega$  microstrip design with metal strip width  $W_1$  of around 1.5 mm. The T-shaped conductor within the first slot 304 has the same width as the microstrip feed line 312.

[0042] At the resonance frequency of the conductive strip 310, the current distribution of the circular ring monopole (i.e. the conductive layer 204) will be disrupted, resulting in the malfunction of ring monopole in the resonant frequency range. The expression for the approximate notch frequency calculation (which is also the expression for tuning the conductive stub 306) is:

$$f_{notch1} = \frac{c}{4\sqrt{\epsilon_r}(L_1 + h)}, \quad (1)$$

[0043] where  $f_{notch1}$  is the rejected first frequency band,  $c$  is the speed of light,  $\epsilon_r$  is the substrate 202 dielectric constant,  $L_1$  the length of the T-shaped conductor and  $h$  is the shortest gap between a feed point (denoted segment 308 on Figure 3) of the conductive layer 204 and a portion on the top surface 202t of the substrate 202 corresponding to where the ground plane 316 is formed on the portion of the bottom surface 202b of the substrate 202. From equation (1), the rejected first frequency band can be changed by tuning the conductive stub 306 as follows. One way of tuning the conductive stub 306 is to vary the length  $L_1$  of the conductive strip 310 connected to the conductive stub 306.

[0044] The second slot 304 is tuned according to the expression:

$$f_{notch2} = \frac{c}{2L_{slot}\sqrt{\epsilon_r}}, \quad (2)$$

[0045] where  $f_{notch2}$  is the rejected second frequency band,  $c$  is the speed of light,  $\epsilon_r$  is the substrate 202 dielectric constant and  $L_{slot}$  is the length of the second slot 304 (being shaped in an arc as shown in Figure 3). From equation (2), it will be appreciated that the rejected second frequency band can be changed by changing the length of the second slot 304.

[0046] In the embodiment shown in Figure 3, the antenna 102 is adapted to operate in the UWB range (i.e. around 3 GHz to around 5 GHz), wherein the rejected first frequency band  $f_{notch1}$  is around 5.2 GHz and the rejected second frequency band  $f_{notch2}$  is around 2.4 GHz.

[0047] While Figures 2 and 3 show a circular shaped first slot 302 with a T-shaped conductor to achieve rejection of a first frequency band  $f_{notch1}$  and an arc-shaped second slot 304 to achieve rejection of a second frequency band  $f_{notch2}$ , it will

be appreciated that other shapes are possible to achieve dual frequency rejection bands. Such other shapes are shown in Figures 3A to 3I.

[0048] Figures 3A to 3I each show a view of an antenna 102a to 102i built in accordance to an embodiment of the present invention. In Figures 3A to 3I, it will be appreciated that the antenna substrate (compare Figure 3) is not shown for the sake of clarity. Also, the respective conductive layers 204a to 204i are shown superimposed over their respective ground planes 316a to 316i, where it does not mean that both the conductive layers 204a to 204i and their respective ground planes 316a to 316i are on a common surface.

[0049] The antenna 102 of Figures 2 and 3 share similar characteristics to each of the antennas 102a to 102i.

[0050] Each of the antennas 102a to 102i has a substrate (not shown) having a top surface and a bottom surface opposite the top surface. A conductive layer 204a to 204i is formed on a portion of each respective top surface of the substrate. A ground plane 316a to 316i is formed on a portion of each respective bottom surface of the substrate. A gap 208a to 208i exists between the respective ground plane 316a to 316i and a portion on the bottom surface of the substrate corresponding to where the respective conductive layer 204a to 204i is formed on the portion of the top surface of the substrate.

[0051] A first slot 302a to 302i is formed within the respective conductive layer 204a to 204i. A conductive stub 306a to 306i is disposed within the respective first slot 302a to 302i, the conductive stub 306a to 306i tuned to reject a first frequency band. A second slot 304a to 304i is also formed within the respective conductive layer 204a to 204i, the second slot 304a to 304i tuned to reject a second frequency band.

[0052] The conductive stub 306a to 306i is disposed within the respective first slot 302a to 302i, the conductive stub 306a to 306i being connected to a respective segment 308a to 308i of the respective first slot 302a to 302i via a respective conductive strip 310a to 310i. In this manner, the conductive stub 306a to 306i and the respective conductive strip 310a to 310i form a T-shaped conductor, accommodated within the space provided by the respective slot 302a to 302i.

[0053] The second slot 304a to 304i is adjacent to a portion of a perimeter of the respective conductive layer 204a to 204i.

[0054] The conductive layers 204a to 204c have a circular shape. On the other hand, the conductive layers 204d to 204f have a trapezoidal shape, while the conductive layers 204g to 204i have an elliptical shape. Thus, the conductive layer may be formed from any one of the following shapes: circular, trapezoidal or elliptical.

[0055] Further, the first slot 302g has a circular shape. On the other hand, the first slots 302a, 302b, 302d, 302e and 302h have rectangular shapes, while the first slots 302c, 302f and 302i have elliptical shapes. Thus, the first slot may be formed from any one of the following shapes: circular, rectangular or elliptical.

[0056] In addition, the second slots 304b, 304e, 304f to 304i are not formed parallel to the portion of the perimeter of the respective conductive layer 204b, 204e, 204f to 204i they are adjacent to. The second slots 304a, 304c, 304e to 304i are arc-shaped and similar to the second slot 304 of Figure 3. On the second slot 304b has an arrowhead shape, while the second slot 304d has a polygonal shape. Thus, the second slot may be formed from any one of the following shapes: arc, arrowhead or polygonal.

[0057] From Figures 3, 3A to 3I, it will be appreciated that the design of the antenna is not limited by the shape of the conductive layer, the shape of the first slot or the shape of the second slot. For one embodiment (not shown), a circular shaped conductive layer may incorporate a first slot having a shape that is either circular, rectangular or elliptical; and a second slot having a shape that is either an arc, an arrowhead or a polygon. In another embodiment (not shown), a trapezoidal shaped conductive layer may incorporate a first slot having a shape that is either circular, rectangular or elliptical; and a second slot having a shape that is either an arc, an arrowhead or a polygon. In one more embodiment (not shown), an elliptical shaped conductive layer may incorporate a first slot having a shape that is either circular, rectangular or elliptical; and a second slot having a shape that is either an arc, an arrowhead or a polygon.

[0058] In addition, the conductive stub (306, 306a to 306i) of the embodiments of the antenna shown in Figures 3 and 3A to 3I has a rectangular shape. In other embodiments (not shown) of the antenna, the conductive stub may have a shape being a square, a triangle, a circle or an ellipse.

[0059] Similar to the antenna 102 of Figures 2 and 3, at the resonance frequency of the conductive strip 310a to 310i, the current distribution of the respective conductive layer 204a to 204i will be disrupted, resulting in malfunction in the resonant frequency range. The expression for the approximate notch frequency calculation (which is also the expression for tuning each of the conductive stubs 306a to 306i) is:

$$f_{notch1} = \frac{c}{4\sqrt{\epsilon_r}(L_1 + h)}, \quad (1)$$

[0060] where  $f_{notch1}$  is the rejected first frequency band,  $c$  is the speed of light,  $\epsilon_r$  is the substrate dielectric constant,  $L_1$  the length of the T-shaped conductor and  $h$  (see Figures 3A to 3I) is the shortest gap between a feed point (denoted segment 308a to 308i on Figures 3A to 3I) of the respective conductive layer 204a to 204i and a portion on the top surface of the substrate corresponding to where the respective ground plane 316a to 316i is formed on the portion of the bottom surface of the substrate. From equation (1), the rejected first frequency band can be changed by tuning each of the conductive stubs 306a to 306i as follows. One way of tuning each of the conductive stubs 306a to 306i is to vary the length  $L_1$  of the conductive strip 310a to 310i connected to the respective conductive stub 306a to 306i.

[0061] Each of the second slot 304a to 304i is tuned according to the expression:

$$f_{notch2} = \frac{c}{2L_{slot}\sqrt{\epsilon_r}}, \quad (2)$$

[0062] where  $f_{notch2}$  is the rejected second frequency band,  $c$  is the speed of light,  $\epsilon_r$  is the substrate dielectric constant and  $L_{slot}$  is the length of the respective second slot 304a to 304i. From equation (2), it will be appreciated that the rejected second frequency band can be changed by changing the length of the respective second slot 304a to 304i.

[0063] Each antenna 102a to 102i is adapted to operate in the UWB range (i.e. around 3 GHz to around 5 GHz), wherein the rejected first frequency band  $f_{notch1}$  is around 5.2 GHz and the rejected second frequency band  $f_{notch2}$  is around 2.4 GHz.

[0064] Figure 4 shows a circuit level implementation, built in accordance to an embodiment of the present invention, of the LNA 106 shown in Figure 1.

[0065] In the embodiment shown in Figure 4, the LNA 106 is a single-ended four-stage current-reuse resistive feedback LNA. The LNA 106 has a first amplification stage 402 and a second amplification stage 404. The output (labeled Port X in Figure 4) of the first amplification stage 402 is connected to the input of the second amplification stage 404.

[0066] The first amplification stage 402 has two transistors ( $NM_1$  and  $NM_2$ ), five capacitors ( $C_3$ ,  $C_4$ ,  $C_5$ ,  $C_6$  and  $C_{decoupling}$ ), three resistors ( $R_n$ ,  $VR_1$  and  $R_1$ ) and two inductors ( $L_2$  and  $L_3$ ).

[0067] The gate terminal  $(NM_1)_G$  of the transistor  $NM_1$  is connected to capacitor  $C_3$ . The source terminal  $(NM_1)_S$  of the transistor  $NM_1$  is connected to a reference potential 406, being at ground level for the embodiment shown in Figure 4. The drain terminal  $(NM_1)_D$  of the transistor  $NM_1$  is connected to resistor  $R_n$ , inductor  $L_2$  and capacitor  $C_4$ . The resistor  $R_n$  is in turn connected to the capacitor  $C_3$ .

[0068] The gate terminal  $(NM_2)_G$  of the transistor  $NM_2$  is connected to capacitor  $C_6$  and the capacitor  $C_4$ . The source terminal  $(NM_2)_S$  of the transistor  $NM_2$  is connected to capacitor  $C_5$  and the inductor  $L_2$ . The capacitor  $C_5$  is in turn connected to the reference potential 406. The drain terminal  $(NM_2)_D$  of the transistor  $NM_2$  is connected to resistor  $VR_1$ , resistor  $R_1$  and capacitor  $C_7$ . (Capacitor  $C_7$  belongs to the second amplification stage 404)  $VR_1$  is a variable resistor which is also connected to the capacitor  $C_6$ .

[0069] The resistor  $R_1$  is connected to inductor  $L_3$ . The inductor  $L_3$  is in turn connected to capacitor  $C_{decoupling}$  and reference potential 408, denoted  $V_{dd}$  in Figure 4. The capacitor  $C_{decoupling}$  is in turn connected to the reference potential 406.

[0070] The LNA 106 input matching network includes capacitors  $C_1$ ,  $C_2$ , inductor  $L_1$  and input bonding wire 410. The capacitor  $C_1$  and the inductor  $L_1$  are both connected to the gate terminal  $(NM_1)_G$  of the first transistor  $NM_1$ . The capacitor  $C_1$

is in turn connected via the bonding wire 410 to an input 412 of the LNA 106. The RF signal from the antenna 102 (see Figure 1) enters the LNA 106 via input 412. The inductor  $L_1$  is in turn connected to capacitor  $C_2$ , whereby the capacitor  $C_2$  is in turn connected to the reference potential 406 via the bonding wire 410.

[0071] The inductor  $L_1$  and the capacitor  $C_2$ , connected in series, form a serial resonance network 420 which can provide a S21 notch at the serial resonance frequency. This notch frequency  $f_{notch\_LNA1}$  is determined by:

$$f_{notch\_LNA1} = \frac{1}{2\pi\sqrt{L_1 C_2}} \quad (3)$$

Thus, the serial resonance network 420 determines a frequency rejection band of the amplifier 106. In the embodiment shown in Figure 4, the LNA 106 provides a fixed notch of around 1.8 GHz. Sample values are as follows: ( $C_3=2$  pF,  $C_4=3$  pF,  $C_5=4$  pF,  $C_6=1.5$  pF,  $C_{decoupling}=100$  pF,  $L_2=2.4$  pF,  $L_3=2.4$  pF,  $R_1=600$  ohm,  $VR_1=800$  ohm and  $R_1=20$  ohm)

[0072] The second amplification stage 404 has two transistors ( $NM_3$  and  $NM_4$ ), seven capacitors ( $C_7$ ,  $C_8$ ,  $C_9$ ,  $C_{10}$ ,  $C_{11}$ ,  $C_{12}$  and  $C_{decoupling}$ ), three resistors ( $R_2$ ,  $VR_2$  and  $R_2$ ) and three inductors ( $L_4$ ,  $L_5$  and  $L_6$ ).

[0073] The gate terminal ( $NM_3$ )<sub>G</sub> of the transistor  $NM_3$  is connected to inductor  $L_4$ . The source terminal ( $NM_3$ )<sub>S</sub> of the transistor  $NM_3$  is connected to the reference potential 406. The drain terminal ( $NM_3$ )<sub>D</sub> of the transistor  $NM_3$  is connected to resistor  $VR_2$ , inductor  $L_5$  and capacitor  $C_9$ . The resistor  $VR_2$  is in turn connected to the capacitor  $C_8$ . The capacitor  $C_8$  is in turn connected to the capacitor  $C_7$  and the inductor  $L_4$ .

[0074] The gate terminal ( $NM_4$ )<sub>G</sub> of the transistor  $NM_4$  is connected to capacitor  $C_{11}$  and the capacitor  $C_9$ . The source terminal ( $NM_4$ )<sub>S</sub> of the transistor  $NM_4$  is connected to capacitor  $C_{10}$  and the inductor  $L_5$ . The capacitor  $C_{10}$  is in turn connected to the reference potential 406. The drain terminal ( $NM_4$ )<sub>D</sub> of the transistor  $NM_4$  is connected to resistor  $R_2$ , resistor  $R_2$  and capacitor  $C_{12}$ . The other terminal of the capacitor  $C_{12}$  forms the output 414 (also denoted RFOUT) of the LNA 106.

[0075] The resistor  $R_2$  is connected to inductor  $L_6$ . The inductor  $L_6$  is in turn connected to capacitor  $C_{decoupling}$  and the reference potential 408. The capacitor

$C_{\text{decoupling}}$  is in turn connected to the reference potential 406. Sample values are as follows: ( $C_7=6$  pF,  $C_8=2.5$  pF,  $C_9=2.5$  pF,  $C_{10}=4$  pF,  $C_{11}=2$  pF,  $C_{12}=2.5$  pF,  $C_{\text{decoupling}}=100$  pF,  $L_4=L_5=L_6=1.43$  nH,  $R_{D2}=800$  ohm,  $V_{R2}=800$  ohm and  $R_2=20$  ohm)

[0076] The notch filter 104 (see Figure 1) is connected to the LNA 106 at port x. Thus, the notch filter 104 is connected to where the first amplification stage 402 connects to the second amplification stage 404. However, it will be appreciated that the notch filter 104 may also be connected at other points, such as the input of the first amplification stage 402 or the output of the second amplification stage 404.

[0077] Figure 5A shows a circuit level implementation, built in accordance to an embodiment of the present invention, of the notch filter 104 shown in Figure 1.

[0078] The notch filter 104 has a tunable active inductor portion 502. The tunable active inductor portion 502 has an active element 504 configurable to change a frequency rejection band of the notch filter 104.

[0079] Coupled to the tunable active inductor portion 502 are capacitors  $C_{\text{para}}$  and  $C_{\text{var}}$ .  $C_{\text{para}}$  is coupled to the tunable active inductor portion 502 via a switch SW1.  $C_{\text{var}}$  is in turn connected to port x of the LNA 106 (see Figure 4) to allow electrical communication between the notch filter 104 and the LNA 106. In the embodiment shown in Figure 5A,  $C_{\text{var}}$  is a varactor.

[0080] The active element 504 has a current mirror configuration. The current mirror configuration allows tuning an inductance value of the notch filter 104. In this manner, the current mirror configuration provides coarse tuning of the frequency rejection band of the notch filter 104.

[0081] The capacitive element  $C_{\text{var}}$  has one terminal connected to the current mirror configuration and an other terminal connected to the amplifier LNA 106 (see Figure 4) through port x. The capacitive element  $C_{\text{var}}$  provides fine tuning of the frequency rejection band of the notch filter 104.

[0082] The current mirror configuration includes two transistors  $NM_4$  and  $NM_5$ , and a biasing resistor network 506.

[0083] The gate terminal  $(NM_4)_G$  of the first transistor  $NM_4$  is connected to the gate terminal  $(NM_5)_G$  of the second transistor  $NM_5$ . Both the gate terminals  $(NM_4)_G$  and  $(NM_5)_G$  are connected to the source terminal  $(NM_5)_S$  of the second transistor

NM<sub>5</sub>. In this manner, a control terminal [(NM<sub>5</sub>)<sub>G</sub>] of the second transistor NM<sub>5</sub> is connected to a control terminal [(NM<sub>4</sub>)<sub>G</sub>] of the first transistor NM<sub>4</sub>. Also, the control terminal [(NM<sub>5</sub>)<sub>G</sub>] of the second transistor NM<sub>5</sub> is also connected to a first controlled terminal [(NM<sub>5</sub>)<sub>S</sub>] of the second transistor NM<sub>5</sub>.

[0084] Both the source terminals (NM<sub>4</sub>)<sub>S</sub> and (NM<sub>5</sub>)<sub>S</sub> of the first and the second transistors NM<sub>4</sub> and NM<sub>5</sub> are connected to the reference potential 406. Denoting potential V<sub>dd</sub> as a first reference potential 508 and reference potential 406 as a second reference potential, a second controlled terminal [(NM<sub>4</sub>)<sub>S</sub>] of the first transistor NM<sub>4</sub> is connected to a second reference potential; and wherein a second controlled terminal [(NM<sub>5</sub>)<sub>S</sub>] of the second transistor NM<sub>5</sub> is connected to the second reference potential.

[0085] The drain terminal (NM<sub>4</sub>)<sub>D</sub> of the second transistor NM<sub>4</sub> is connected to the capacitive element C<sub>var</sub>. In this manner, a first controlled terminal (NM<sub>4</sub>)<sub>D</sub> of the first transistor NM<sub>4</sub> is connected to the capacitive element C<sub>var</sub>.

[0086] A biasing resistor network 506 connects the first controlled terminal (NM<sub>5</sub>)<sub>D</sub> of the second transistor NM<sub>5</sub> to the first reference potential 508. The biasing resistor network 506 includes a plurality of resistors R<sub>1</sub> and R<sub>2</sub> arranged in parallel. Each of the plurality of resistors (R<sub>1</sub> and R<sub>2</sub>) is connected to the first reference potential 508. A switch SW2 connects to the first controlled terminal (NM<sub>5</sub>)<sub>D</sub> of the second transistor NM<sub>5</sub>. The switch SW2 is operable to connect the first controlled terminal (NM<sub>5</sub>)<sub>D</sub> of the second transistor NM<sub>5</sub> to the first reference potential 508 through connection via a selected one of the plurality of resistors (R<sub>1</sub> and R<sub>2</sub>).

[0087] The remainder of the tunable active inductor portion 502 includes transistors NM<sub>1</sub>, NM<sub>2</sub> and NM<sub>3</sub>; resistors R<sub>a</sub> and 510; a current source I<sub>2</sub> and capacitors C<sub>p</sub> and C<sub>a</sub>.

[0088] The gate terminal (NM<sub>1</sub>)<sub>G</sub> of the transistor NM<sub>1</sub> is connected to resistor R<sub>a</sub> and capacitor C<sub>a</sub>. The source terminal (NM<sub>1</sub>)<sub>S</sub> of the transistor NM<sub>1</sub> is connected to the capacitor C<sub>a</sub>, the capacitive element C<sub>var</sub>, the switch SW1, the drain terminal of the (NM<sub>4</sub>)<sub>D</sub> of the first transistor NM<sub>4</sub> [or the first controlled terminal (NM<sub>4</sub>)<sub>D</sub> of the first transistor NM<sub>4</sub>] and the gate terminal (NM<sub>2</sub>)<sub>G</sub> of the transistor NM<sub>2</sub>. The drain

terminal  $(NM_1)_D$  of the transistor  $NM_1$  is connected to resistor 510, current source  $I_2$  and the first reference potential 508.

[0089] The source terminal  $(NM_2)_S$  of the transistor  $NM_2$  is connected to the second reference potential (i.e. reference potential 406). The drain terminal  $(NM_2)_D$  of the transistor  $NM_2$  is connected to capacitor  $C_p$  and the source terminal  $(NM_3)_S$  of the transistor  $NM_3$ .

[0090] The gate terminal  $(NM_3)_G$  of the transistor  $NM_3$  is connected to the resistor 510 and the capacitor  $C_p$ . The drain terminal  $(NM_3)_D$  of the transistor  $NM_3$  is connected to the resistor  $R_a$  and the current source  $I_2$ .

[0091] In the embodiment shown in Figure 5A, the first reference potential 508 is of the same potential  $V_{dd}$  as the reference potential 408 of Figure 4. It will be appreciated that the first reference potential 508 may use another potential value.

[0092] The tunable active inductor portion 502 forms a third order active notch filter together with the capacitive elements  $C_{para}$  and  $C_{var}$ . The proposed active inductor has a capacitor gyrator (C-G) based grounded cascode topology and incorporates a modified implementation of the feedback loss-regulation technique. The loss compensation is achieved by transistor  $M_3$  which creates a series negative resistance which compensates for the losses due to the other active devices in the tunable active inductor 502.

[0093] The inductor value of the notch filter 104 is tunable by switching between the current mirror  $(NM_4, NM_5)$  biasing resistors  $R_1$  and  $R_2$  using switch  $SW_2$ . The control signal for the current mirror also controls switch  $SW_1$ . The current mirror topology provides a coarse tuning to the overall notch frequency of the notch filter 104.

[0094] On the other hand, fine tuning of the notch filter 104 is achieved by the varactor ( $C_{var}$ ) which can be controlled by an on-chip DAC (digital to analog converter).

[0095] Since both the inductance and the capacitance of the notch filter 104 are tunable, the active notch filter 104 can cover a much wider notch frequency range. In the embodiment shown in Figure 5A, the frequency rejection band of the notch filter 104 is around 2 GHz to around 3.6GHz.

[0096] Figure 5B shows an equivalent circuit diagram of the notch filter 104 shown in Figure 1.

[0097] As shown in Figure 5B, the tunable active inductor portion 502 can be represented by a RLC parallel configuration. The RLC parallel configuration includes resistors  $R_{in}$ ,  $R_{loss}$ , capacitor  $C_{in}$  and inductor  $L_{eq}$ . The resistor  $R_{loss}$  is connected in series with the inductor  $L_{eq}$ . Sample values are as follows: ( $C_{in}=0.5$  pF,  $L_{eq}=5$  nH,  $R_{in}=2$  ohm and  $R_{loss}=1$  ohm).

[0098] For the embodiments shown in Figures 5A and 5B, various parameters of the notch filter 104 can be derived from the following equations.

$$L_{eq} \approx \frac{C_a + C_{gs2}}{g_{m1}g_{m2}} \quad (4)$$

$$R_{loss} = \frac{g_{m2}g_{ds1}g_{ds3} + \omega^2 [g_{m3}C_{gs2}^2 - g_{m2}C_{gs2}S(\omega)]}{g_{m1}g_{m2}g_{m3} + \omega^2 g_{m1}g_{m3}C_{gs2}^2} \quad (5)$$

$$Q = \frac{\omega_0 L_{eq}}{R_{loss}} = \sqrt{\frac{g_{m1}g_{m2}g_{m3}(C_a + C_{gs2})}{C_{gs1}C_{ds1}g_{ds1}^2}} \quad (6)$$

$$f_{high\_notch} = \frac{1}{2\pi\sqrt{L_{eq\_low}C_{VAR}}} \quad (7)$$

$$f_{low\_notch} = \frac{1}{2\pi\sqrt{L_{eq\_high}(C_{para} + C_{VAR})}} \quad (8)$$

$C_{gs1}$  and  $C_{gs2}$  are the gate source capacitances of the transistors  $M_1$  and  $M_2$  respectively.  $C_{ds1}$  is the drain source capacitance of the transistor  $M_1$ .  $g_{m1}$ ,  $g_{m2}$  and  $g_{m3}$  are the transconductances of the transistors  $M_1$ ,  $M_2$  and  $M_3$  respectively.  $g_{ds1}$ ,  $g_{ds2}$  and  $g_{ds3}$  are physical drain conductances of the transistors  $M_1$ ,  $M_2$  and  $M_3$  respectively.  $L_{eq\_low}$  and  $L_{eq\_high}$  are respectively the lowest and highest inductance values of the notch filter 104, determined by which of the transistors  $NM_4$  and  $NM_5$  (see Figure 5A) of the current mirror configuration is instantaneously activated.  $Q$  is the quality factor of the notch filter 104. Sample values are as follows: ( $C_p=1$  pF,  $C_{para}=0.8$  pF,  $C_{var}=2$  pF,  $C_a=0.5$  pF,  $R_a=300$  ohm and resistance  $510=400$  ohm).

[0099] Thus, from the above, and returning to Figure 1, the receiver circuit 108 includes a notch filter (see for instance, notch filter 104 shown in Figure 5A),

wherein the notch filter includes an active element (see for instance, active element 504 having a current mirror configuration, shown in Figure 5A) configurable to change a frequency rejection band of the notch filter 104.

**[00100]** The front-end architecture 100 provides an integrated solution for inband and out-of-band interference rejection through the receiver circuit 108 and the antenna 102. The antenna 102 and the receiver circuit 108 work in conjunction to provide a high interference rejection. The antenna 102 and the receiver circuit 108 can be co-designed to achieve the desired inband/out-of-band interference mitigation.

**[00101]** In-band frequency refers to the range of around 3 to 5 GHz, while out-of-band frequency refers to the ranges below 3 GHz or above 5 GHz. As the notch filter of the receiver circuit 108 is tunable in the range of around 2 to around 3.6 GHz (i.e. overlapping the lower ranges of both the in-band frequency and the out-of-band frequency), the notch filter provides a tunable filter that operates in the in-band and out-of-band frequencies and may be used for unknown interference searching.

**[00102]** Figure 6 shows the measured normalized receiver front-end transfer function of a receiver circuit built in accordance to an embodiment of the present invention.

**[00103]** Figure 6 shows the front-end transfer functions 602 and 604 of the receiver circuit operating with notching at 3.2 GHz and 2.4 GHz respectively. To compare the band-notch performance at these two notch frequencies, each case is normalized to its maximum.

**[00104]** It can be seen a maximum attenuation of 40 dB and a minimum attenuation of 20 dB occurs at a frequency of 2.4 GHz. The maximum attenuation is achieved when the notch filter of the receiver circuit is tuned to this frequency. The maximum attenuation in the 5 GHz frequency band is around 35 dB at a 5.5 GHz frequency. The notch frequency band in the 5 GHz range, where attenuation greater than 20 dB occurs, is from 5.16 GHz to 5.82 GHz. The inband notch produced by the active notch filter is tunable between 1.9 GHz to 3.3 GHz, where the measured attenuation at 3.2 GHz is around 20 dB.

[00105] While the invention has been particularly shown and described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The scope of the invention is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced.

## CLAIMS

1. An antenna comprising:
  - a substrate;
  - a conductive layer formed on a portion of a top surface of the substrate;
  - a first slot formed within the conductive layer;
  - a conductive stub disposed within the first slot, the conductive stub tuned to reject a first frequency band; and
  - a second slot formed within the conductive layer, the second slot tuned to reject a second frequency band, wherein the first slot and the second slot have different shapes, and
  - wherein the conductive stub is connected to a segment of the first slot via a conductive strip, so that the conductive stub and the conductive strip form a T-shaped conductor.
2. The antenna of claim 1, wherein the conductive layer is disposed within the substrate, so that the conductive layer is surrounded by an area of exposed substrate.
3. The antenna of any one of the preceding claims, wherein the second slot is adjacent to a portion of a perimeter of the conductive layer.
4. The antenna of any one of the preceding claims, further comprising
  - a ground plane formed on a portion of the bottom surface of the substrate,wherein a gap exists between the ground plane and a portion on the bottom surface of the substrate corresponding to where the conductive layer is formed on the portion of the top surface of the substrate.
5. The antenna of any one of the preceding claims, wherein the conductive layer has any one of the following shapes circular, trapezoidal or elliptical.

6. The antenna of any one of the preceding claims, wherein the first slot has any one of the following shapes circular, rectangular or elliptical.

7. The antenna of claims 1 to 4, wherein the conductive layer has a circular shape and the first slot has a circular shape with a radius smaller than a radius of the conductive layer.

8. The antenna of any one of the preceding claims, wherein the second slot has any one of the following shapes arc, arrowhead or polygonal.

9. The antenna of claim 1, wherein the conductive stub is tuned according to the expression

$$f_{notch1} = \frac{c}{4\sqrt{\epsilon_r}(L_1 + h)}$$

where  $f_{notch1}$  is the rejected first frequency band,  $c$  is the speed of light,  $\epsilon_r$  is the substrate dielectric constant,  $L_1$  the length of the T-shaped conductor and  $h$  is the shortest gap between a feed point of the conductive layer and a portion on the top surface of the substrate corresponding to where a ground plane is formed on the portion of a bottom surface of the substrate.

10. The antenna of any one of the preceding claims, wherein the second slot is tuned according to the expression

$$f_{notch2} = \frac{c}{2L_{slot}\sqrt{\epsilon_r}}$$

where  $f_{notch2}$  is the rejected second frequency band,  $c$  is the speed of light,  $\epsilon_r$  is the substrate dielectric constant and  $L_{slot}$  is the length of the second slot.

11. The antenna of any one of the preceding claims, wherein the antenna is adapted to operate in the UWB range, wherein the rejected first frequency band is around 5.2 GHz and the rejected second frequency band is around 2.4 GHz.

12. A receiver circuit comprising  
an antenna as claimed in any one of the preceding claims;  
an amplifier connected to the antenna; and  
a notch filter connected to the amplifier.
13. The receiver circuit of claim 12, wherein the notch filter comprises an active element configurable to change a frequency rejection band of the notch filter.
14. The receiver circuit of claim 13, wherein the active element has a current mirror configuration, the current mirror configuration allowing tuning an inductance value of the notch filter, the current mirror configuration providing coarse tuning of the frequency rejection band of the notch filter.
15. The receiver circuit of claim 14, wherein the notch filter further comprises a capacitive element with one terminal connected to the current mirror configuration and an other terminal connected to the amplifier, the capacitive element providing fine tuning of the frequency rejection band of the notch filter.
16. The receiver circuit of claim 15, wherein the capacitive element is a varactor.
17. The receiver circuit of claims 15 to 16, wherein the current mirror configuration comprises:  
a first transistor, a first controlled terminal of which connected to the capacitive element; and  
a second transistor, a control terminal of which connected to a control terminal of the first transistor, the control terminal of the second transistor also connected to a first controlled terminal of the second transistor.
18. The receiver circuit of claim 17, wherein the notch filter further comprises a biasing resistor network to connect the first controlled terminal of the second transistor to a first reference potential.

19. The receiver circuit of claim 18, wherein the biasing resistor network comprises a plurality of resistors arranged in parallel, each of the plurality of resistors connected to the first reference potential; and  
a switch connected to the first controlled terminal of the second transistor, the switch operable to connect the first controlled terminal of the second transistor to the first reference potential through connection via a selected one of the plurality of resistors.
20. The receiver circuit of claims 17 to 19, wherein a second controlled terminal of the first transistor is connected to a second reference potential; and wherein a second controlled terminal of the second transistor is connected to the second reference potential.
21. The receiver circuit of claims 12 to 20, wherein the frequency rejection band of the notch filter is around 2 GHz to around 3.6GHz.
22. The receiver circuit of claims 12 to 21, wherein the amplifier further comprises:  
a first amplification stage; and  
a second amplification stage, wherein an output of the first amplification stage is connected to an input of the second amplification stage and wherein the notch filter is connected to where the first amplification stage connects to the second amplification stage.
23. The receiver circuit of claims 12 to 22, wherein the amplifier further comprises a serial resonance network, the serial resonance network determining a frequency rejection band of the amplifier.
24. The receiver circuit of claim 23, wherein the serial resonance network comprises an inductor and a capacitor connected in series.
25. The receiver circuit of claims 23 to 24, wherein the frequency rejection band of the amplifier is around 1.8 GHz.