FIG. 1

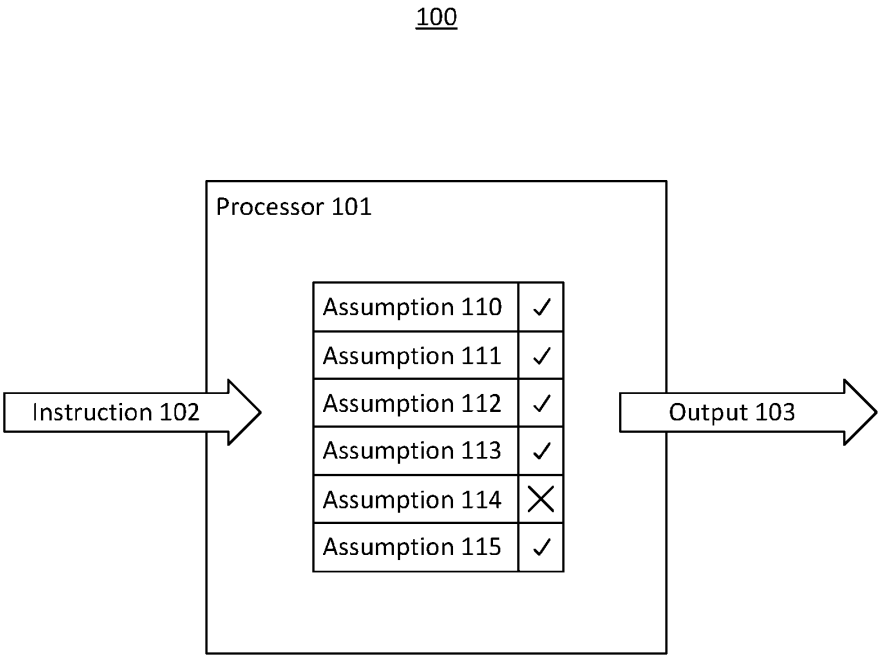

100
Processor 101
Assumption 110
Assumption 111
Assumption 112
Assumption 113
Assumption 114
Assumption 115
Instruction 102
Output 103

FIG. 2

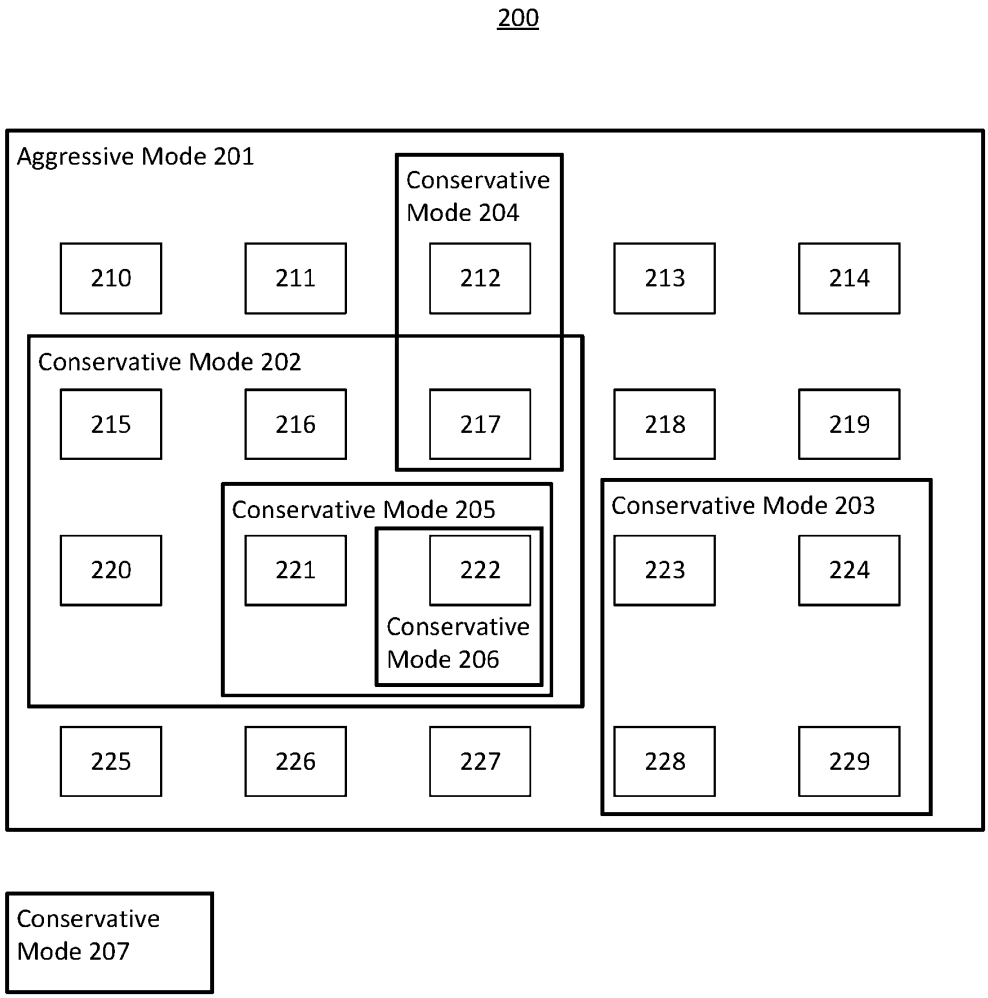

200
Aggressive Mode 201
Conservative Mode 204
210
211
212
213
214
Conservative Mode 202
215
216
217
218
219
Conservative Mode 205
Conservative Mode 203
220
221
222
223
224
Conservative Mode 206
225
226
227
228
229
Conservative Mode 207

FIG. 3

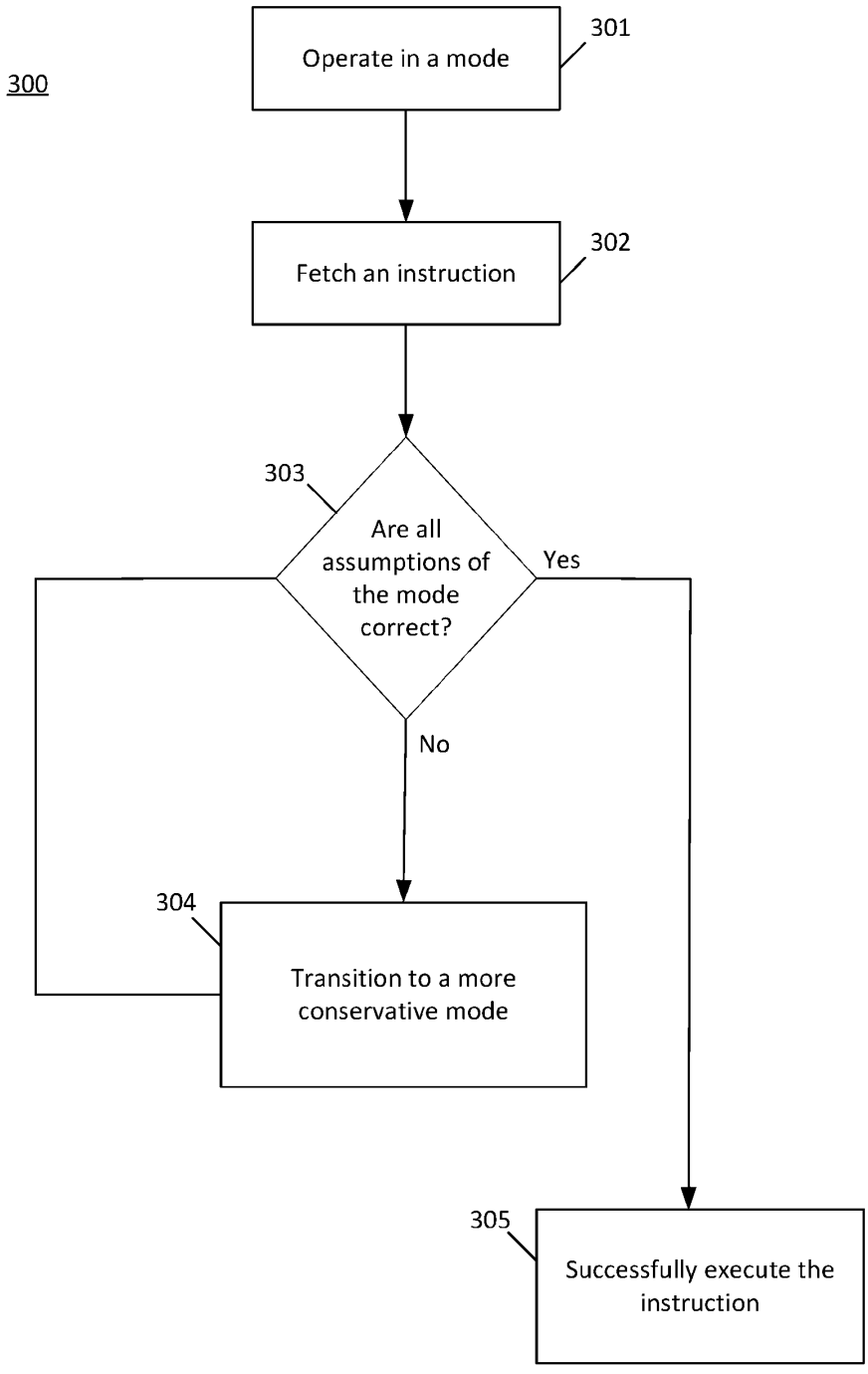

300
Operate in a mode
301
Fetch an instruction
302
303
Are all assumptions of the mode correct?
Yes
No
304
Transition to a more conservative mode
305
Successfully execute the instruction

FIG. 4

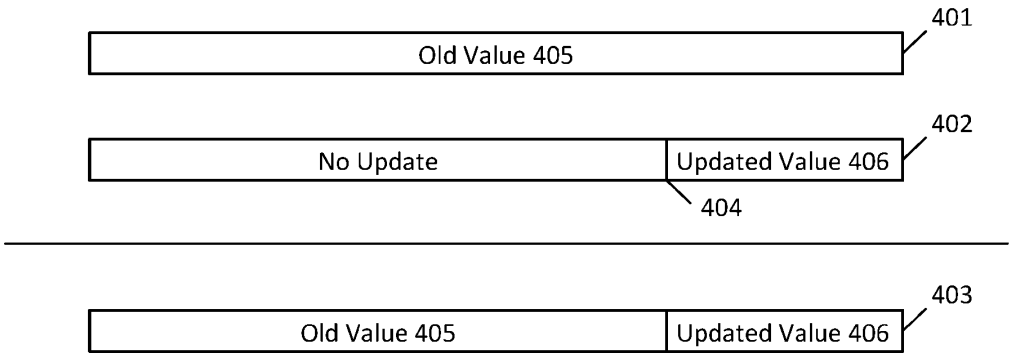

401
Old Value 405
402
No Update
Updated Value 406
404
403
Old Value 405
Updated Value 406

FIG. 5

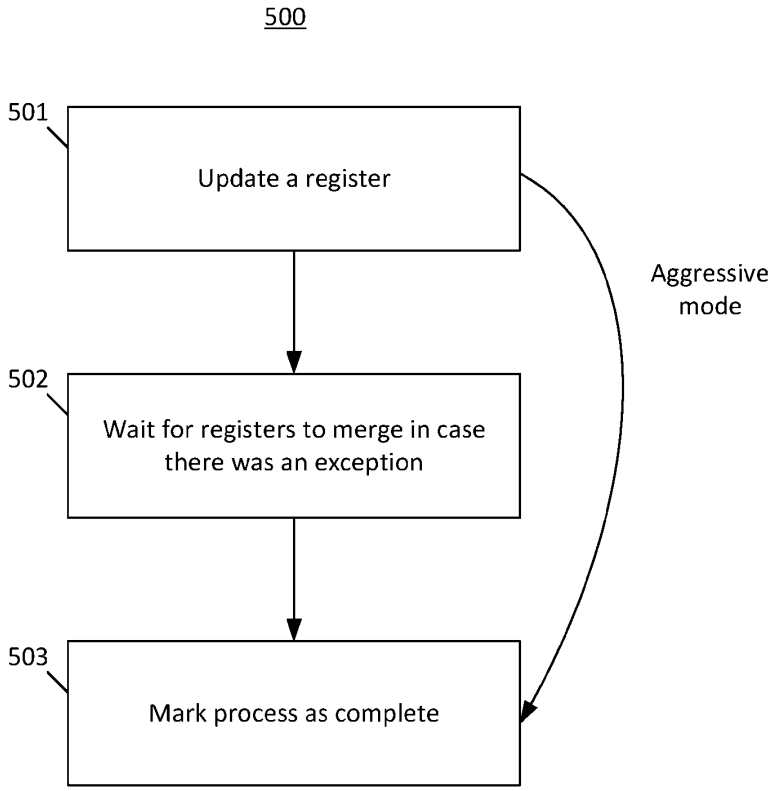

500
501
Update a register
Aggressive mode
502
Wait for registers to merge in case there was an exception
503
Mark process as complete

FIG. 6

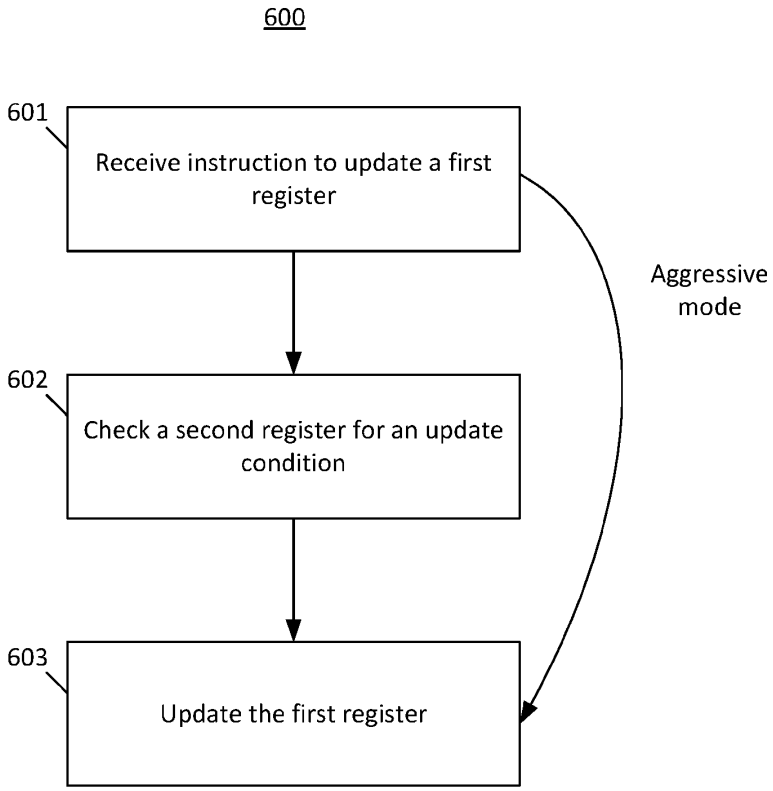

600
601
Receive instruction to update a first register
Aggressive mode
602
Check a second register for an update condition
603
Update the first register

FIG. 7

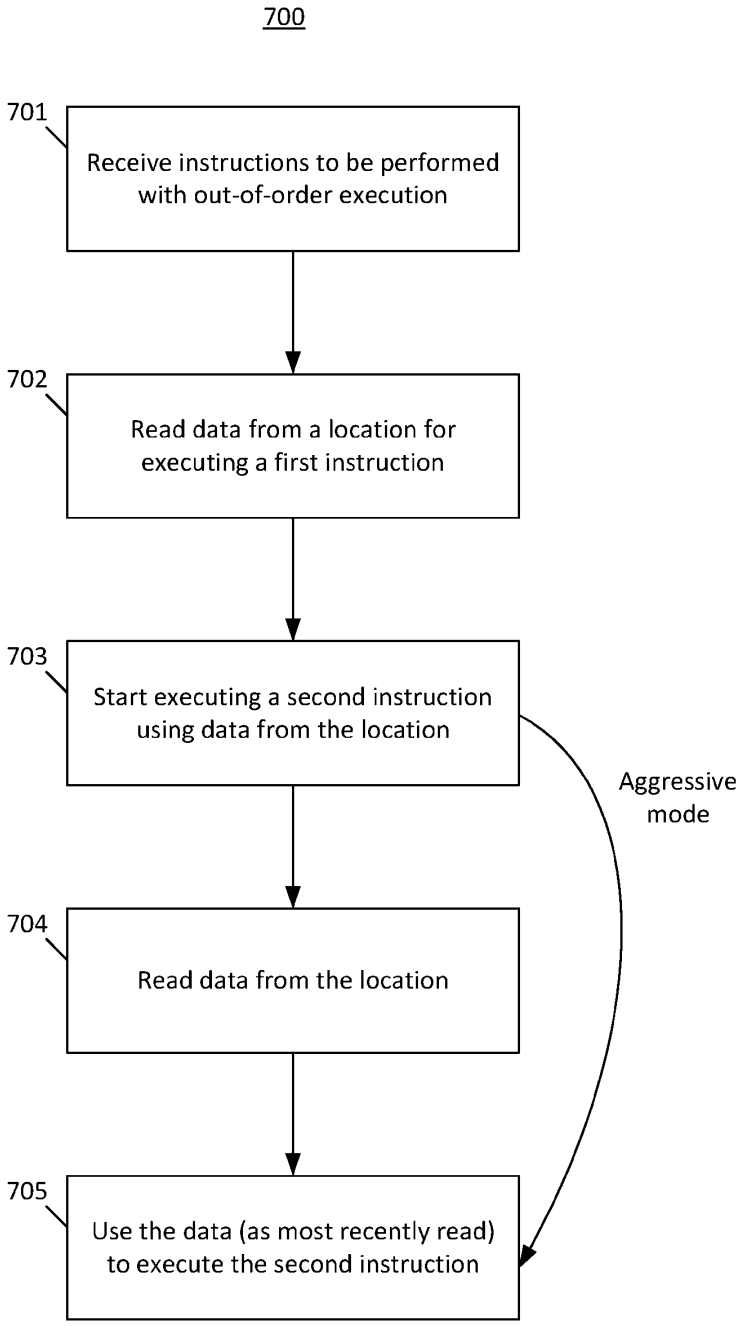
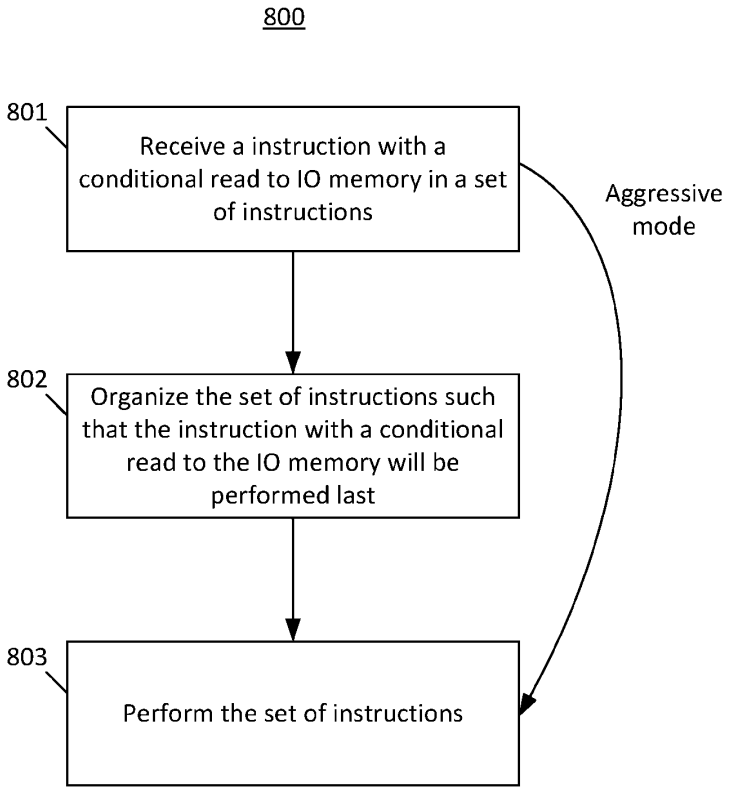

700
701
Receive instructions to be performed with out-of-order execution
702
Read data from a location for executing a first instruction
703
Start executing a second instruction using data from the location
Aggressive mode
704
Read data from the location
705
Use the data (as most recently read) to execute the second instruction

FIG. 8


800
801
Receive a instruction with a conditional read to IO memory in a set of instructions
Aggressive mode
802
Organize the set of instructions such that the instruction with a conditional read to the IO memory will be performed last
803
Perform the set of instructions