(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
23 September 2004 (23.09.2004)

PCT

(10) International Publication Number
WO 2004/082017 A1

(51) International Patent Classification[7]: H01L 21/768

(21) International Application Number:
PCT/US2004/006388

(22) International Filing Date: 2 March 2004 (02.03.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/383,318 7 March 2003 (07.03.2003) US

(71) Applicant *(for all designated States except US)*: **ADVANCED MICRO DEVICES, INC.** [US/US]; One AMD Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **WANG, Pin-Chin, Connie** [US/US]; 461 Burgess Drive, Unit #2, Menlo Park, CA 94025 (US). **HUANG, Richard, J.** [US/US]; 1068 West Hill Court, Cupertino, CA 95014 (US).

(74) Agent: **COLLOPY, Daniel, R.**; One AMD Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).

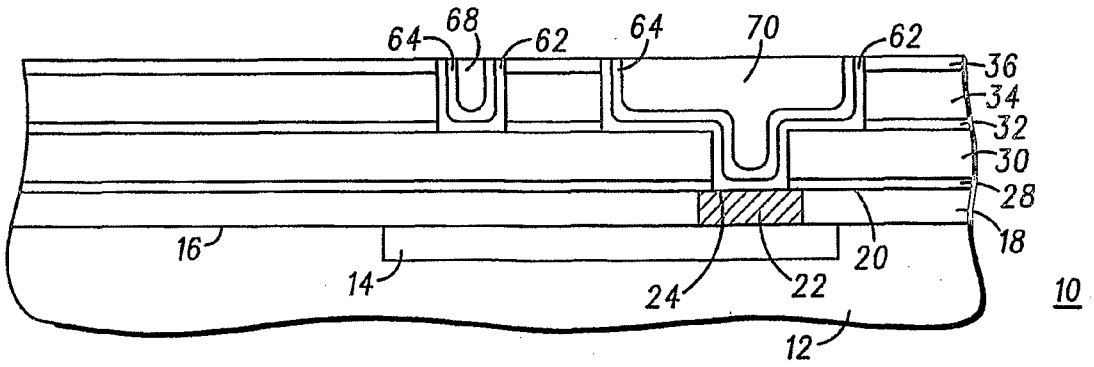
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD FOR MANUFACTURING A SEMICONDUCTOR COMPONENT HAVING A BARRIER-LINED OPENING



(57) Abstract: A semiconductor component (10) having a metallization system that includes a thin conformal multilayer barrier structure (60) and a method for manufacturing the semiconductor component (10). A layer of dielectric material (30, 34) is formed over a lower level interconnect. A hardmask (36) is formed over the dielectric layer (30, 34) and an opening (50, 52, 54) is etched through the hardmask (36) into the dielectric layer (30, 34). The opening (50, 52, 54) is lined with a thin conformal multi-layer barrier (60) using atomic layer deposition. The multi-layer barrier lined opening is filled with an electrically conductive material (66) which is planarized.

WO 2004/082017 A1