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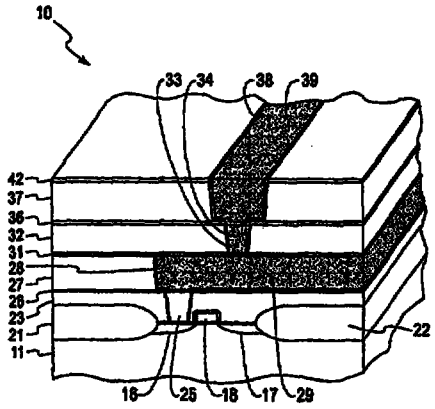
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(54) Title: REDUCED ELECTROMIGRATION AND STRESS INDUCED MIGRATION OF Cu WIRES BY SURFACE COATING



(57) Abstract: The idea of the invention is to coat the free surface of patterned Cu conducting lines (60, 70) in on-chip interconnections (BEOL) wiring by a 1-20 nm thick metal layer (63, 74) prior to deposition of the interlevel dielectric. This coating is sufficiently thin so as to obviate the need for additional planarization by polishing, while providing protection against oxidation and surface, or interface, diffusion of Cu which has been identified by the inventors as the leading contributor to metal line failure by electromigration and thermal stress voiding. Also, the metal layer (63, 74) increases the adhesion strength between the Cu (60, 70) and dielectric (66) so as to further increase lifetime and facilitate process yield. The free surface is a direct result of the CMP (chemical mechanical polishing) in a damascene process or in a dry etching process by which Cu wiring is patterned. It is proposed that the metal capping layer (63, 74) be deposited by a selective process onto the Cu to minimize further processing. We have used electroless metal coatings, such as CoWP, CoSnP and Pd, to illustrate significant reliability benefits, although chemical vapor deposition (CVD) of metals or metal forming compounds can be employed.

WO 01/08213 A1