

ABSTRACT

A semiconductor memory device includes a stack structure including a plurality of layers stacked on a substrate in a vertical direction, and bit lines disposed at a side of the stack structure and extending in the vertical direction. The plurality of layers include semiconductor patterns, gate electrodes extending from the semiconductor patterns in a first horizontal direction, and information storage elements adjacent to the semiconductor patterns in a second horizontal direction crossing the first horizontal direction. The semiconductor patterns include first impurity regions adjacent to the bit lines, second impurity regions adjacent to the information storage elements, and channel regions between the first impurity regions and the second impurity regions. The information storage elements include first electrodes adjacent to the second impurity regions. A portion of the stack structure includes metal silicides disposed between the second impurity regions at a side of the semiconductor patterns and the first electrodes.

FIG. 6