WHAT IS CLAIMED IS:

1. An integrated circuit formed in a semiconductor substrate, comprising:
a first static random access memory (SRAM) cell having a first cell size; and
a second SRAM cell having a second cell size greater than the first cell size, wherein:
the first SRAM cell includes first n-type field effect transistors (nFETs) each having a first gate stack, and
the second SRAM cell includes second nFETs each having a second gate stack different from the first gate stack.

2. The integrated circuit of claim 1, wherein the second gate stack is different from the first gate stack in at least one of gate electrode material, gate dielectric material, and gate dielectric thickness.

3. The integrated circuit of claim 1, wherein:
the first SRAM cell includes a first number N1 of the first nFETs;
the second SRAM cell includes a second number N2 of the second nFETs; and
the second number N2 is greater than the first number N1.

4. The integrated circuit of claim 1, wherein:
the first SRAM cell includes:
first two pull-up devices,
first two pull-down devices configured with the first two pull-up devices to form first two cross-coupled inverters for data storage, and
first two pass-gate devices configured with the first two cross-coupled inverters to form first ports for data access;
the second SRAM cell includes:
second two pull-up devices,

second two pull-down devices configured with the second two pull-up devices to form second two cross-coupled inverters for data storage; and

second two pass-gate devices configured with the second two cross-coupled inverters to form second ports for data access; and

wherein the first and second SRAM cells each include a plurality of fin-like field-effect transistors (FinFETs).

5. The integrated circuit of claim 4, wherein:

each of the first two pull-up devices and the second two pull-up devices includes a single p-type fin-like field-effect transistor (pFinFET);

each of the first two pull-down devices and the first two pass-gate devices includes a single n-type FinFET (nFinFET); and

each of the second two pull-down devices and the second two pass-gate devices includes a plurality of n-type FinFETs (nFinFETs).

6. The integrated circuit of claim 4 further comprising a write-assist circuitry connected to the first two pull-up devices.

7. The integrated circuit of claim 1, wherein:

the first SRAM cell has a first alpha ratio ranging within 0.8 and 1.3; and

the second SRAM cell has a second alpha ratio ranging within 0.2 and 0.6.

8. The integrated circuit of claim 1, wherein:

the first nFETs each include a first p-type well (p-well) and a first channel region;

the second nFETs each include a second p-type well (p-well) and a second channel region; and

at least one of the first p-well and the first channel is different from respective one of the second p-well and the second channel.

9. An integrated circuit, comprising:

a first static random access memory (SRAM) cell having a first cell size on a substrate, wherein the first SRAM cell includes:

first and second pull-up devices each having only one of first p-type field effect transistors (pFETs),

first and second pull-down devices configured with the first and second pull-up devices to form first two cross-coupled inverters for data storage, and

first and second pass-gate devices configured with the first two cross-coupled inverters for data access, wherein the first and second pull-down devices and the first and second pass-gate devices each include only one of first n-type field effect transistors (nFETs); and

a second SRAM cell on the substrate having a second cell size greater than the first cell size, wherein the second SRAM cell includes:

third and fourth pull-up devices each having only one of second pFETs,

third and fourth pull-down devices configured with the third and fourth pull-up devices to form second two cross-coupled inverters for data storage, and

third and fourth pass-gate devices configured with the second two cross-coupled inverters for data access, wherein the third and fourth pull-down devices and the third and fourth pass-gate devices each include at least two of second nFETs, wherein the second nFETs are different from the first nFETs.

10. The integrated circuit of claim 9, wherein:

the first nFETs have a first threshold voltage, and

the second nFETs have a second threshold voltage different from the first threshold voltage.

11. The integrated circuit of claim 9, wherein

the first nFETs each include a first gate stack, and

the second nFETs each include a second gate stack different from the first gate stack in at least one of gate electrode material, gate dielectric material, and gate dielectric thickness.

12. The integrated circuit of claim 9, wherein the second nFETs are different from the first nFETs in at least one of channel doping concentration, p-well dimension, and p-well doping concentration.

13. The integrated circuit of claim 9, wherein:

the first nFETs each include a first n-type light doped drain (NLDD) feature and a first pocket doping feature adjacent the first NLDD feature;

the second nFETs each include a second NLDD feature and a second pocket doping feature adjacent the second NLDD feature; and

at least one of the first NLDD feature and the first pocket doping feature is different from respective one of the second NLDD feature and the second pocket doping feature.

14. The integrated circuit of claim 9, wherein:

the first pFETs each include a first gate stack; and

the second pFETs each include a second gate stack different from the first gate stack in at least one of gate electrode material, gate dielectric material, and gate dielectric thickness.

15. The integrated circuit of claim 9, wherein the second cell size is at least 10% greater than the first cell size.

16. The integrated circuit of claim 9, further comprising a write-assist circuitry connected to the first and second pull-up devices.

17. The integrated circuit of claim 9, wherein:

the first SRAM cell has a first alpha ratio ranging within 0.8 and 1.3; and

the second SRAM cell has a second alpha ratio ranging within 0.2 and 0.6.

18. A method comprising:

forming a first static random access memory (SRAM) cell of a first cell size on a substrate, wherein the forming of the first SRAM cell includes forming first n-type fin field-effect transistors (nFinFETs) using a first nFinFET formation process; and

forming a second SRAM cell of a second cell size on the substrate, wherein the forming of the second SRAM cell includes forming second nFinFETs using a second nFinFET formation process different from the first nFinFET formation process, wherein the second cell size is greater than the first cell size.

19. The method of claim 18, wherein:

the first nFinFET formation process includes

forming a first p-well using a first p-well doping dose and with a first p-well dimension,

forming a first channel region in the first p-well using a first channel doping dose,

forming a first n–type light doped drain (NLDD) feature in the first p-well and interposed by the first channel region, using a first NLDD doping dose,

forming a first pocket doping feature adjacent the first NLDD feature using a first pocket doping dose,

forming a first gate dielectric layer on the first channel region, with a first gate dielectric material and a first gate dielectric thickness, and

forming a first gate electrode on the first gate dielectric layer using a first gate electrode material;

the second nFinFET formation process includes:

forming a second p-well using a second p-well doping dose and with a second p-well dimension,

forming a second channel region in the second p-well using a second channel doping dose,

forming a second n–type light doped drain (NLDD) feature in the second p-well and interposed by the second channel region, using a second NLDD doping dose,

forming a second pocket doping feature adjacent the second NLDD feature using a second pocket doping dose,

forming a second gate dielectric layer on the second channel region, with a second gate dielectric material and a second gate dielectric thickness, and

forming a second gate electrode on the second gate dielectric layer using a second gate electrode material; and

wherein at least one of the first p-well doping dose, the first p-well dimension, the first channel doping dose, the first NLDD doping dose, the first pocket doping dose, the first gate dielectric material, the first gate dielectric thickness, and the first gate electrode material is different from respective one of the second p-well doping dose, the second p-well dimension, the second channel doping dose, the second NLDD doping dose, the second pocket doping dose, the second gate dielectric material, the second gate dielectric thickness, and the second gate electrode material.

20. The method of claim 18, further comprising forming a write assist circuitry, wherein:

the forming of the first SRAM cell includes forming first p-type fin field-effect transistors (pFinFETs);

the forming of the second SRAM cell includes forming second pFinFETs; and

the forming of the write assist circuitry includes forming the write assist circuitry connected to the first pFinFETs.

CLAIMS

1. An integrated circuit formed in a semiconductor substrate, comprising:

a first static random access memory (SRAM) cell having a first cell size; and

a second SRAM cell having a second cell size greater than the first cell size, wherein:

the first SRAM cell includes first n-type field effect transistors (nFETs) each having a first gate stack, and

the second SRAM cell includes second nFETs each having a second gate stack different from the first gate stack, wherein the second gate stack is different from the first gate stack in at least one of gate electrode material, gate dielectric material, and gate dielectric thickness.

2. The integrated circuit of claim 1, wherein:

the first SRAM cell includes a first number N1 of the first nFETs;

the second SRAM cell includes a second number N2 of the second nFETs; and

the second number N2 is greater than the first number N1.

3. The integrated circuit of claim 1, wherein:

the first SRAM cell includes:

first two pull-up devices,

first two pull-down devices configured with the first two pull-up devices to form first two cross-coupled inverters for data storage, and

first two pass-gate devices configured with the first two cross-coupled inverters to form first ports for data access;

the second SRAM cell includes:

second two pull-up devices,

second two pull-down devices configured with the second two pull-up devices to form second two cross-coupled inverters for data storage; and

second two pass-gate devices configured with the second two cross-coupled inverters to form second ports for data access; and

wherein the first and second SRAM cells each include a plurality of fin-like field-effect transistors (FinFETs).

4. The integrated circuit of claim 3, wherein:

each of the first two pull-up devices and the second two pull-up devices includes a single p-type fin-like field-effect transistor (pFinFET);

each of the first two pull-down devices and the first two pass-gate devices includes a single n-type FinFET (nFinFET); and

each of the second two pull-down devices and the second two pass-gate devices includes a plurality of n-type FinFETs (nFinFETs).

5. The integrated circuit of claim 4, further comprising a write-assist circuitry connected to the first two pull-up devices.

6. The integrated circuit of claim 1, wherein:

the first SRAM cell has a first alpha ratio ranging within 0.8 and 1.3; and

the second SRAM cell has a second alpha ratio ranging within 0.2 and 0.6.

7. The integrated circuit of claim 1, wherein:

the first nFETs each include a first p-type well (p-well) and a first channel region;

the second nFETs each include a second p-type well (p-well) and a second channel region; and

at least one of the first p-well and the first channel is different from respective one of the second p-well and the second channel.

8. An integrated circuit, comprising:

a first static random access memory (SRAM) cell having a first cell size on a substrate, wherein the first SRAM cell includes:

first and second pull-up devices each having only one of first p-type field effect transistors (pFETs),

first and second pull-down devices configured with the first and second pull-up devices to form first two cross-coupled inverters for data storage, and

first and second pass-gate devices configured with the first two cross-coupled inverters for data access, wherein the first and second pull-down devices and the first and second pass-gate devices each include only one of first n-type field effect transistors (nFETs); and

a second SRAM cell on the substrate having a second cell size greater than the first cell size, wherein the second SRAM cell includes:

third and fourth pull-up devices each having only one of second pFETs,

third and fourth pull-down devices configured with the third and fourth pull-up devices to form second two cross-coupled inverters for data storage, and third and fourth pass-gate devices configured with the second two cross-coupled inverters for data access, wherein the third and fourth pull-down devices and the third and fourth pass-gate devices each include at least two of second nFETs,

wherein the second nFETs are different from the first nFETs.

9. The integrated circuit of claim 8, wherein:

the first nFETs have a first threshold voltage, and

the second nFETs have a second threshold voltage different from the first threshold voltage.

10. The integrated circuit of claim 8, wherein the first nFETs each include a first gate stack, and the second nFETs each include a second gate stack different from the first gate stack in at least one of gate electrode material, gate dielectric material, and gate dielectric thickness.

11. The integrated circuit of claim 8, wherein the second nFETs are different from the first nFETs in at least one of channel doping concentration, p-well dimension, and p-well doping concentration.

12. The integrated circuit of claim 8, wherein:

the first nFETs each include a first n-type light doped drain (NLDD) feature and a first pocket doping feature adjacent the first NLDD feature;

the second nFETs each include a second NLDD feature and a second pocket doping feature adjacent the second NLDD feature; and

at least one of the first NLDD feature and the first pocket doping feature is different from respective one of the second NLDD feature and the second pocket doping feature.

13. The integrated circuit of claim 8, wherein:

the first pFETs each include a first gate stack; and

the second pFETs each include a second gate stack different from the first gate stack in at least one of gate electrode material, gate dielectric material, and gate dielectric thickness.

14. The integrated circuit of claim 8, wherein the second cell size is at least 10% greater than the first cell size.

15. The integrated circuit of claim 8, further comprising a write-assist circuitry connected to the first and second pull-up devices.

16. The integrated circuit of claim 8, wherein:

the first SRAM cell has a first alpha ratio ranging within 0.8 and 1.3; and

the second SRAM cell has a second alpha ratio ranging within 0.2 and 0.6.

17. An integrated circuit formed in a semiconductor substrate, comprising:

a first static random access memory (SRAM) cell having:

first two pull-up devices,

first two pull-down devices configured with the first two pull-up devices to form first two cross-coupled inverters for data storage, and

first two pass-gate devices configured with the first two cross-coupled inverters to form first ports for data access; and

a second SRAM cell having:

second two pull-up devices,

second two pull-down devices configured with the second two pull-up devices to form second two cross-coupled inverters for data storage; and

second two pass-gate devices configured with the second two cross-coupled inverters to form second ports for data access; and

wherein:

the first two pull-down devices and the first two pass-gate devices each include a first number of first n-type field effect transistors (nFETs)

the second two pull-down devices and the second two pass-gate devices each include a second number of second nFETs;

the first number is smaller than the second number; and

the first nFETs are different from the second nFETs.

18. The integrated circuit of claim 17, wherein the first nFETs are different from the second nFETs in at least one of: gate stack, channel doping concentration, p-well dimension, and p-well doping concentration.

19. The integrated circuit of claim 17, wherein:

the first two pull-up devices each include only one of first p-type field effect transistors (pFETs);

the second two pull-up devices each include only one of second pFETs; and

the first and second pFETs have different gate stacks.

20. The integrated circuit of claim 17, wherein the first SRAM cell has a first cell size and the second SRAM cell has a second cell size, and

wherein the second cell size is at least 10% greater than the first cell size.