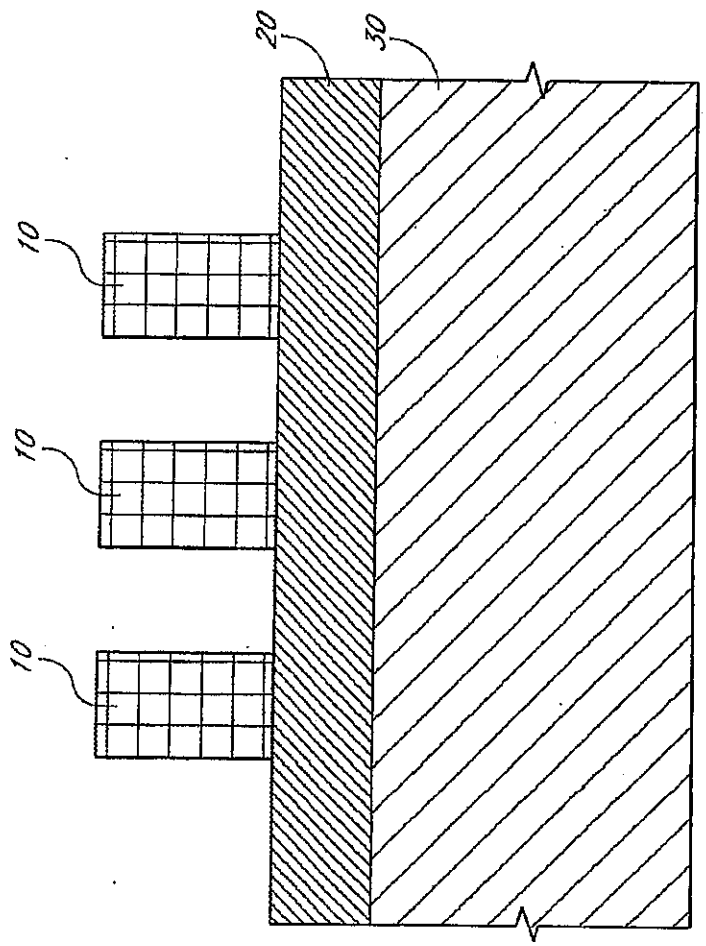


FIG. 1A
(PRIOR ART)

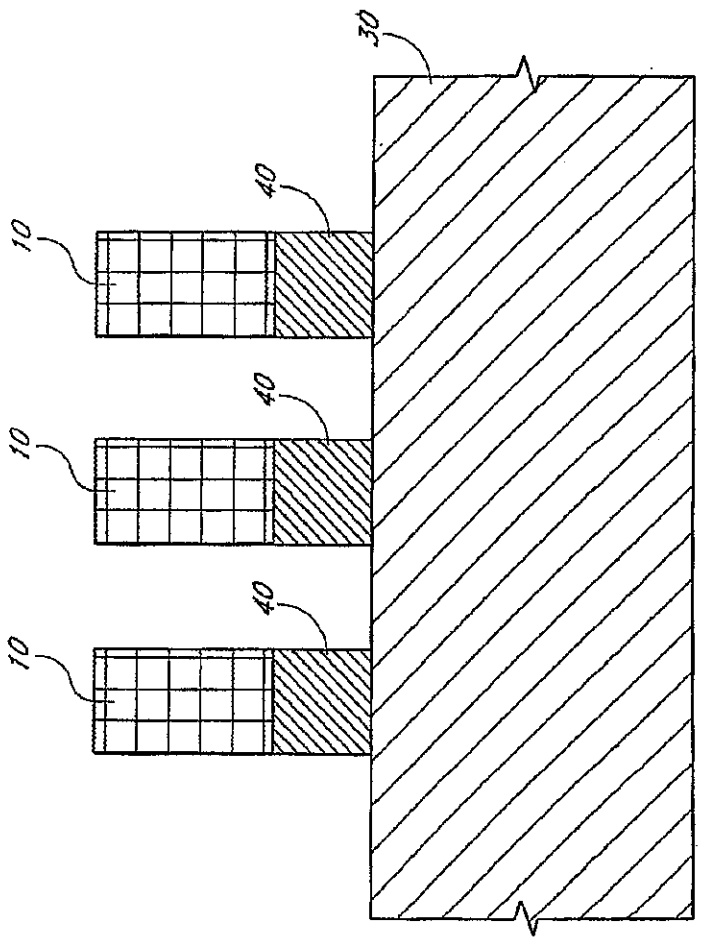


FIG. 1B
(PRIOR ART)

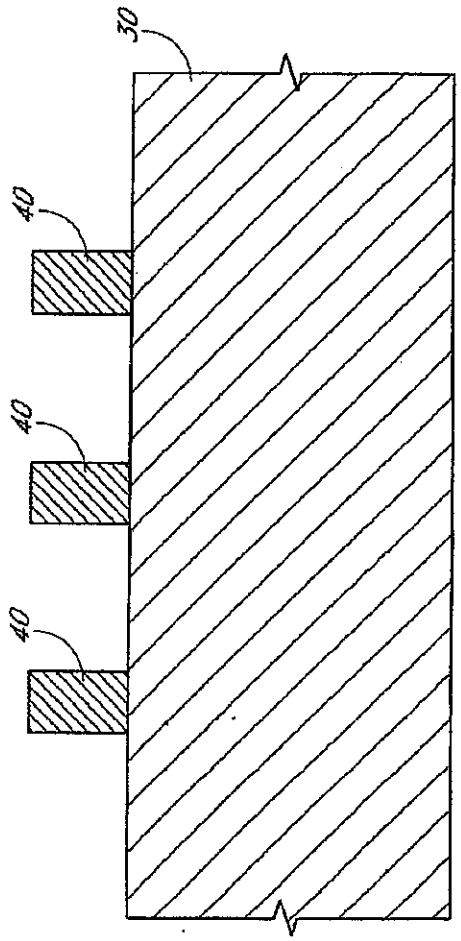


FIG. 1C
(PRIOR ART)

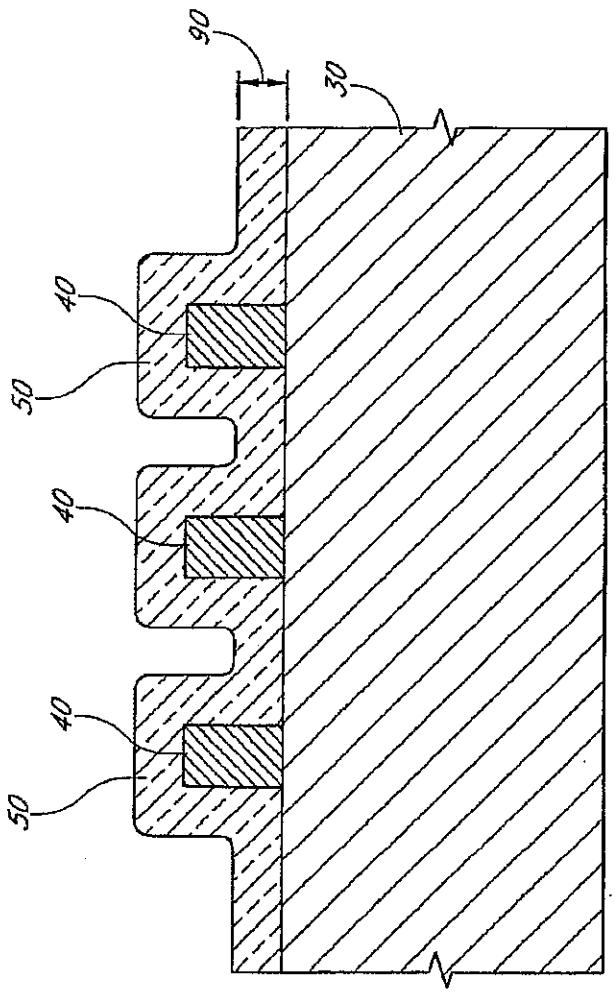


FIG. 1D
(PRIOR ART)

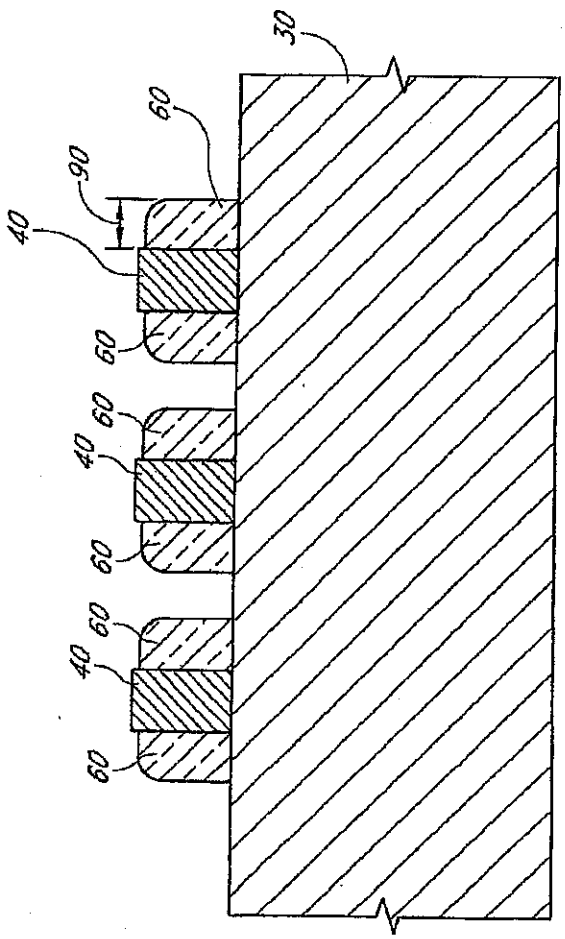


FIG. 1E
(PRIOR ART)

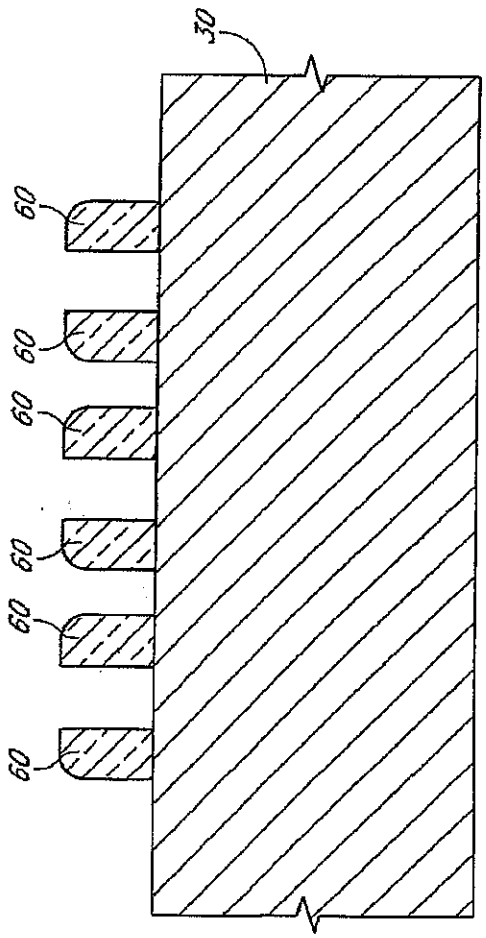


FIG. 1F
(PRIOR ART)

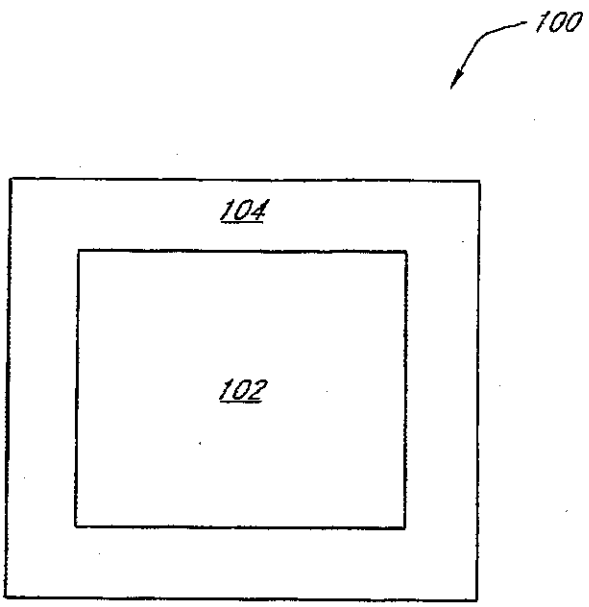


FIG. 2

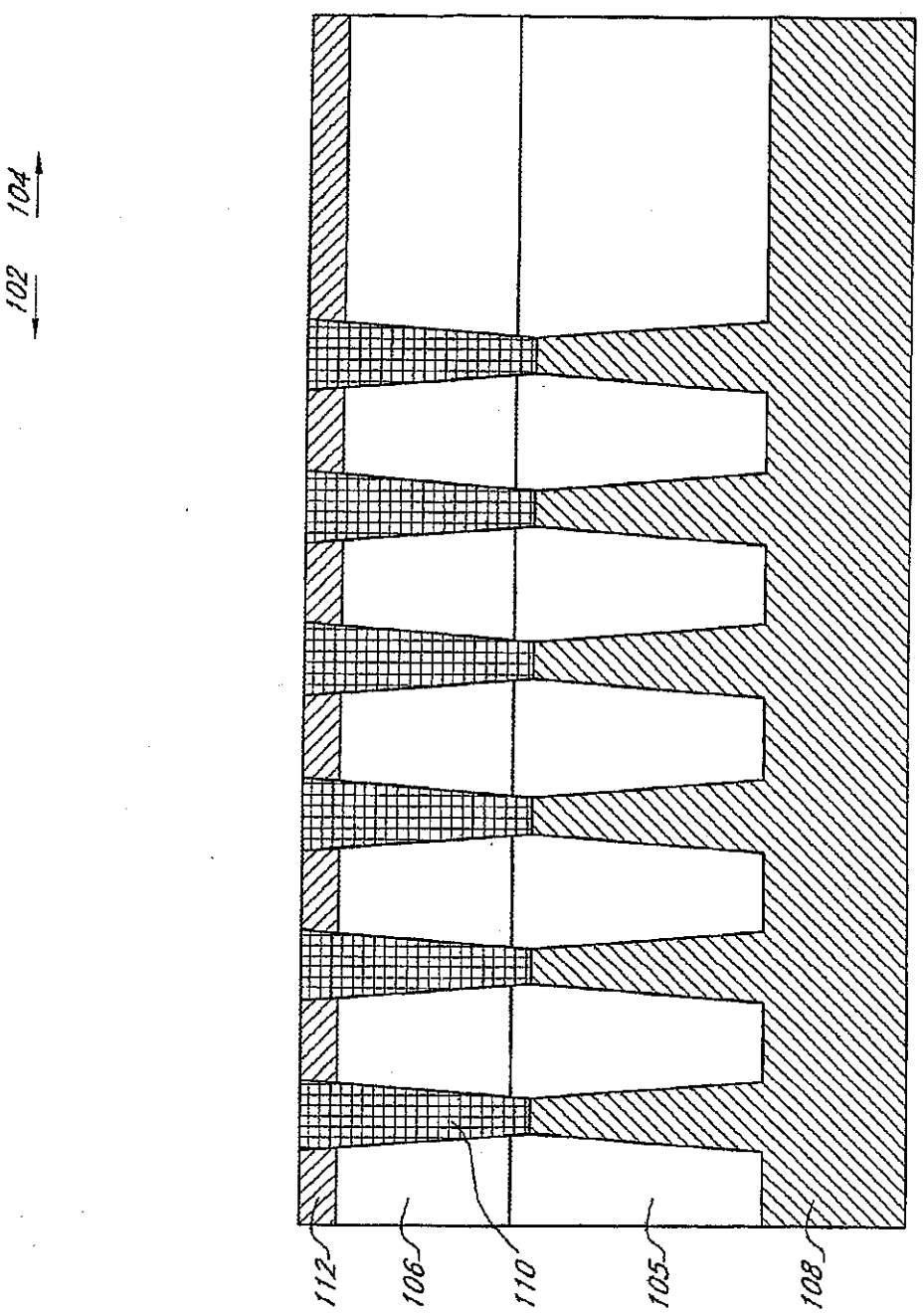


FIG. 3

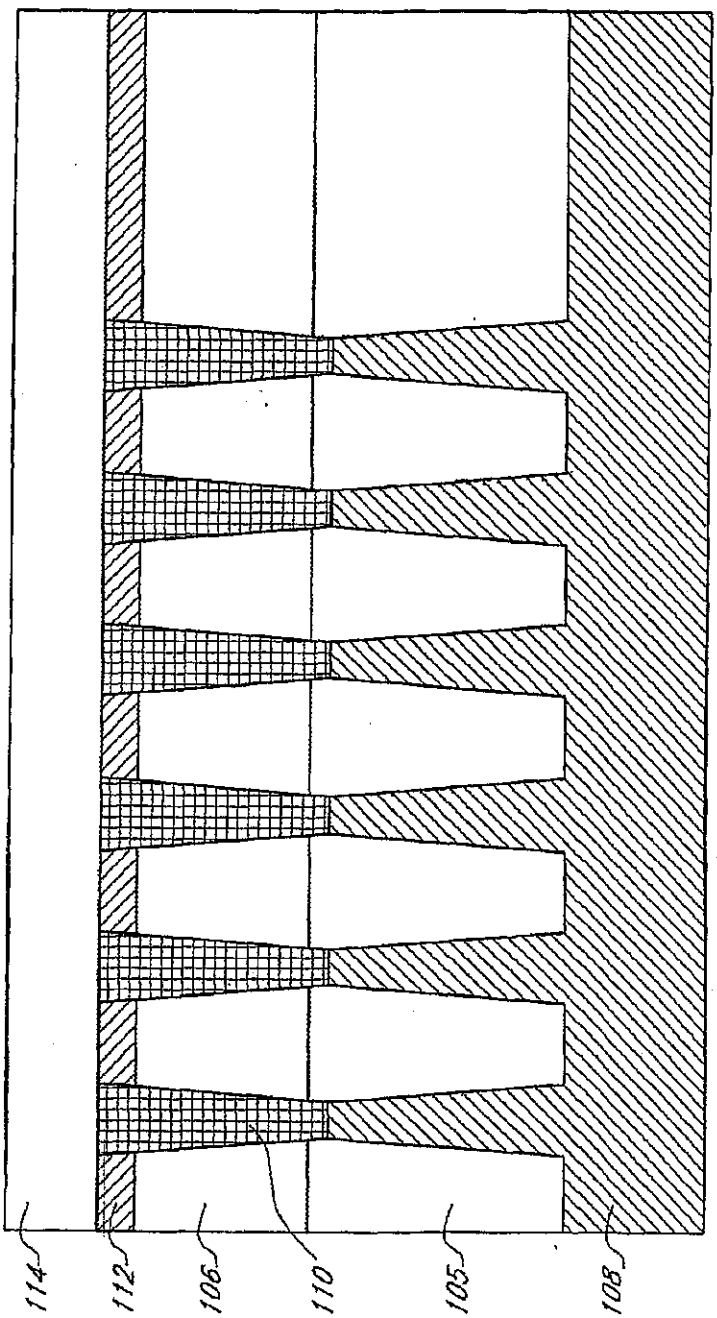


FIG. 4

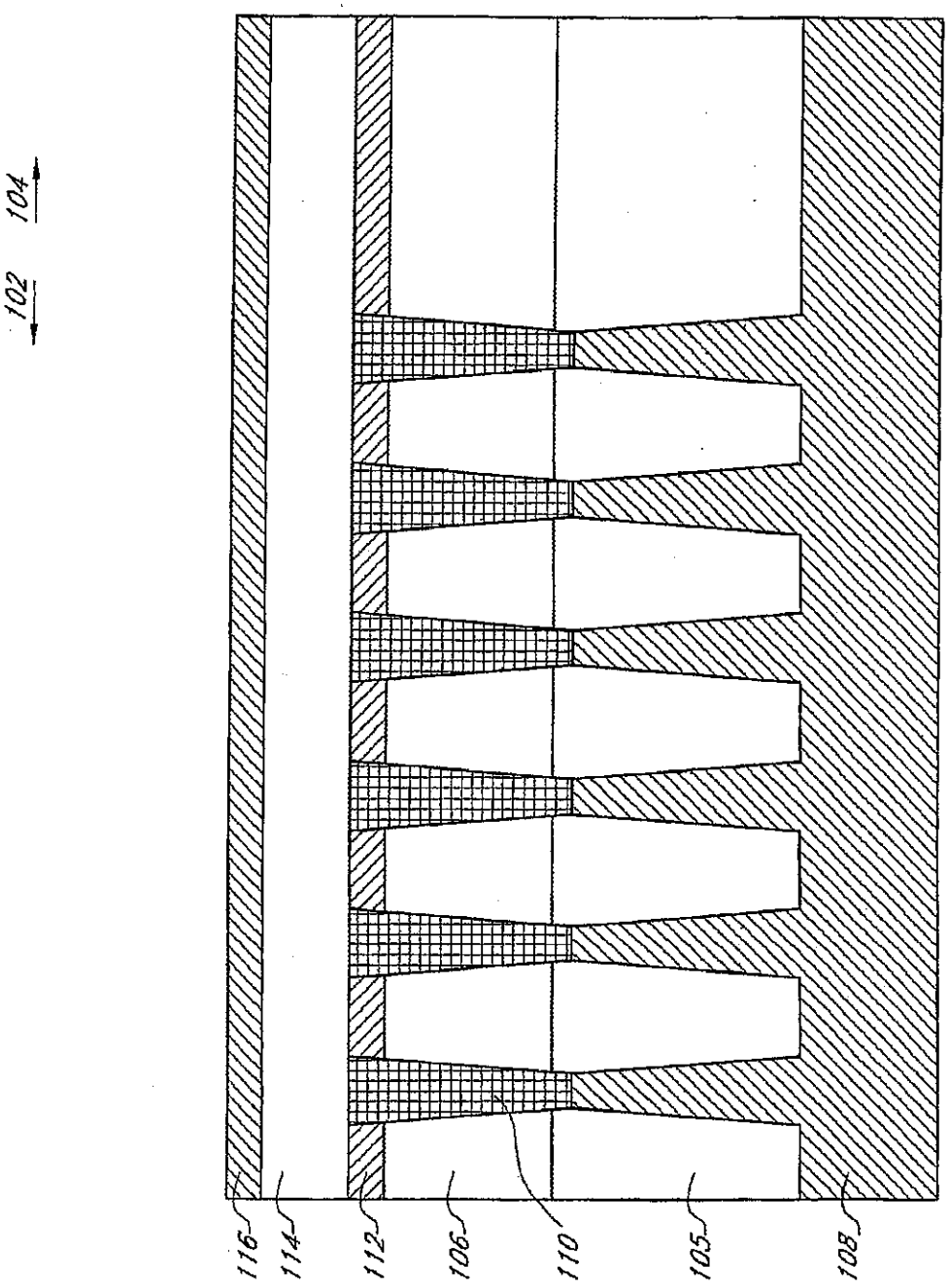


FIG. 5

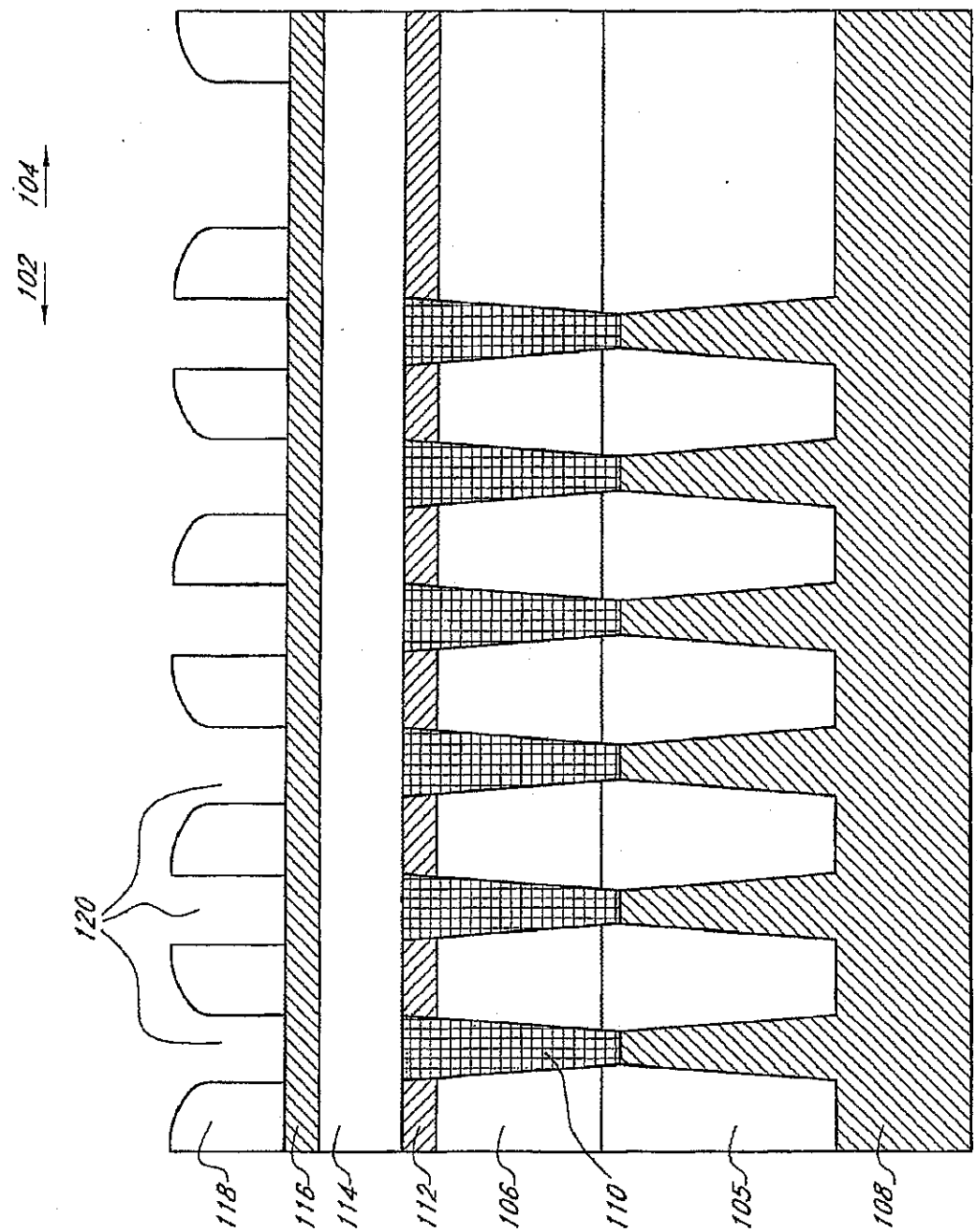


FIG. 6A

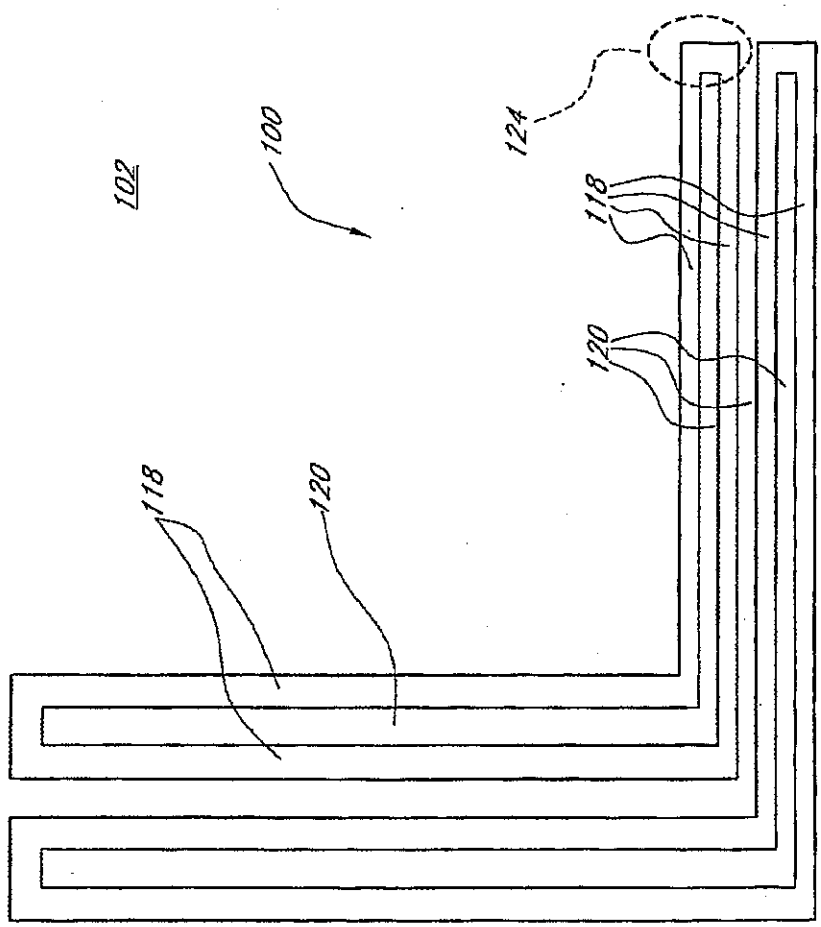


FIG. 6B

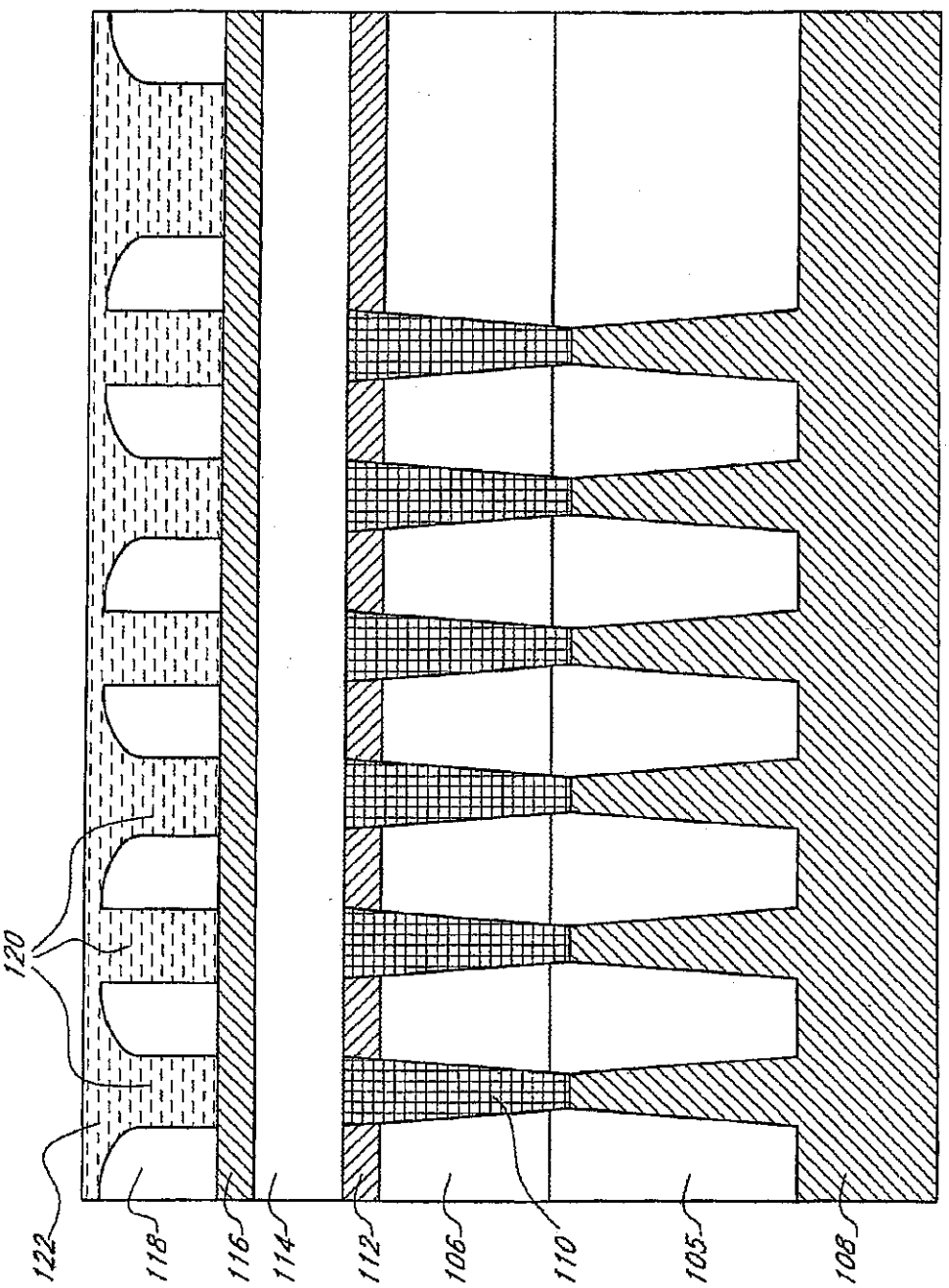


FIG. 7

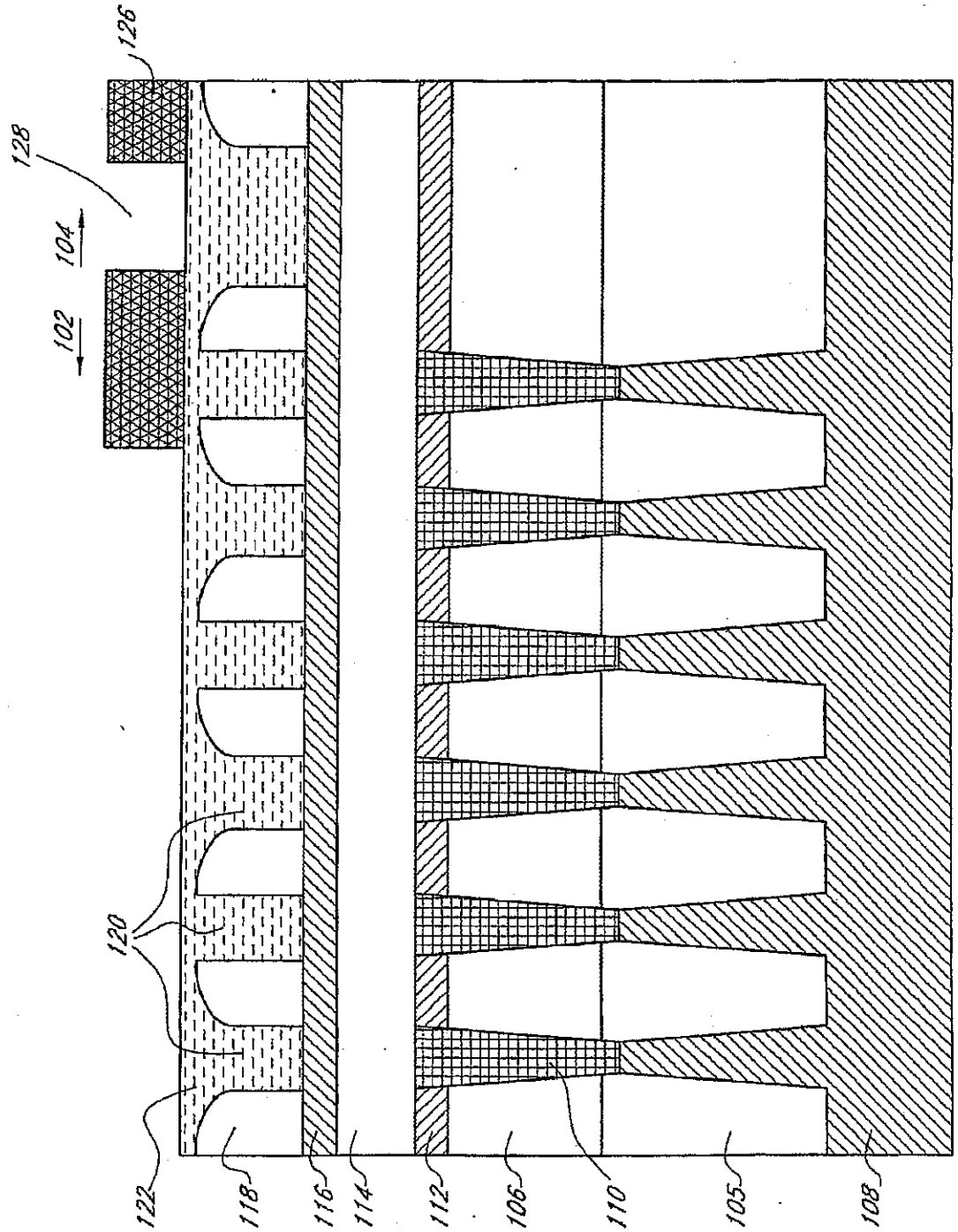


FIG. 8A

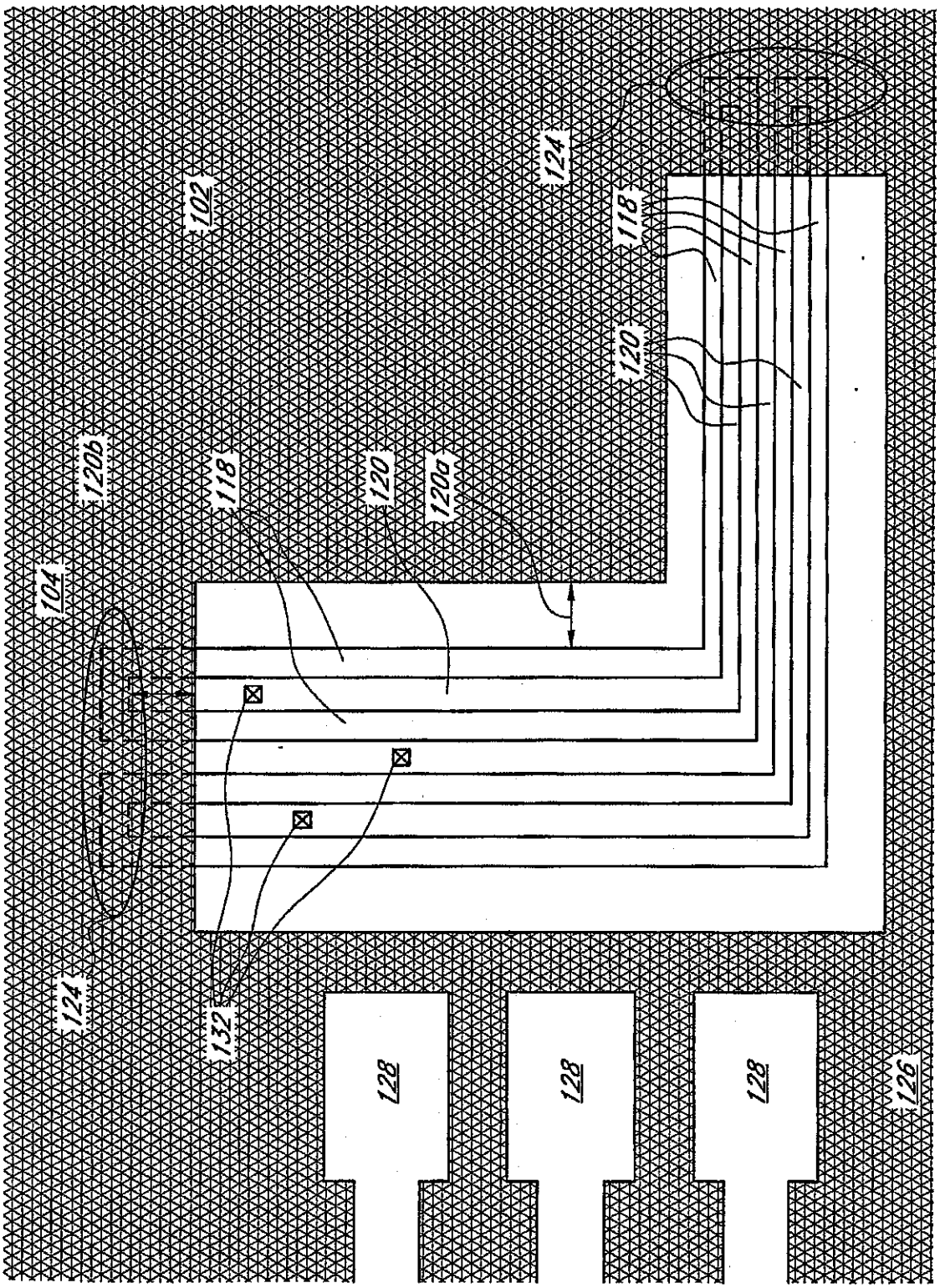


FIG. 8B

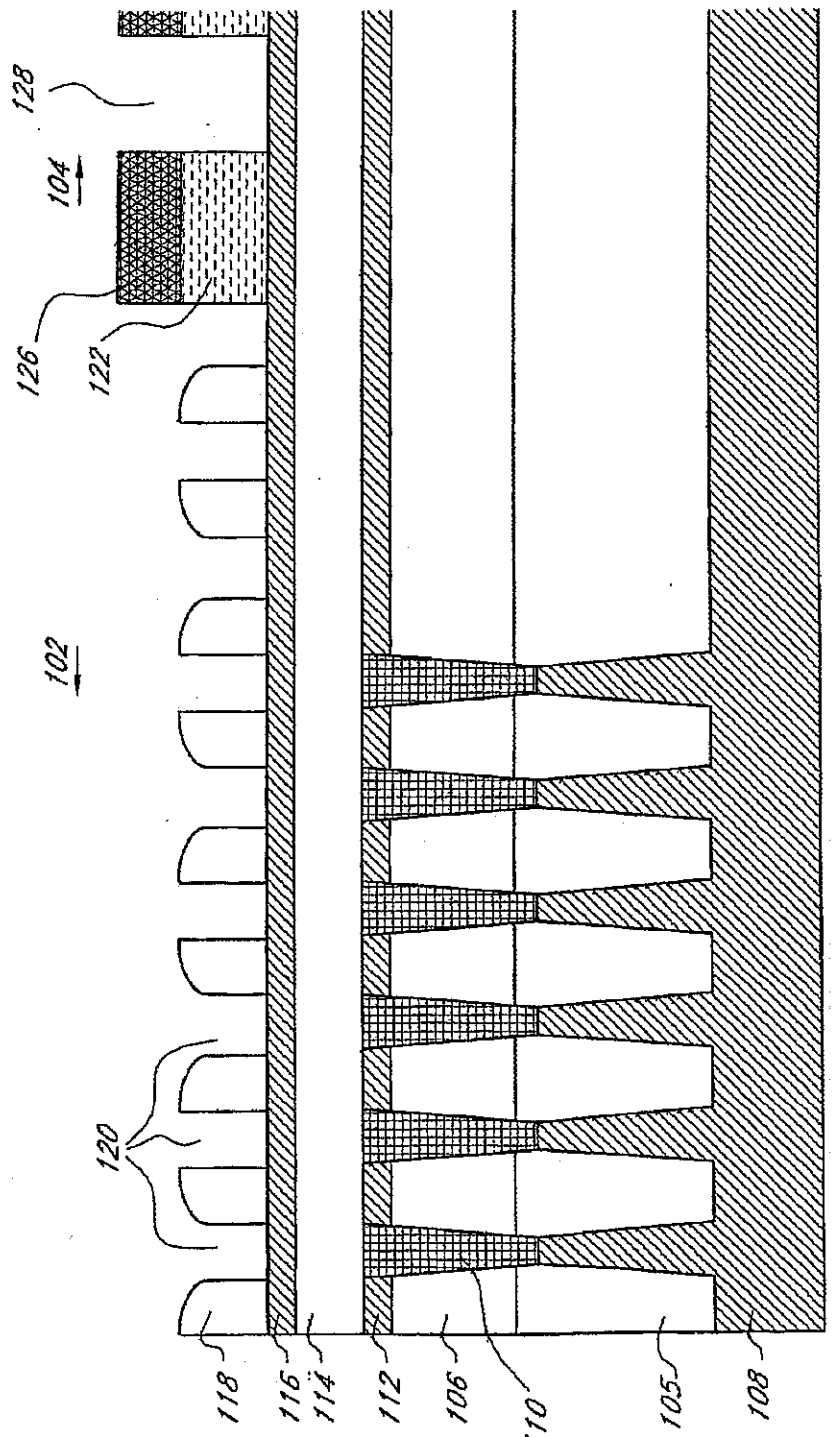


FIG. 9

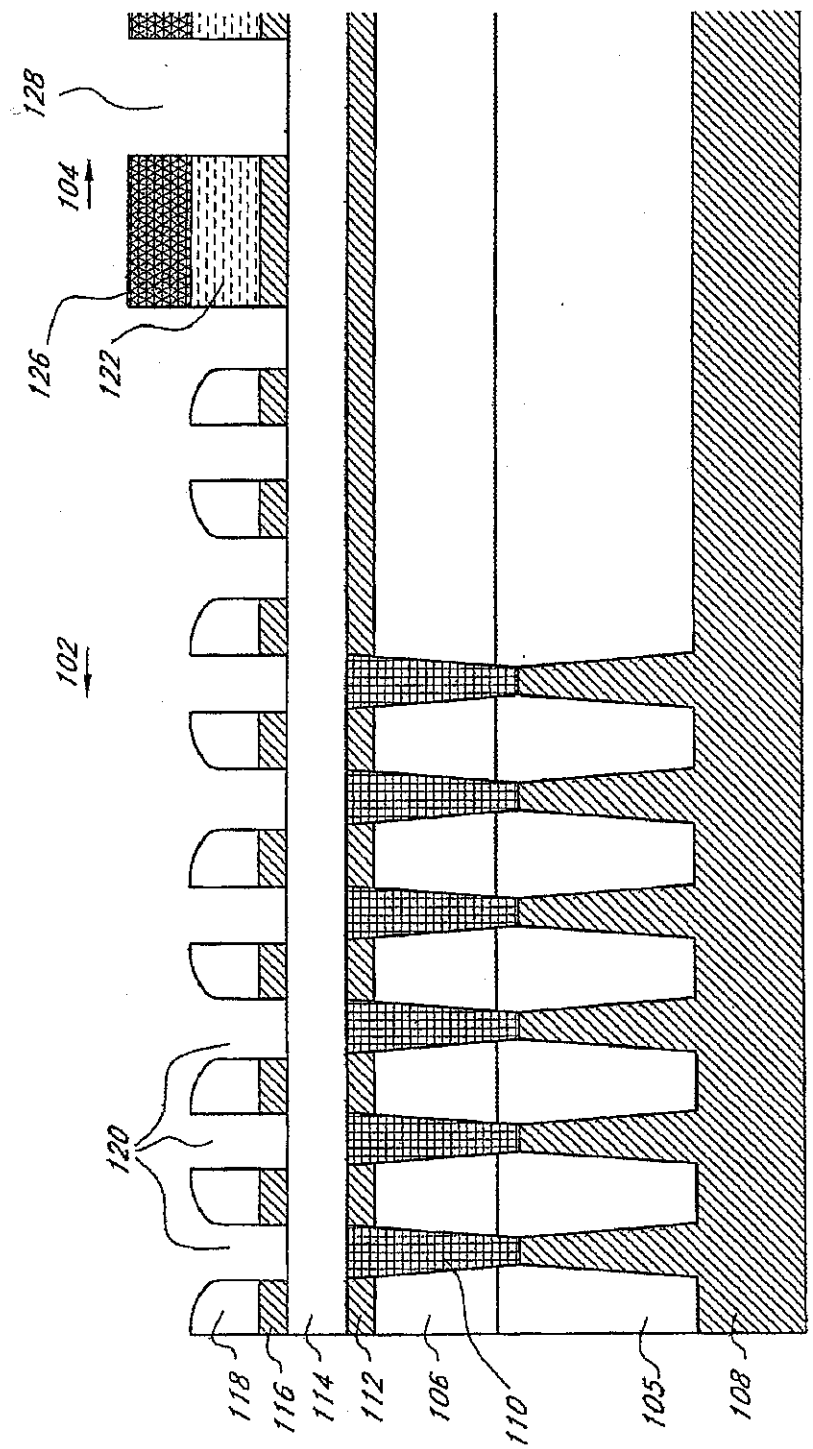


FIG. 10A

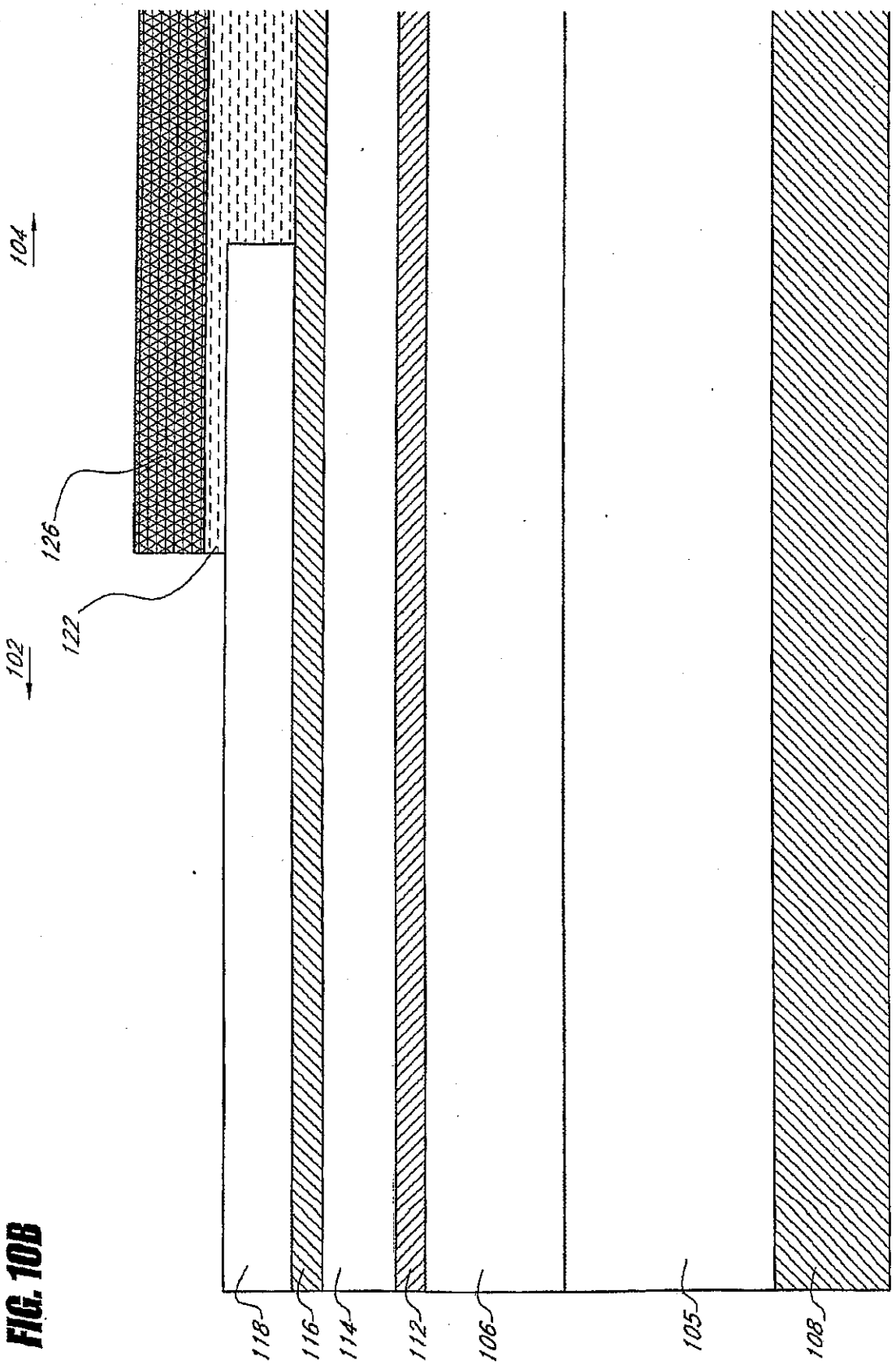


FIG. 10B

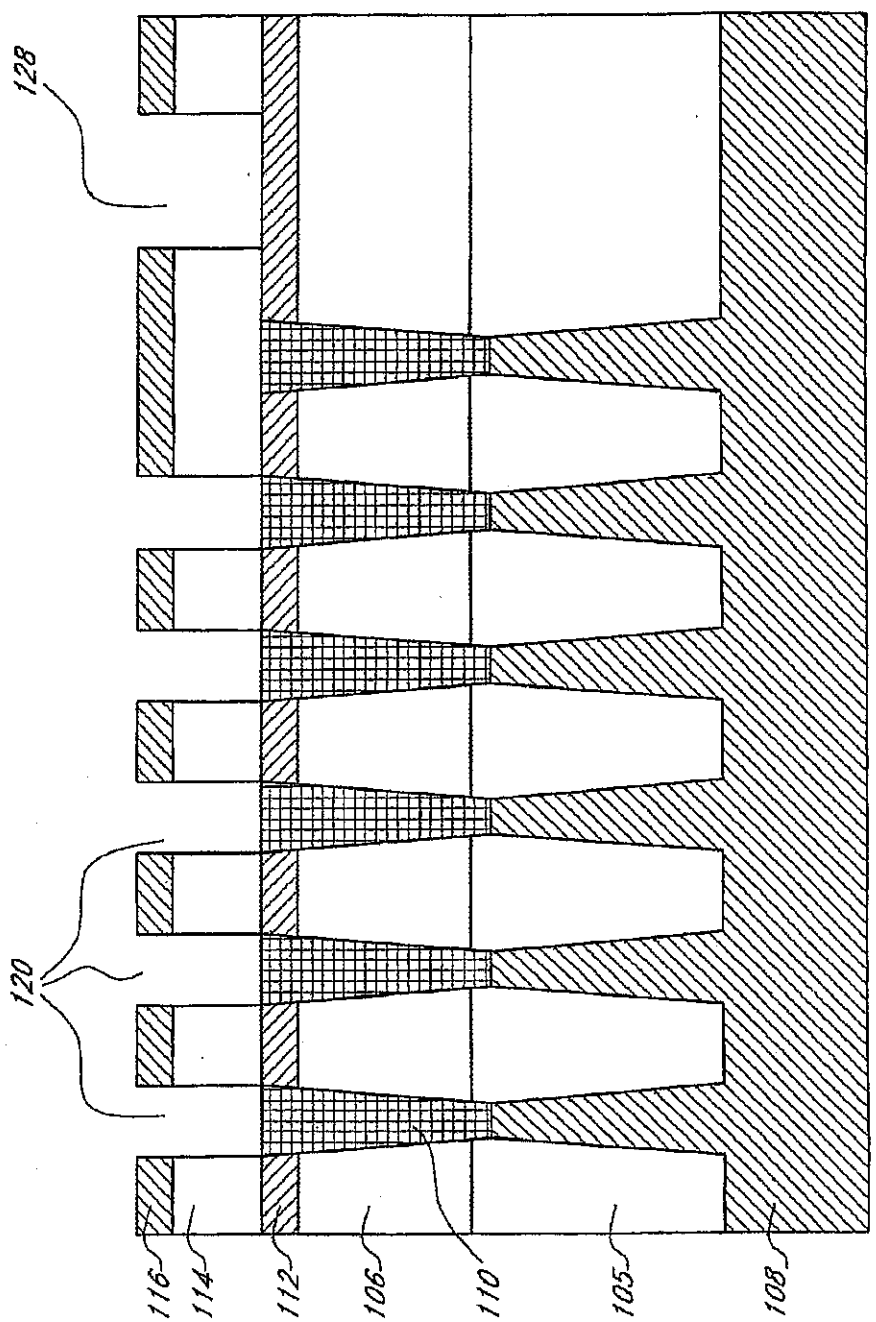


FIG. 11

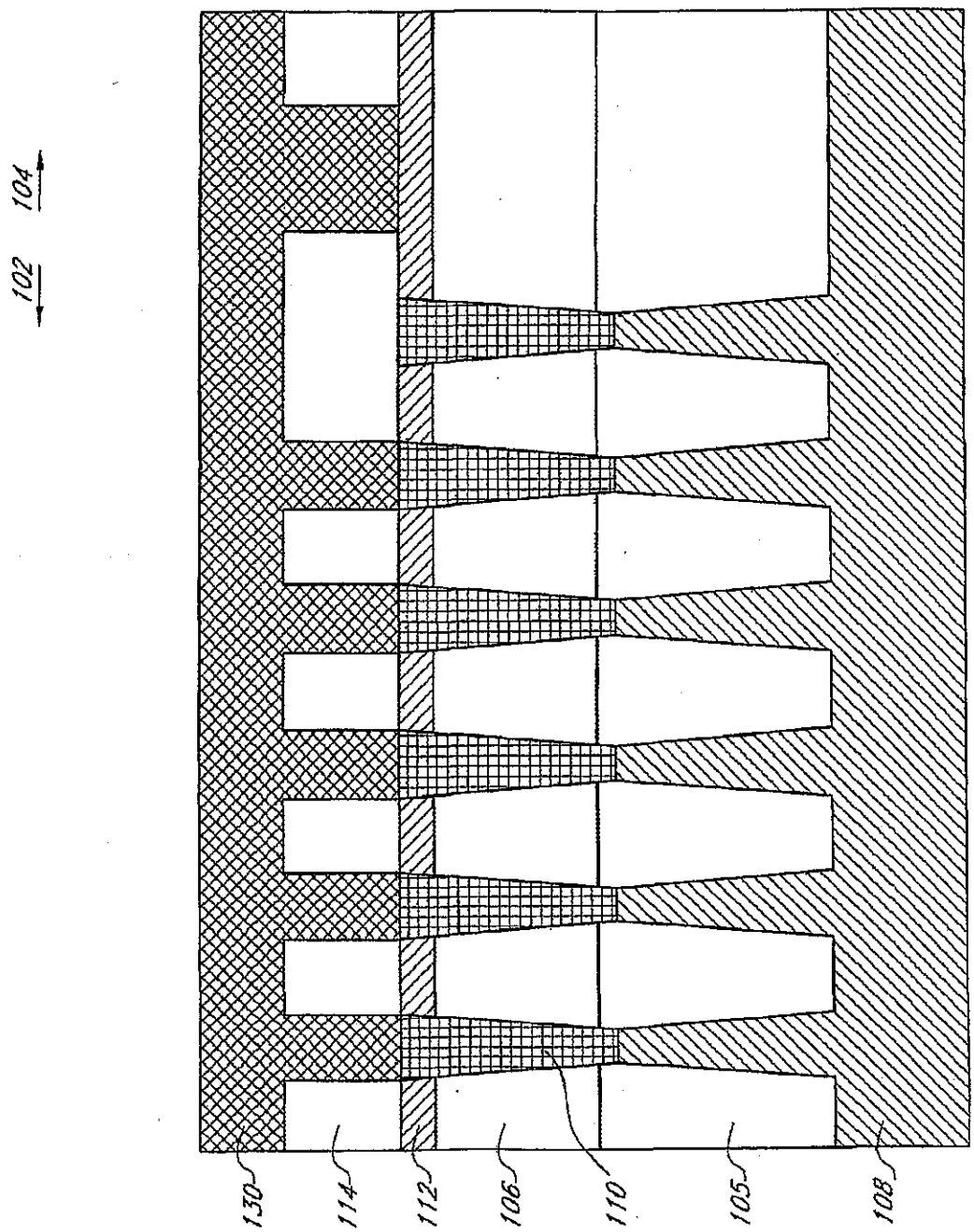


FIG. 12

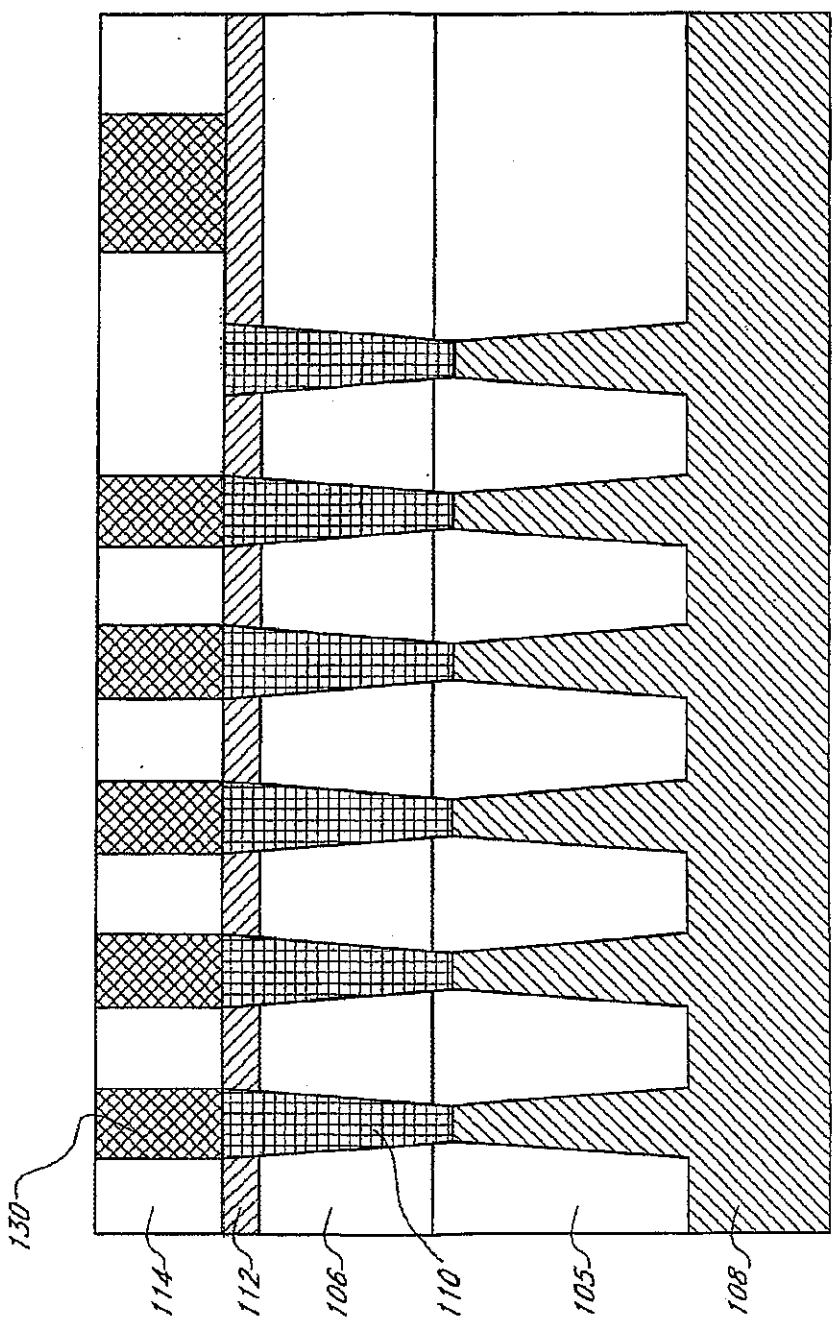


FIG. 13

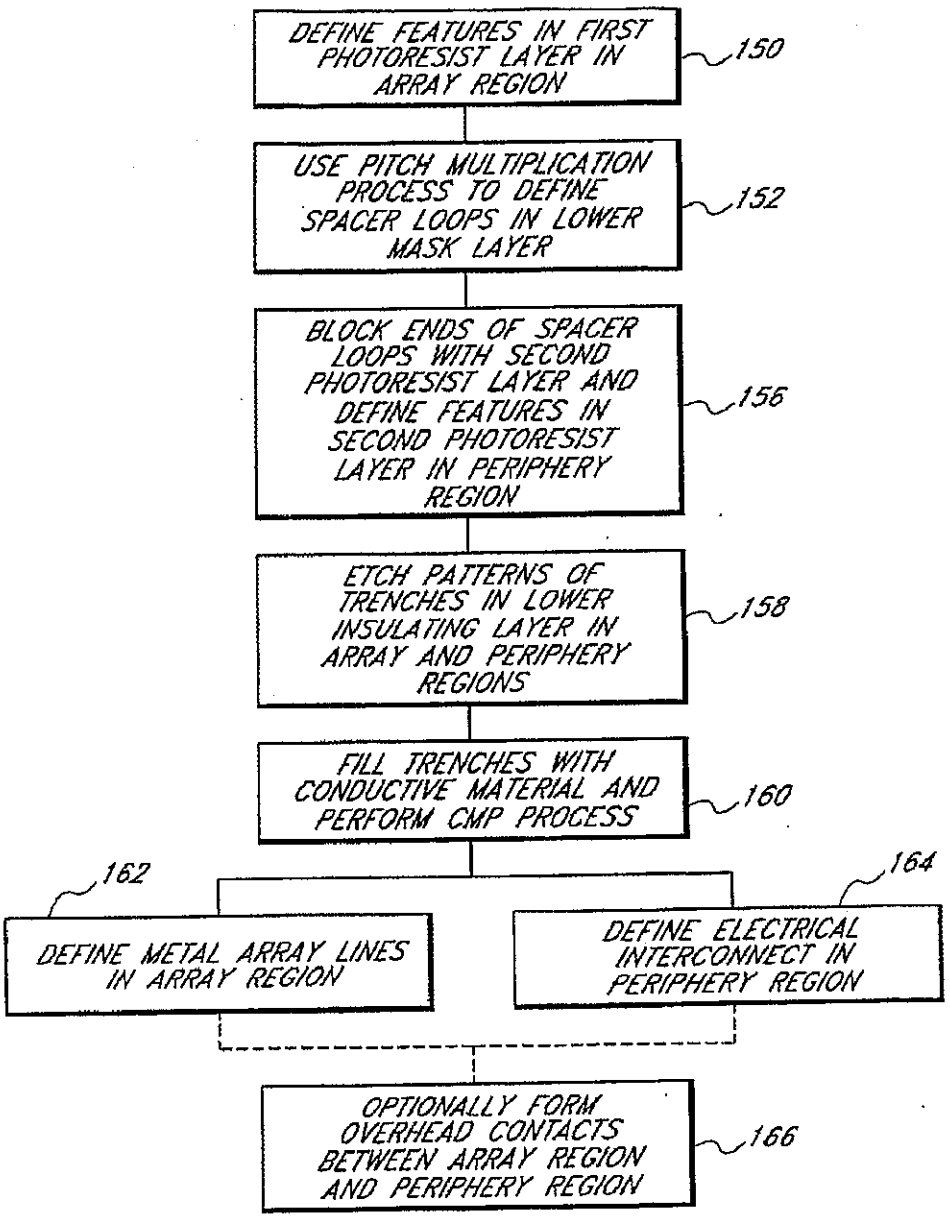

DEFINE FEATURES IN FIRST PHOTORESIST LAYER IN ARRAY REGION
150
USE PITCH MULTIPLICATION PROCESS TO DEFINE SPACER LOOPS IN LOWER MASK LAYER
152
BLOCK ENDS OF SPACER LOOPS WITH SECOND PHOTORESIST LAYER AND DEFINE FEATURES IN SECOND PHOTORESIST LAYER IN PERIPHERY REGION
156
ETCH PATTERNS OF TRENCHES IN LOWER INSULATING LAYER IN ARRAY AND PERIPHERY REGIONS
158
FILL TRENCHES WITH CONDUCTIVE MATERIAL AND PERFORM CMP PROCESS
160
162
DEFINE METAL ARRAY LINES IN ARRAY REGION
164
DEFINE ELECTRICAL INTERCONNECT IN PERIPHERY REGION
OPTIONALLY FORM OVERHEAD CONTACTS BETWEEN ARRAY REGION AND PERIPHERY REGION
166

FIG. 14

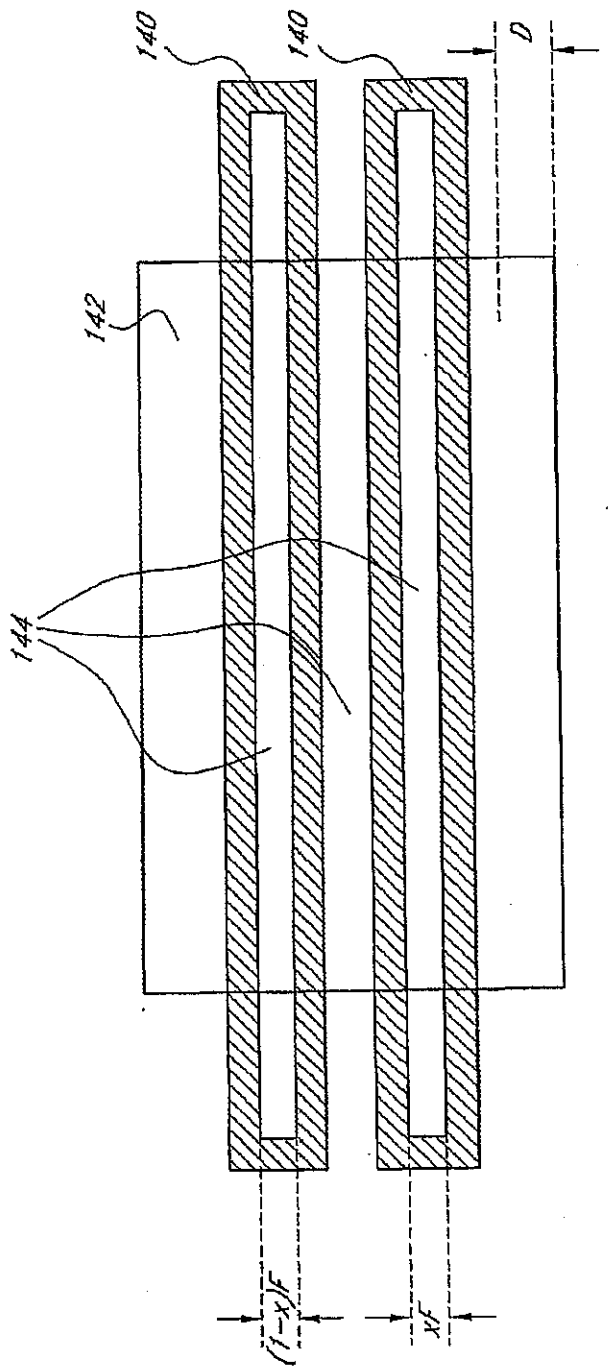


FIG. 15

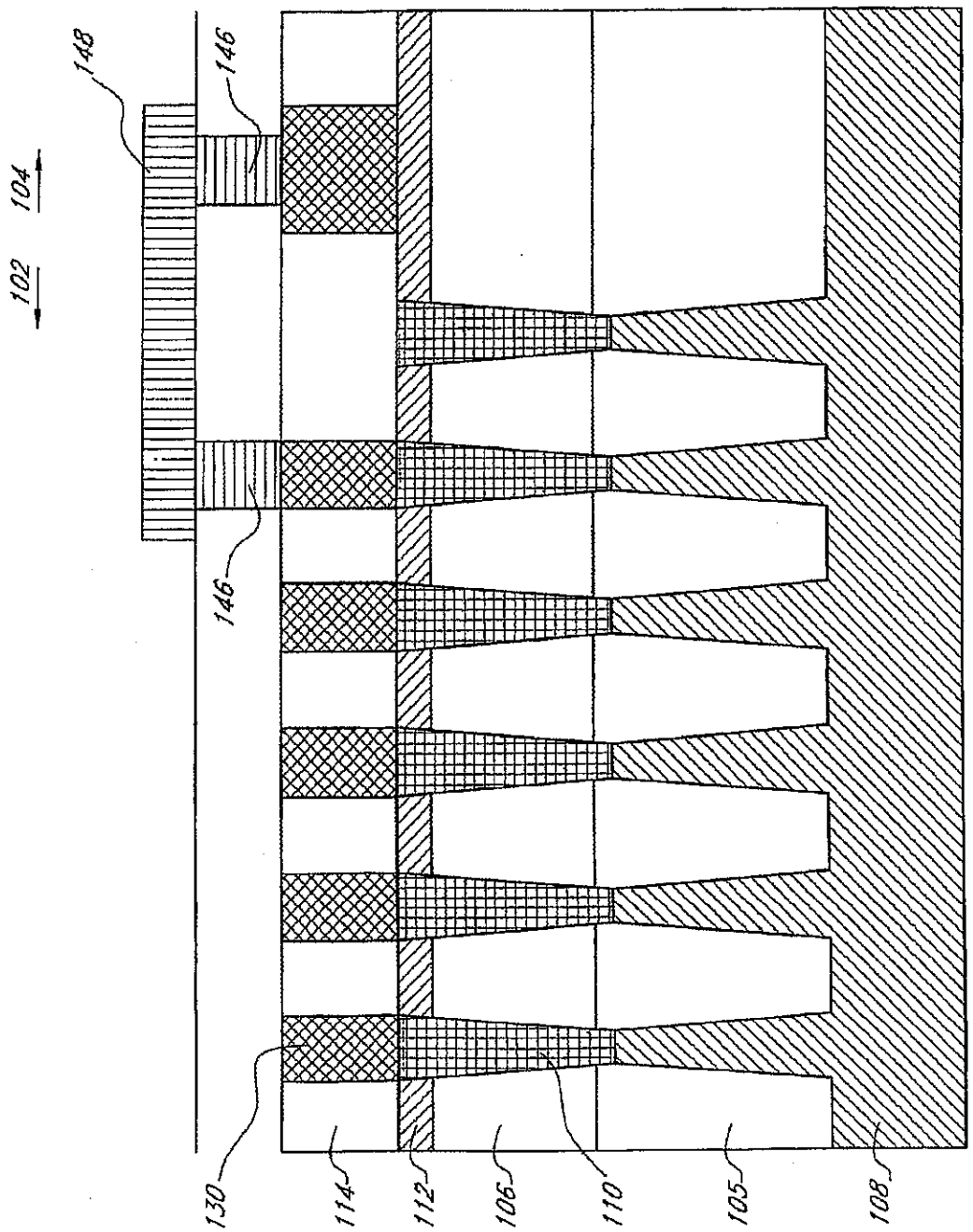


FIG. 16

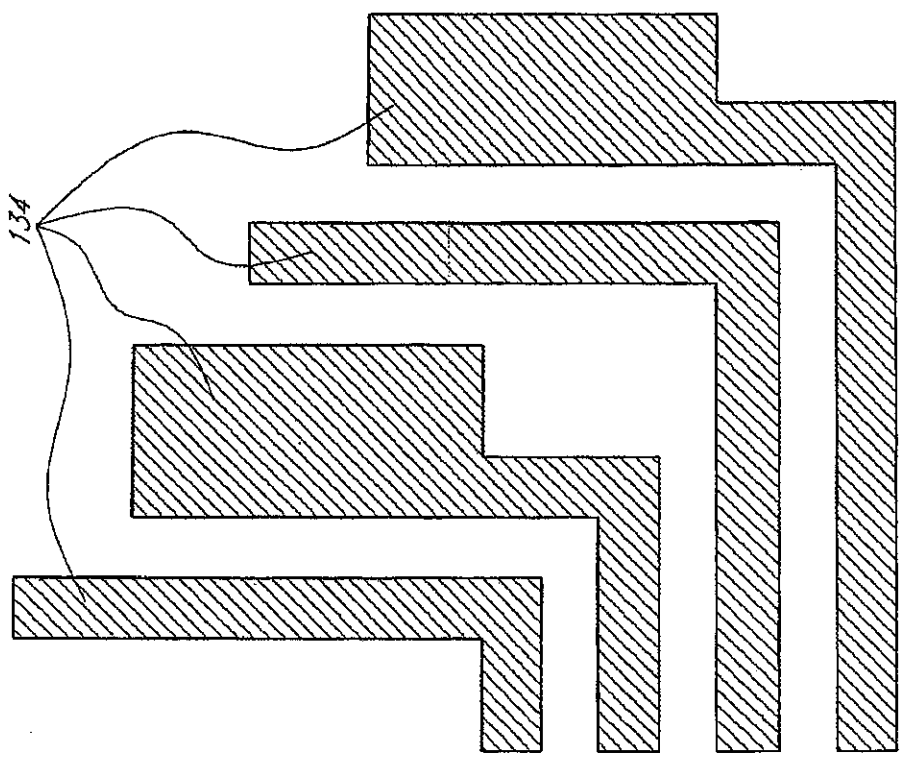


FIG. 17A

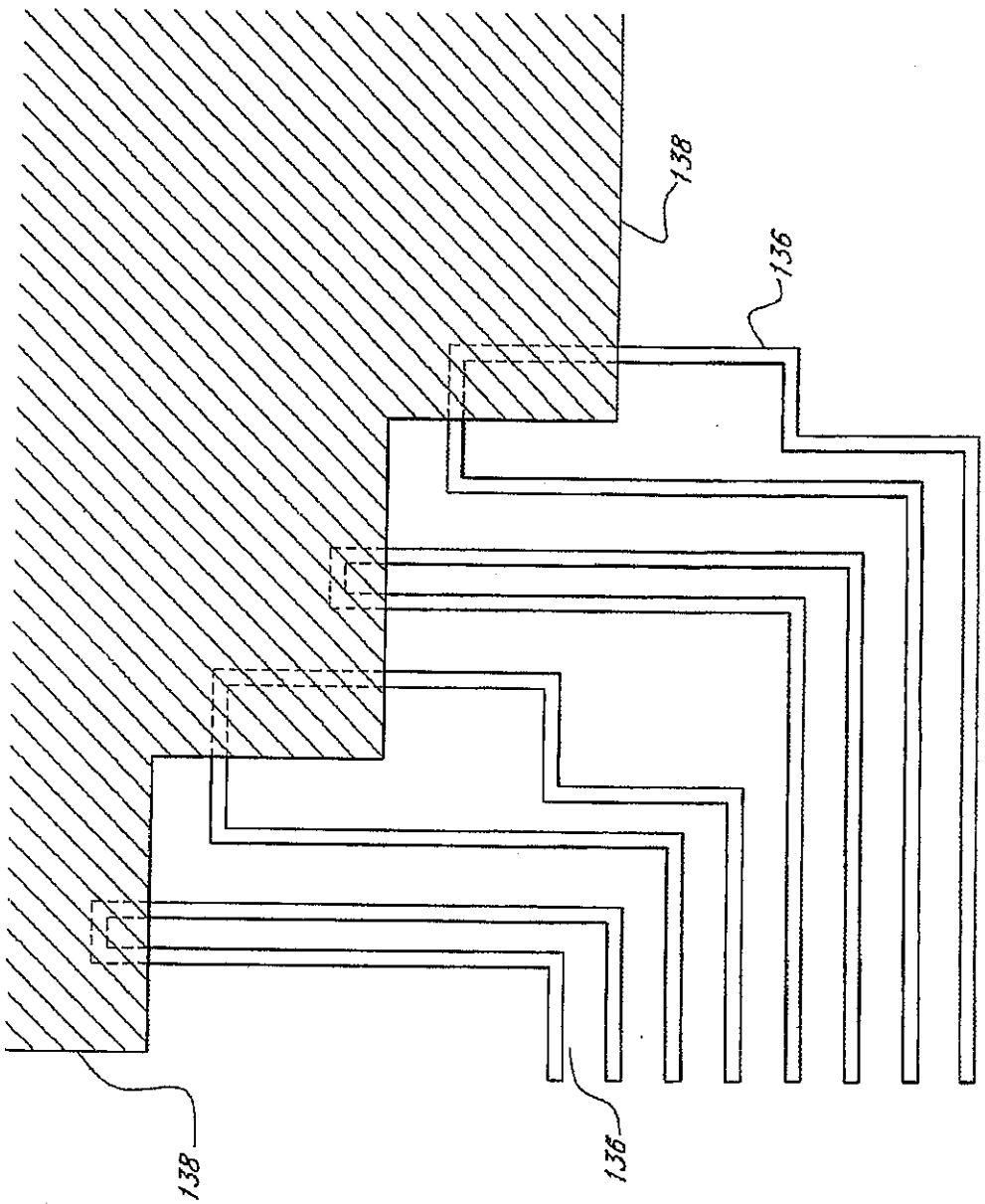


FIG. 17B

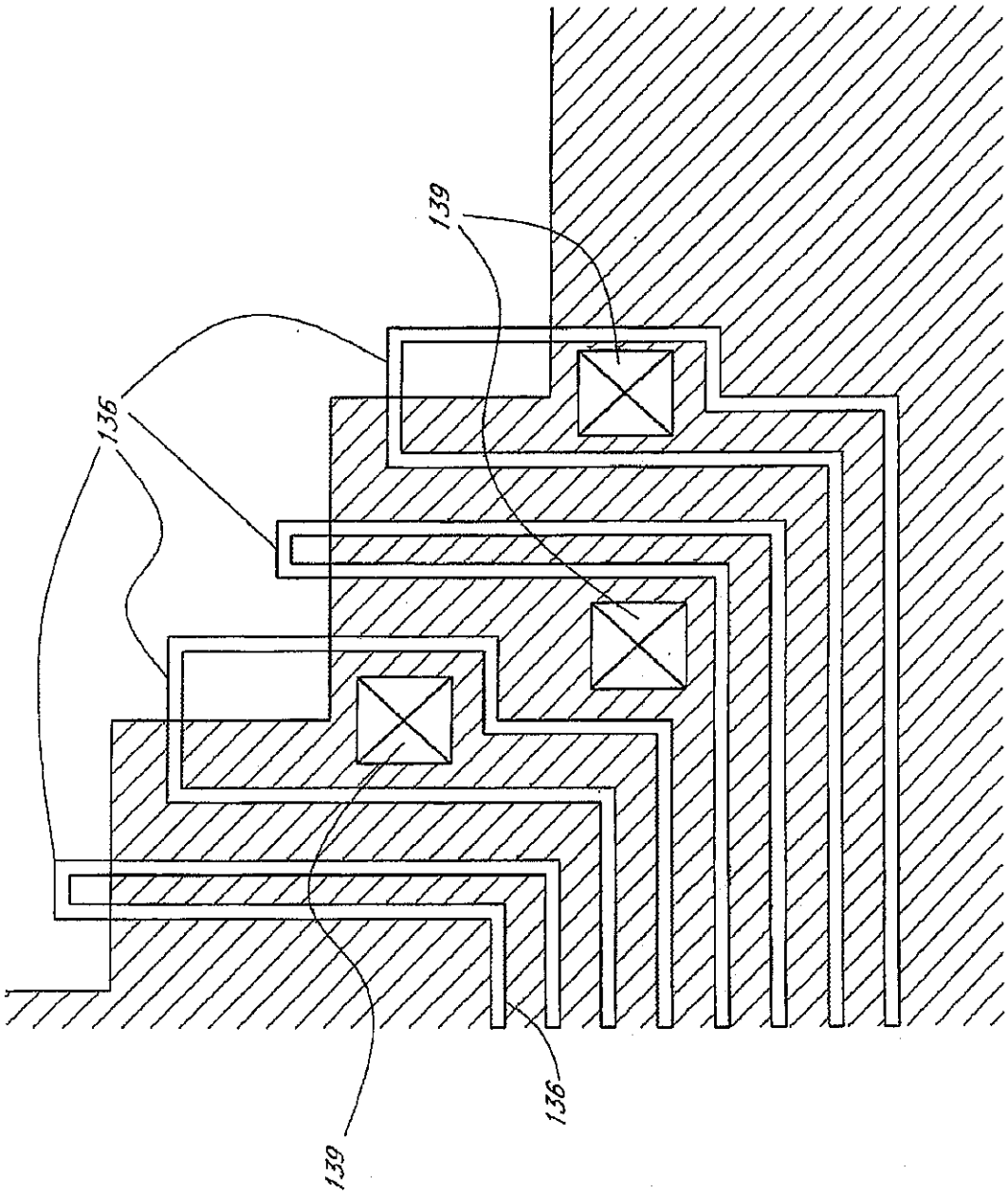


FIG. 17C