

RESERVE COPY

PATENT SPECIFICATION

DRAWINGS ATTACHED

Inventor: LARNED AMES MEACHAM

1150.546



1150.546

Date of Application and filing Complete Specification: 26 May, 1966.

No. 23534/66.

Application made in United States of America (No. 463601) on 14 June, 1965.

Complete Specification Published: 30 April, 1969.

© Crown Copyright 1969.

Index at acceptance: —H3 T(1A1, 1N1, 2J, 2T3J, 2T4, 3P, 4C, 4D, 4E2N, 4F, 4M); H4 R19

Int. Cl.: —H 03 f 3/04

COMPLETE SPECIFICATION

Negative Impedance Converters

5 We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195, Broadway, New York City, New York State, United States of America, a Corporation organized and existing according to the laws of the State of New York, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

10 This invention pertains to negative impedance devices using active elements.

15 It has always been desirable to obtain a simple and effective negative impedance device for use where substantially distortionless and lossless operation is desired. One such use is in two-wire or bi-directional telephone transmission lines. If the conductor resistance could be neutralized, the need for heavy gauge wire, equalizers and loading coils would be obviated since conduct-resistance is a prime source of transmission loss and frequency distortion.

20 In the past, various attempts have been made, with limited success, to meet these needs. Arrangements employing thermistors having negative temperature characteristics have been employed and found wanting due to inherent slowness of response to signal frequencies and inability to duplicate desired responses. Transformer-coupled vacuum tube circuits for obtaining negative impedances have had the disadvantages of large bulk, inefficient use of operating power and unsatisfactory frequency response. Other combinations have included circuits which incorporated semiconductor elements but which were found unsuitable for many applications due to limited range of operation and instability of characteristics, both in the negative impedance region and otherwise.

[Price 4s. 6d.]

According to one aspect of the present invention a two-terminal negative impedance converter comprises two transistor devices of opposite conductivity type each having a collector, an emitter and a base, having the base of each connected to the collector of the other and each of the emitters being connected to a respective one of the two terminals, means for biasing each of the transistor devices comprising an impedance connected between respective base and emitter electrodes of each transistor device, and a control impedance connected between the two bases, the arrangement being such that on the application of a suitable current source across the two terminals, the transistor devices are each biased in a linear region of operation, and the impedance produced between the emitters is proportional to the negative of the control impedance.

According to another aspect of the invention a two-terminal negative converter comprises a semiconductive device having four successive zones of alternately opposite conductivity type capable of exhibiting current amplification, the two terminals being connected respectively to the outer zones, respective biasing means including an impedance connected between each outer zone and the next adjacent zone, and a control impedance connected between the two inner zones, the arrangement being such that the application of a suitable current source across the two terminals results in a negative impedance across the two terminals the value of which is proportional to the negative of the control impedance.

This arrangement may be considered as being formed of two three-zone devices having certain zones in common. A bias circuit comprising an impedance is provided to effect a regenerative augmentation of current flow

Price 5s. 0d. Price 25p

through the devices when a threshold value is exceeded. The function of the control impedance may be thought of as a means for diverting current that would otherwise flow from the main current path of one device to the gating path of the other device. This "diverted current" is now made to flow from the main current path of one to and through the main current path of the other transistor so that the regenerative tendency of the circuit, once the threshold value of input current has been exceeded, is moderated and controlled. Therefore, assuming that the current is supplied from a source with positive resistance of greater absolute value than the negative resistance of the circuit, the net effect is to permit the circuit to operate stably in the current range associated with the regenerative increase in current. Within this current range the voltage-current characteristic has a definitely determined negative slope.

In one specific embodiment to be described, an NPN and a PNP transistor are connected with the base or control electrode of each coupled to the collector or main current path of the other. The configuration is biased so that once a threshold value of input current is reached, collected current from one transistor produces forward-bias in the base circuit of the other transistor causing an increase in the collector current of the second transistor which in turn produces forward-bias in the base circuit of the first transistor to further increase in a regenerative manner the first transistor's collector current. Additionally, there is an impedance connected between the base electrodes of the respective transistors to provide a path for diverting nearly all the current that would otherwise flow from the collector circuit of one through the base biasing circuit of the other. This current is now diverted so that it flows from the collector circuit of one, backward through the diverting impedance, and thence through the collector circuit of the other to stabilize and control the regenerative current increase. For currents of operating value applied from a sufficiently resistive source each transistor is thus stably biased within its linear range of operation. The increasing backward current through the diverting impedance is effectively deducted from the value of forward current therethrough at threshold so that any further increase in input current manifests itself in a corresponding decrease in total current flowing through the diverting impedance. Since the input voltage in this region of current can be approximated by the voltage across the diverting impedance, the input impedance of the device is negative and essentially proportional to the positive impedance connected between the base electrodes.

The invention will now be described with

reference to the following embodiments and the accompanying drawings in which:

Fig. 1 is a circuit diagram representing one illustrative embodiment of the invention;

Fig. 2 is a graph representing a typical characteristic of a circuit embodiment;

Figs. 3, 4, 5 and 6 depict other embodiments of the invention; and

Fig. 7 is an illustrative application of the embodiments.

Referring now to the drawings, the circuit illustrated in Fig. 1 comprises a PNP transistor Q1 and an NPN transistor Q2 connected with the base of each coupled to the collector of the other and with the emitter of each connected, respectively, to terminals 1 and 2. Resistor R1 connected between emitter and base of transistor Q1, resistor R3 connected between the respective bases of transistors Q1 and Q2 and resistor R2 connected between the base and emitter of transistor Q2 collectively form the biasing circuit for the configuration.

By applying a current source I to terminals 1 and 2 and measuring the voltage thereacross, the circuit may be shown to have a characteristic curve represented by the graph shown in Fig. 2. As the current is increased from zero, represented by point *a* in Fig. 2, transistors Q1 and Q2 remain nonconducting until the current reaches the threshold value near point *b*. Consequently, the slope of the curve between points *a* and *b* is substantially determined by the sum of the resistance values of resistor R1, R2 and R3. In this range of operation, substantially all of the current I (except for leakage currents) flows from terminal 1 to terminal 2 through resistors R1, R2 and R3, respectively. Once the value of current exceeds that corresponding to point *b* the voltage across each of the resistors R1 and R2 is sufficient to forward-bias the emitter-base junctions of transistors Q1 and Q2 to cause the flow of collector current in each transistor. In the absence of resistor R3, and in the presence of conventional biasing circuitry, all of the collector current from transistor Q1 would be constrained to flow through resistor R2 in parallel with the base-emitter junction of transistor Q2 to increase the forward-bias of transistor Q2. This would result in increased collector current of transistor Q2 which collector current would cause a corresponding increase in the forward-bias of transistor Q1 since this current is similarly constrained to flow in resistor R1 in parallel with the base-emitter junction of transistor Q1. Therefore, an increase in forward-bias beyond the threshold value would (combined with a corresponding decrease in terminal voltage V unless the current source has zero impedance) manifest itself in a regenerative increase in collector current until both transistors would be driven into saturation. The transistors, somehow biased to threshold

in the
stabil
or b
one
very
cribe
TI
path
curre
10 curre
in pa
sistor
Q1 is
resist
15 emitt
there
bias
regene
transi
20 R3 p
curre
which
R2 to
emitt
25 effect
contro
mittin
stably
source
30 tive
teristic
The
charac
b and
35 biasing
regene
more
that t
sum o
40 R1, R
increas
b, the
remain
cise
45 deter
forward
sensitiv
increas
a few
50 constan
R2, the
equal
creased
shown,
55 creases
sistor C
current
Any
itself in
60 to the
with
The
b and
tive
65 number

in the absence of resistor R3, would operate stably only when either both were cut off or both were saturated and a transition from one stable state to the other would occur very rapidly by the regenerative process described.

The insertion of resistor R3 provides a path through which current from the main current path of transistor Q1 (emitter-collector current) is diverted away from resistor R2 in parallel with the emitter junction of transistor Q2. Collector current from transistor Q1 is now permitted to flow backward through resistor R3 and thence through the collector-emitter junction of transistor Q2 so that there is no significant increase in the forward-bias of transistor Q2 with the consequent regenerative increase in the forward-bias of transistor Q1. In a similar fashion, resistor R3 provides a diversionary path for collector current flowing in transistor Q2 more of which would otherwise flow through resistor R2 to increase the forward-bias of the base-emitter junction of transistor Q1. The net effect of the insertion of resistor R3 is to control the regenerative effect described, permitting the circuit arrangement to operate stably in conjunction with a suitable current source (of finite resistance) within the negative sloping region of its volt-ampere characteristic associated with the regenerative action.

The stable negative sloping volt-ampere characteristic (shown in Fig. 2 between points *b* and *c*) resulting from the controlled forward-biasing of each of the transistors in the regenerative region may now be explained in more detail. At the outset, it is to be noted that the terminal voltage *V* consists of the sum of the voltage drops across the resistors R1, R2 and R3. As the applied current *I* increases beyond the threshold value of point *b*, the voltages across resistors R1 and R2 remain substantially constant (or more precisely increase only slightly) since each is determined by the voltage of its associated forward-biased base-emitter junction which sensitively controls collector current between threshold and saturation without rising above a few tenths of a volt. As a result of this constancy of voltage across resistors R1 and R2, the terminal voltage *V* is approximately equal to the voltage across resistor R3 increased by a small fixed value. As will be shown, the voltage across resistor R3 decreases with increasing current *I* until transistor Q1 and Q2 saturate at the value of current corresponding to point *c* of Fig. 2. Any further increase in current *I* reflects itself in a small increase in voltage *V* due to the slight increase in saturation voltage with increasing current.

The portion of the curve between points *b* and *c* is substantially linear with a negative slope being equal to kR_3 where k is a number smaller than 1. The relatively insignificant

deviation from linearity and the restriction of proportionality constant k to values less than unity result from the small increase in voltage across resistors R1 and R2 with increasing current *I* and deviation from unity of the current amplification factor α for each transistor. Finally, as stated above, the slope of the characteristic curve for current greater than that at point *c* is very small and attributable to the small increase in junction voltage in the saturation region.

It is possible to prove qualitatively the existence of the negative slope in the characteristic curve between points *b* and *c* by considering the effect of the various currents defined in Fig. 1. Assume the circuit is biased to operate at point *b* of the characteristic curve by means of an applied current *I* and that this current is then increased by an amount ΔI . This increase of current must reflect itself in a corresponding increase in the emitter currents I_{e1} and I_{e2} of the transistors Q1 and Q2 respectively since the emitter-base junction voltage of transistors Q1 and Q2 does not rise significantly beyond the forward-bias values. Therefore, since the voltage across resistors R1 and R2 is so constrained, current I_{R1} and I_{R2} through resistors R1 and R2 respectively remain substantially the same. Assuming the respective current amplification factor α of each transistor is equal to 1, the collector current of each transistors will be equal to the respective emitter current. Consequently, due to the increase in current *I* by an amount ΔI , each of the collector currents I_{c1} and I_{c2} of transistors Q1 and Q2 respectively, increases by an amount equal to ΔI . Furthermore, since the sum of currents I_{c1} , I_{R3} and I_{c2} must at all times be equal to the current supplied through terminals 1 and 2, it follows that current I_{R3} must decrease by an amount ΔI when the impressed current *I* increases by ΔI . Therefore, as the current *I* increases between points *b* and *c*, the current I_{R3} decreases correspondingly as does the voltage across resistor R3.

Figs. 3A and 3B serve to illustrate the fact that the electrical connection between transistors Q1 and Q2 produces an analogue for a PNP device and therefore that a circuit embodiment of the invention shown in Fig. 3A using a PNP device is possible. Furthermore, as with each of the embodiments disclosed if a generalized impedance Z_3 is used in place of resistor R3 shown in Fig. 1, the terminal impedance Z_n will be equal to $-kZ_3$. In other words, if Z_3 is a generalized impedance having a positive real and a positive imaginary part, the terminal impedance will correspondingly have a negative real and a negative imaginary part. Fig. 3B pictorially illustrates the fact that the PNP device can electrically be split into a PNP portion and an NPN portion with appropriate elec-

trical interconnections between the split portions to provide a two-transistor analogue for the PNP device.

Fig. 4 illustrates another embodiment of the invention wherein the "control" or "diverting" impedance between the base electrodes of transistors Q1 and Q2 is in the form of a parallel RC circuit and wherein resistors are included in the emitter circuit of each transistor to provide negative feedback. By including capacitor C3 in parallel with resistor R3, the circuit becomes more suitably designed for inclusion in transmission lines as a negative impedance loading circuit. The effects of distributed reactance in transmission lines combined with reflections between adjacent loading circuits tend to produce instability unless care is taken that at some frequency the negative impedance of each circuit does not become unstably related to the impedance of the line in which it is inserted. This condition results in some form of self-oscillation even when the line is energized from a regulated direct-current source. Capacitor C3 manifests itself at terminals 1-2 as a negative capacitance in parallel with the negative resistance and thus acts to prevent the condition of instability of introducing effective inductance and by gradually eliminating the negative resistance as frequency increases. The gross effect of the capacitor therefore is to alter the impedance relationships (Nyquist plot) in a manner which ensures stability of operation.

As noted above, the portion of the characteristic curve of Fig. 2 between points *b* and *c* deviates from linearity because of the increase with rising collector current of the current amplification factor α , and because of the small, but nonlinear increase in voltage across resistors R1 and R2, as the circuit current *I* increases in value. This portion of the curve has a slight concave downward slope thereby producing harmonic frequency distortions which may be undesirable for some applications. The effect of the feedback resistors R₁ and R₂ included in the emitter circuits of transistors Q1 and Q2, respectively, to stabilize the base to collector transconductance substantially increases the linearity and therefore decreases the distortion introduced. Furthermore, the use of feedback reduces the proportionality constant *k* so that a larger value of resistor R3 must be used to obtain a given negative resistance. The net effect of such an adjustment is to alter the characteristic curve shown in Fig. 2 so that the portion between *a* and *b* has an increased slope thereby reducing the minimum usable current of the operating range between points *b* and *c*. In effect, the current range between *b* and *c* is pushed closer to the voltage axis by compressing the current range between points *a* and *b*.

The circuit shown in Fig. 5 is a modification of that shown in Fig. 1 with a two-transistor circuit of the type disclosed in patent No. 737,506 replacing each of the transistors shown in Fig. 1. The purpose of this modification is to improve the linearity of the negative resistance portion of the characteristic curve by effectively increasing towards unity and stabilizing the value of the current amplification factor α of each stage. With one exception the circuit operates in all other respects in a manner identical to that described in connection with the circuit of Fig. 1 since the two transistors of like conductivity are equivalent to a single transistor with a higher α . The exception noted is that the threshold for forward-bias across resistor R1 or R2 is essentially twice as great, since each corresponds to two-base-emitter junctions in series. As a result, points *b* and *c* in Fig. 2 are moved upward, effectively representing a larger expenditure of average operating voltage.

Another embodiment of the invention is shown in Fig. 6. This circuit substantially eliminates the nonlinearity in the negative resistance portion of the curve due to both the deviation of α from unity and the varying voltage drop across resistors R1 and R2. In this circuit a pair of transistors Q1_a and Q2_a of opposite conductivity type (NPN and PNP, respectively) acts to bypass current in excess of the value shown at point *b* in Fig. 2 around resistor R3 in a manner similar to the action of transistors Q1 and Q2 in the circuit embodiment of Fig. 1. Transistor Q1_b, interposed between transistor Q1_a and the biasing circuit resistor R1 performs as an amplifying device responsive to changes in voltage across resistor R1 to control the base current of transistor Q1_a. Since the base and emitter electrodes of transistor Q1_a are connected across resistor R1, any change in voltage across resistor R1 manifests itself in a corresponding current change in the collector of transistor Q1_a. Thus, the emitter current sensitivity of transistor Q1_a, in response to changes in voltage across resistor R1, is effectively increased by β (approximately

equal to $\frac{1}{1-\alpha}$), the transconductance of the added transistor Q1_b. The operation of transistor Q2_b is identical with that of transistor Q1_b so that their combined effect is to heighten the sensitivity of transistors Q1_a and Q2_a to voltage changes across resistors R1 and R2, respectively. The currents through resistors R1 and R2 are therefore constrained to remain substantially constant to produce a linear variation of emitter current of transistor Q1_a and Q2_a with total current *I*. For this circuit, the points *b* and *c* of Fig. 2 are not moved upward as described for the

circ
bric
A
tion
tion
the
clos
If d
pon
inse
esta
k th
nize
if n
the
ther
sisto
the
trans
mad
the t
Fi
any
tive
trate
phon
a tel
a dis
tion
pensi
pedar
is po
equal
neces
35
distor
ing c
vals
circuit
of th
40
negati
herein
the p
know
respon
the
45
p
curren
loadin
region
50
tially
freque
the ci
arrang
tive
two
impro
WH
1. A
60
verter
opposi
lector,
of each
and ca

circuit of Fig. 5, as resistors R1 and R2 each bridge only a single emitter-base junction.

Another effect of this circuit configuration is an increase in the value of the proportionality constant k toward unity to cause the negative terminal resistance to more closely approximate the value of resistor R3. If desired, emitter feedback resistances corresponding to those shown in Fig. 4 may be inserted in conductors d and e of Fig. 6 to establish a stable preferred value of constant k that is less than unity. It is to be recognized that appropriately valued resistors may, if needed, be connected between the base and the emitter of transistor Q1, to prevent thermal instability and to ensure that transistor Q1 is not operated unwantedly by the reverse-bias collector current (I_{co}) of transistor Q1. A similar statement can be made for the inclusion of a resistor between the base and the emitter of transistor Q2.

Fig. 7 illustrates one specific application of any one of the circuits shown in the respective embodiments. This figure serves to illustrate how it is possible to obtain a long telephone transmission line connected between a telephone central office 7 at one location and a distant station set 8 at a subscriber's location in a simple, stable, versatile and inexpensive manner. By using the negative impedance elements of the type described, it is possible to reduce wire size and eliminate equalizers and bulky loading coils formerly necessary to reduce the effects of loss and distortion on the lines. Thus, by placing loading circuits 10, 11 . . . n at regular intervals along one side of the line and loading circuits 10', 11' . . . n' in the other side of the line, (these loading circuits being negative impedances of the types disclosed herein) the line can be made lossless between the portions so compensated, as is common knowledge, a suitable repeater spacing corresponds roughly to a quarter wavelength at the highest frequency of such a range. By providing in the central office a regulated current source suitable to bias the respective loading circuits in their negative resistance regions and by providing suitable resistive terminations, the line may be rendered essentially distortionless and lossless over a given frequency range. Due to the simplicity of the circuit embodiments disclosed, such an arrangement provides an economically attractive technique for improving bi-directional two-wire transmission lines and consequently improving subscriber service.

WHAT WE CLAIM IS:—

1. A two-terminal negative impedance converter comprising two transistor devices of opposite conductivity type each having a collector, an emitter and a base, having the base of each connected to the collector of the other and each of the emitters being connected to

a respective one of the two terminals, means for biasing each of the transistor devices comprising an impedance connected between respective base and emitter electrodes of each transistor device, and a control impedance connected between the two bases, the arrangement being such that on the application of a suitable current source across the two terminals, the transistor devices are each biased in a linear region of operation, and the impedance produced between the emitters is proportional to the negative of the control impedance.

2. A two-terminal negative impedance converter comprising a semiconductive device having four successive zones of alternatively opposite conductivity type capable of exhibiting current amplification, the two terminals being connected respectively to the outer zones, respective biasing means including an impedance connected between each outer zone and the next adjacent zone, and a control impedance connected between the two inner zones, the arrangement being such that the application of a suitable current source across the two terminals result in a negative impedance across the two terminals the value of which is proportional to the negative of the control impedance.

3. A converter according to claim 1 wherein the two transistor devices are compound transistors each comprising two transistors of like conductivity type having their collectors connected directly together to form the collector of the device, the base of one forming the base of the device and the emitter of the other forming the emitter of the device, the remaining two electrodes being connected directly together.

4. A converter according to claim 1 wherein the transistor devices each consists of a first transistor having its base connected to one end of the control impedance and its collector connected through the base-emitter path of a further transistor of opposite conductivity type to the first to the other end of the control impedance, the collector of the further transistor being connected to the emitter of the first which is connected to one of the said terminals, so that voltage variations in the biasing means produce an amplified current input to the associated first transistor to increase the linearity of the negative impedance.

5. A converter according to any preceding claim wherein the biasing impedances are resistors.

6. A converter according to claim 1, 3 or 4 including in series with the emitter of each transistor device a feedback impedance to linearise the negative impedance portion of the current-voltage characteristic.

7. A converter according to claim 6 wherein the feedback impedances are resistors.

8. A converter according to any preceding claim wherein the control impedance has a



circuit of Fig. 5, as resistors R1 and R2 each bridge only a single emitter-base junction.

Another effect of this circuit configuration is an increase in the value of the proportionality constant k toward unity to cause the negative terminal resistance to more closely approximate the value of resistor R3. If desired, emitter feedback resistances corresponding to those shown in Fig. 4 may be inserted in conductors d and e of Fig. 6 to establish a stable preferred value of constant k that is less than unity. It is to be recognized that appropriately valued resistors may, if needed, be connected between the base and the emitter of transistor Q1_a to prevent thermal instability and to ensure that transistor Q1_a is not operated unwantedly by the reverse-bias collector current (I_{co}) of transistor Q1_a. A similar statement can be made for the inclusion of a resistor between the base and the emitter of transistor Q2_a.

Fig. 7 illustrates one specific application of any one of the circuits shown in the respective embodiments. This figure serves to illustrate how it is possible to obtain a long telephone transmission line connected between a telephone central office 7 at one location and a distant station set 8 at a subscriber's location in a simple, stable, versatile and inexpensive manner. By using the negative impedance elements of the type described, it is possible to reduce wire size and eliminate equalizers and bulky loading coils formerly necessary to reduce the effects of loss and distortion on the lines. Thus, by placing loading circuits 10, 11 . . . n at regular intervals along one side of the line and loading circuits 10', 11' . . . n' in the other side of the line, (these loading circuits being negative impedances of the types disclosed herein) the line can be made lossless between the portions so compensated, as is common knowledge, a suitable repeater spacing corresponds roughly to a quarter wavelength at the highest frequency of such a range. By providing in the central office a regulated current source suitable to bias the respective loading circuits in their negative resistance regions and by providing suitable resistive terminations, the line may be rendered essentially distortionless and lossless over a given frequency range. Due to the simplicity of the circuit embodiments disclosed, such an arrangement provides an economically attractive technique for improving bi-directional two-wire transmission lines and consequently improving subscriber service.

WHAT WE CLAIM IS:—

1. A two-terminal negative impedance converter comprising two transistor devices of opposite conductivity type each having a collector, an emitter and a base, having the base of each connected to the collector of the other and each of the emitters being connected to

a respective one of the two terminals, means for biasing each of the transistor devices comprising an impedance connected between respective base and emitter electrodes of each transistor device, and a control impedance connected between the two bases, the arrangement being such that on the application of a suitable current source across the two terminals, the transistor devices are each biased in a linear region of operation, and the impedance produced between the emitters is proportional to the negative of the control impedance.

2. A two-terminal negative impedance converter comprising a semiconductive device having four successive zones of alternatively opposite conductivity type capable of exhibiting current amplification, the two terminals being connected respectively to the outer zones, respective biasing means including an impedance connected between each outer zone and the next adjacent zone, and a control impedance connected between the two inner zones, the arrangement being such that the application of a suitable current source across the two terminals result in a negative impedance across the two terminals the value of which is proportional to the negative of the control impedance.

3. A converter according to claim 1 wherein the two transistor devices are compound transistors each comprising two transistors of like conductivity type having their collectors connected directly together to form the collector of the device, the base of one forming the base of the device and the emitter of the other forming the emitter of the device, the remaining two electrodes being connected directly together.

4. A converter according to claim 1 wherein the transistor devices each consists of a first transistor having its base connected to one end of the control impedance and its collector connected through the base-emitter path of a further transistor of opposite conductivity type to the first to the other end of the control impedance, the collector of the further transistor being connected to the emitter of the first which is connected to one of the said terminals, so that voltage variations in the biasing means produce an amplified current input to the associated first transistor to increase the linearity of the negative impedance.

5. A converter according to any preceding claim wherein the biasing impedances are resistors.

6. A converter according to claim 1, 3 or 4 including in series with the emitter of each transistor device a feedback impedance to linearise the negative impedance portion of the current-voltage characteristic.

7. A converter according to claim 6 wherein the feedback impedances are resistors.

8. A converter according to any preceding claim wherein the control impedance has a

(14)

capacitor connected across it to provide dynamic stability of the converter.

- 5 9. A converter according to any preceding claim in which the control impedance is a resonance.

- 10 10. A transmission line including one or more converters according to any preceding claim in series with each of its conductors so as to reduce the effect of the distributed resistance of the conductor.

- 15 11. A transmission line according to claim 10 wherein the converters are spaced along the conductors at approximately a quarter of a wavelength of the highest frequency signal to be transmitted by the line.

12. A converter substantially as herein described with reference to and as shown in Fig. 1 or Figs. 3A and 3B or Fig. 4 or Fig. 5 or Fig. 6 of the accompanying drawings.

13. A transmission line including one or more converters according to claim 12 in series with its conductors substantially as herein described with reference to and as shown in Fig. 7 of the accompanying drawings.

25

P. S. BROWN,
Chartered Patent Agent.
5, Mornington Road,
Woodford Green, Essex.
Agent for the Applicants.

Printed for Her Majesty's Stationery Office by the Courier Press, Leamington Spa, 1969.

Published by the Patent Office, 25, Southampton Buildings, London, W.C.2, from which copies may be obtained.



* C L N S *