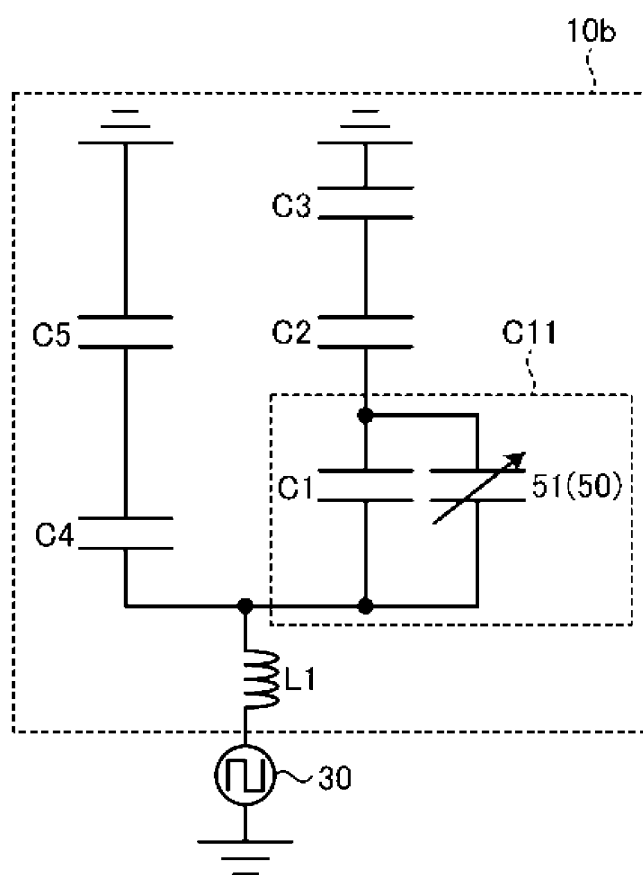


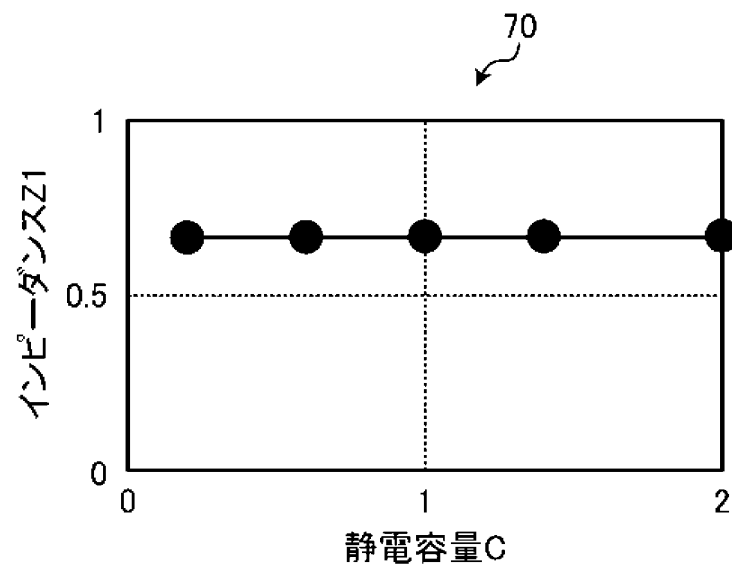




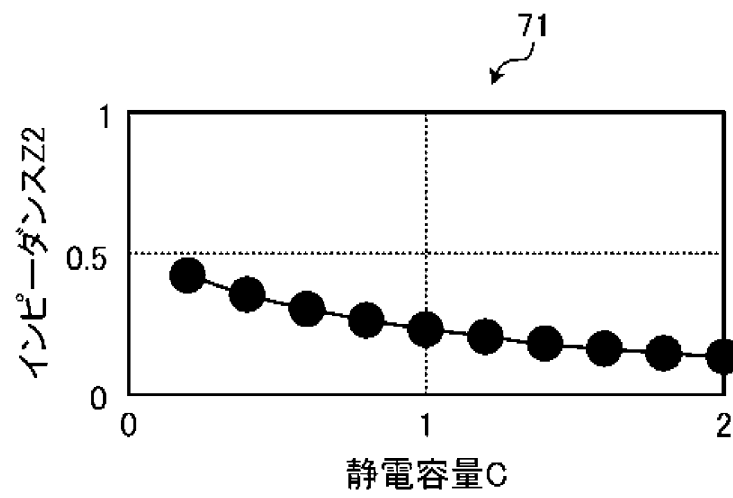
[図3]



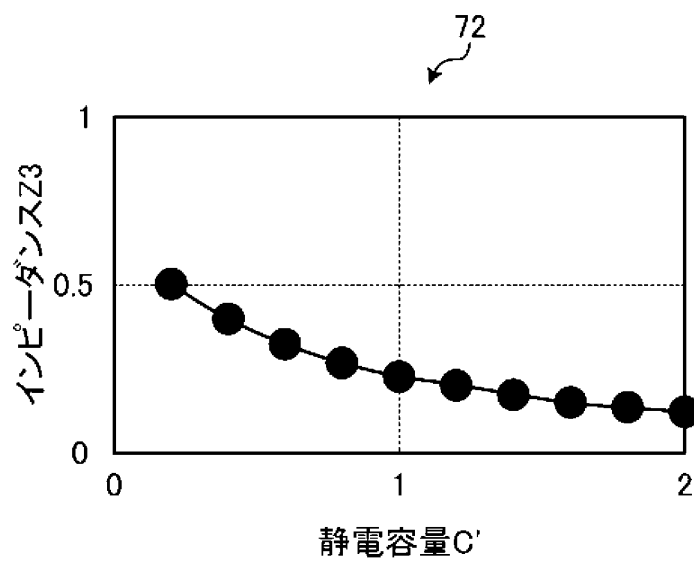
[illegible]



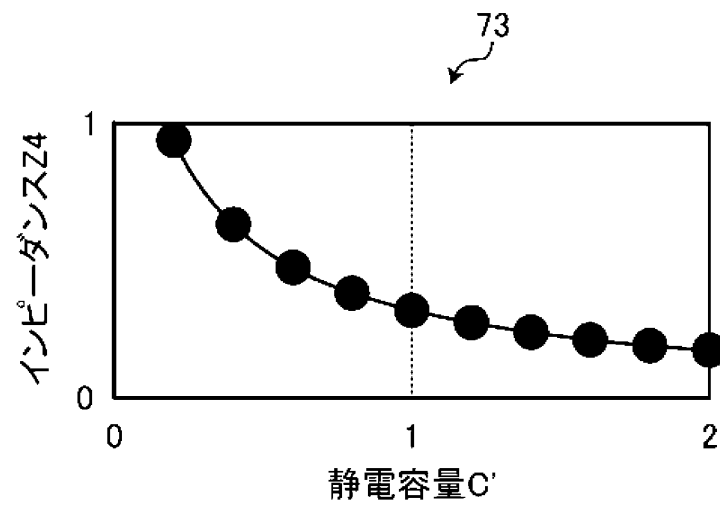
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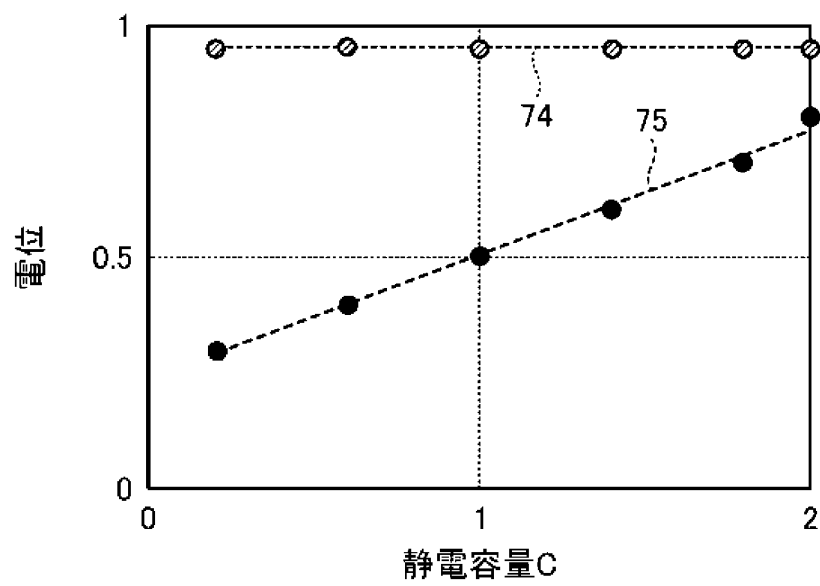
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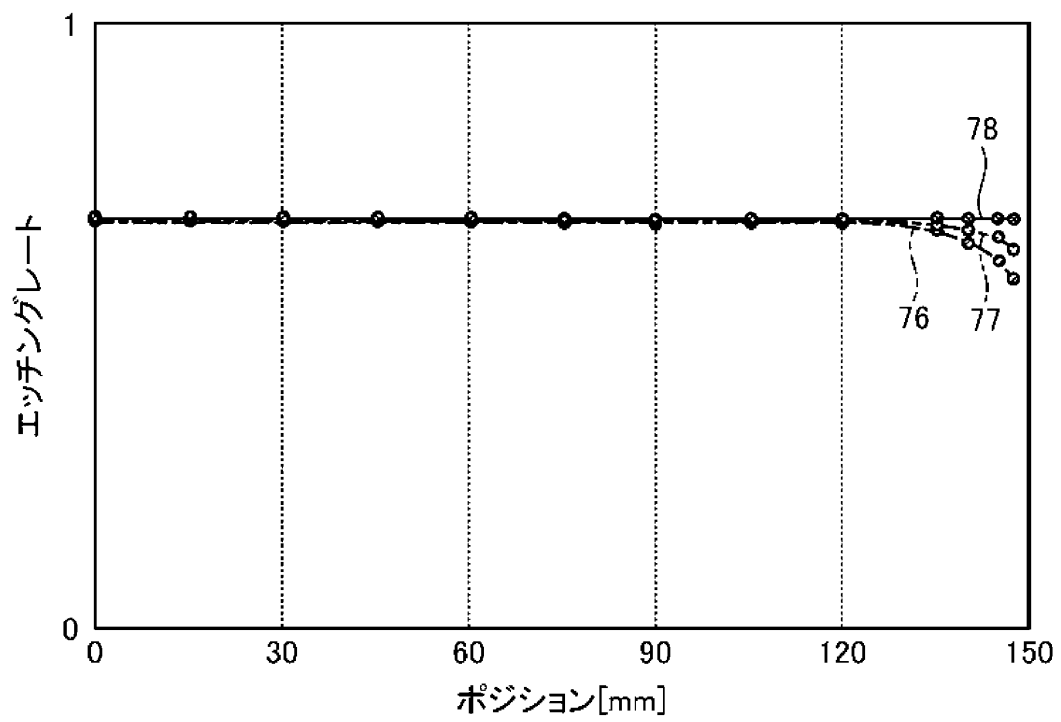
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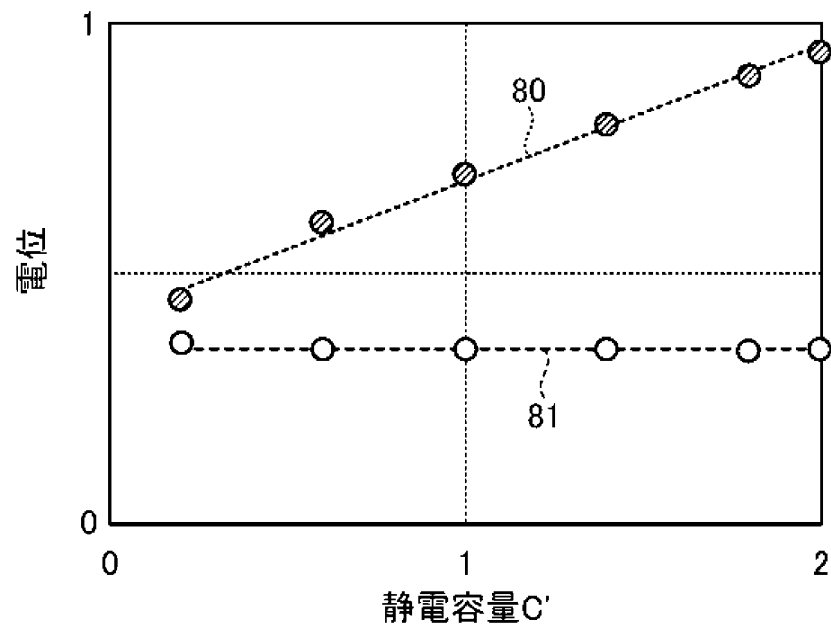
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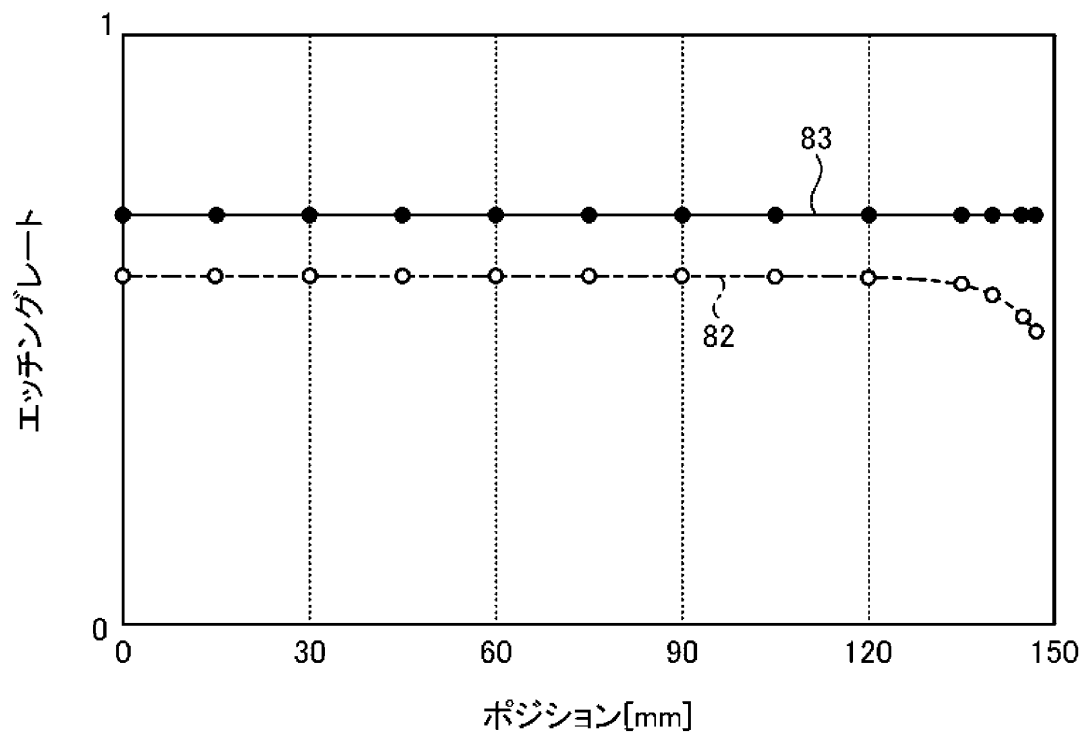
[図11]



[図12]



[図13]



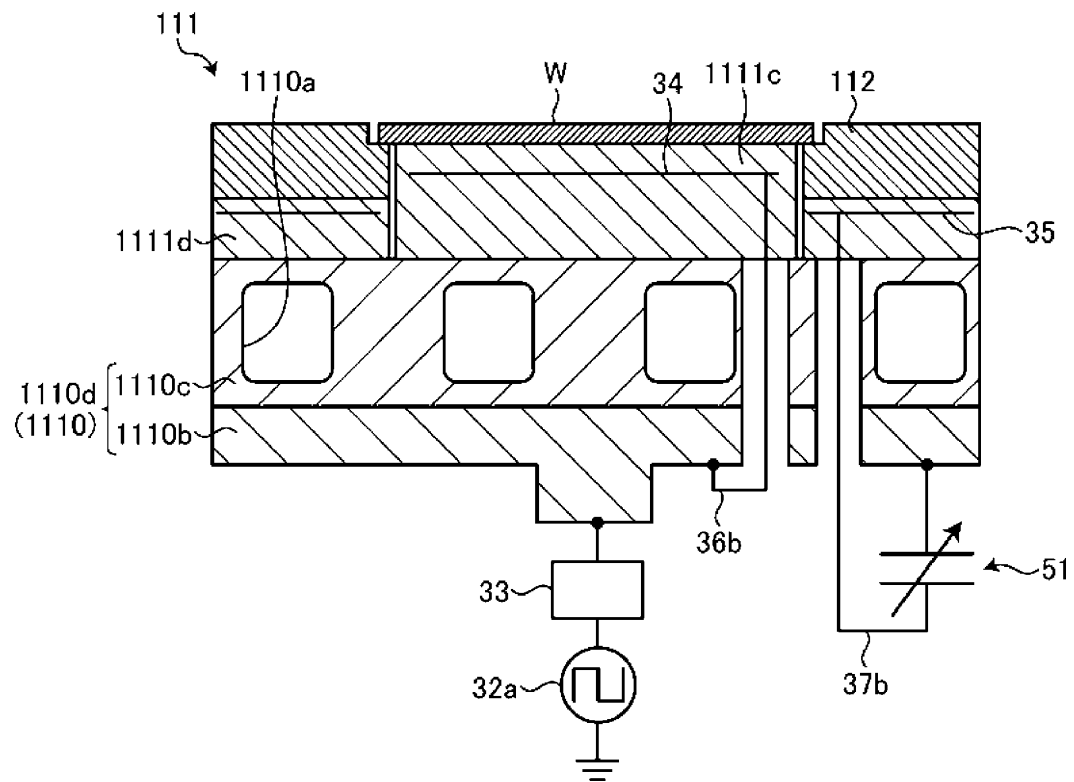




[illegible]

This cross-sectional view shows a semiconductor device with a substrate 110 containing a memory array of square cells. A top layer 111 is patterned into regions 1110a and 1112. A word line W is positioned above the array. A peripheral circuit 30 is located on the right, including a gate stack 34, a gate 35, and a vertical line 36b. The circuit is connected to a power source 32a and a control line 33. A dashed box 50 encloses a portion of the circuit, showing a transistor 51 and a capacitor 55 connected to ground.

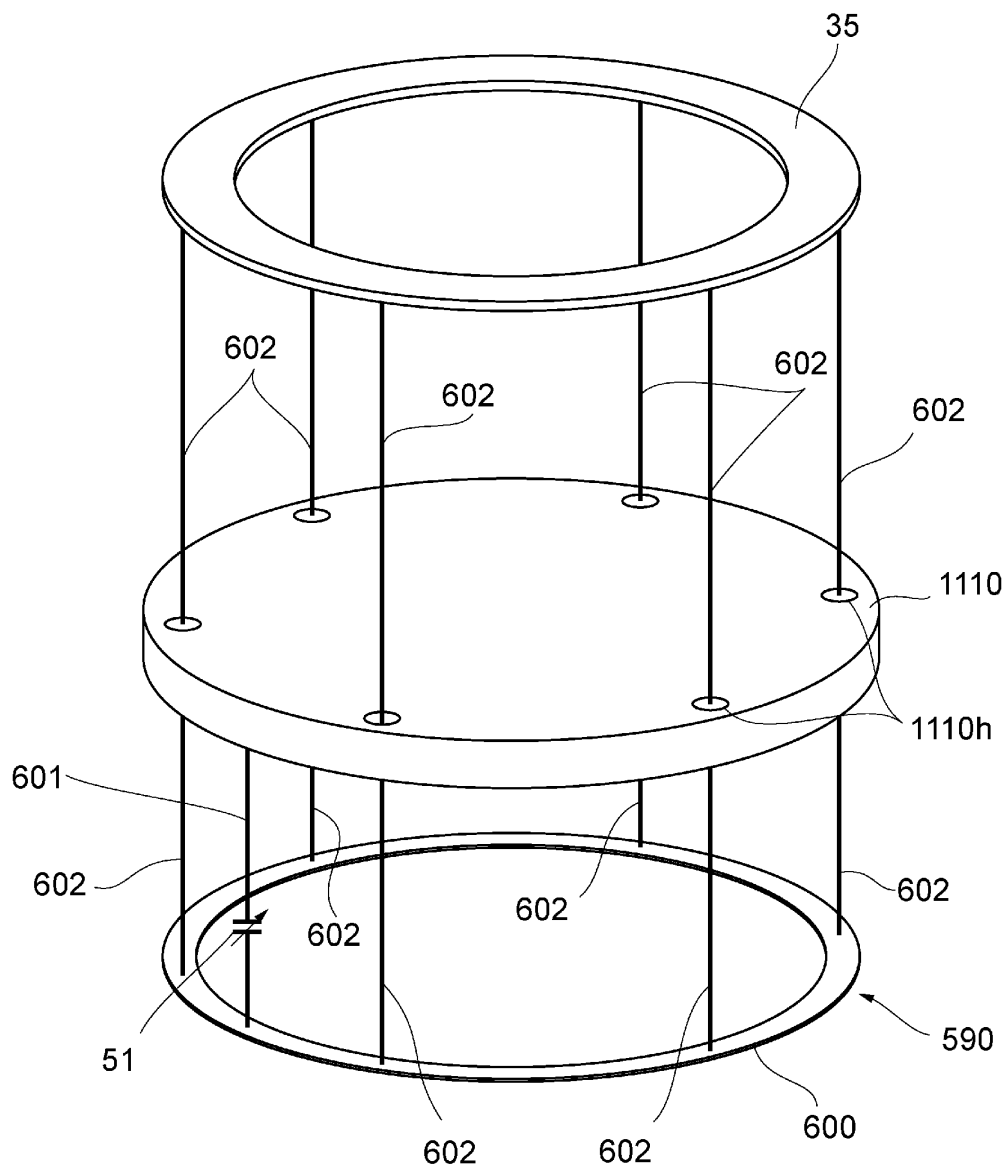
[図18]



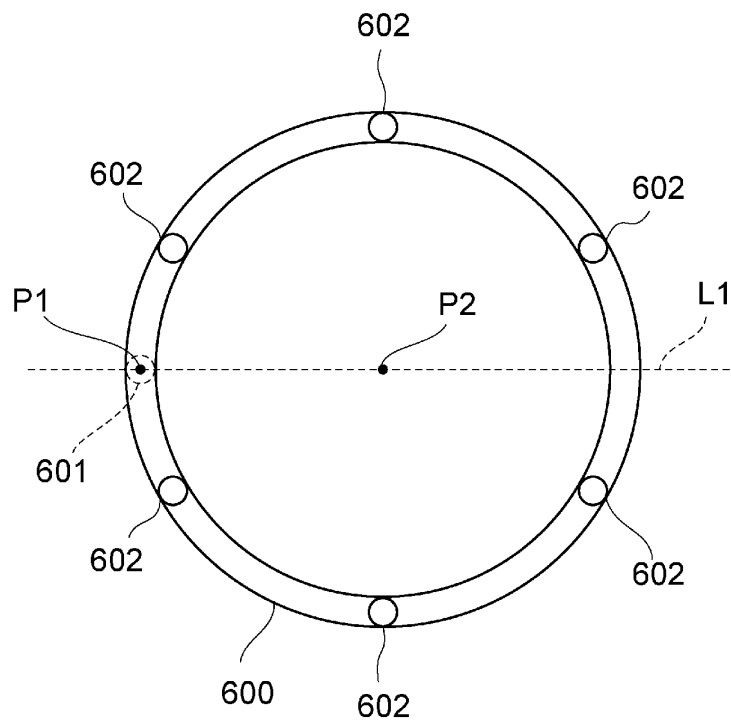




[図21]

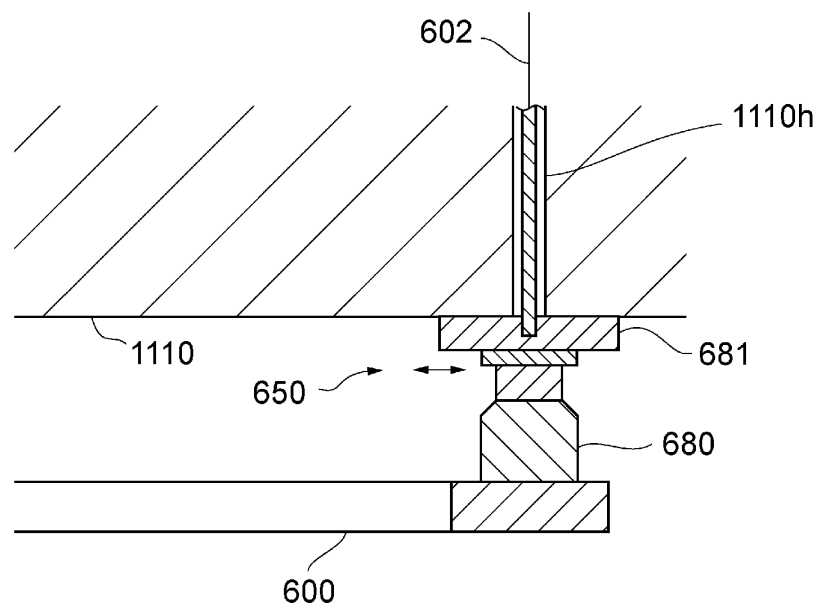


[図22]

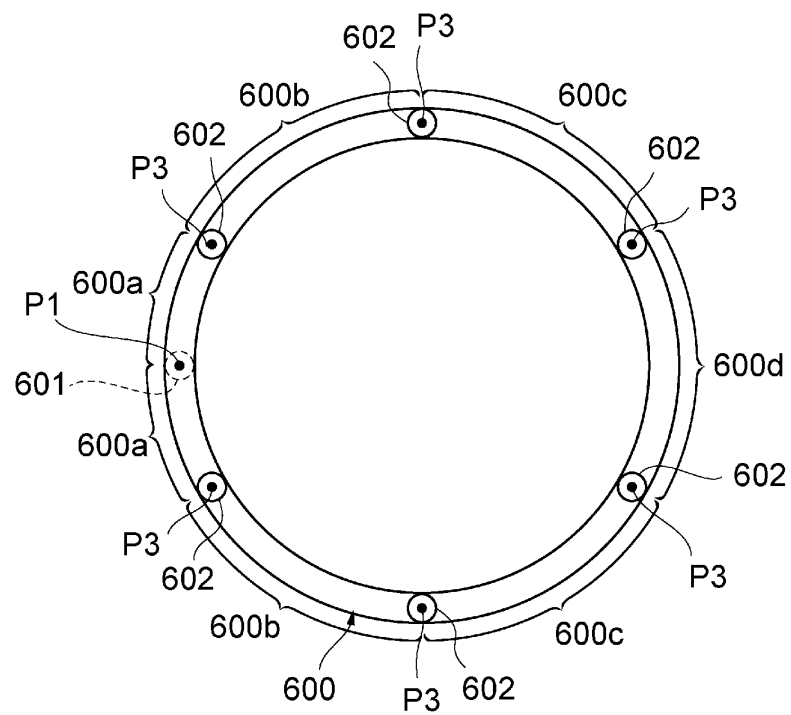


[illegible]

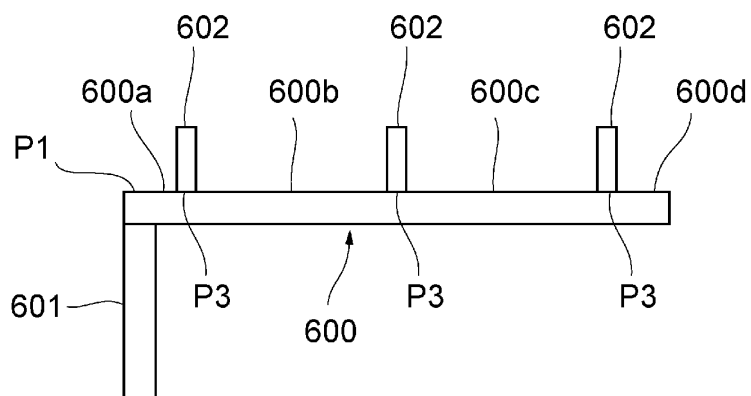
[図25]



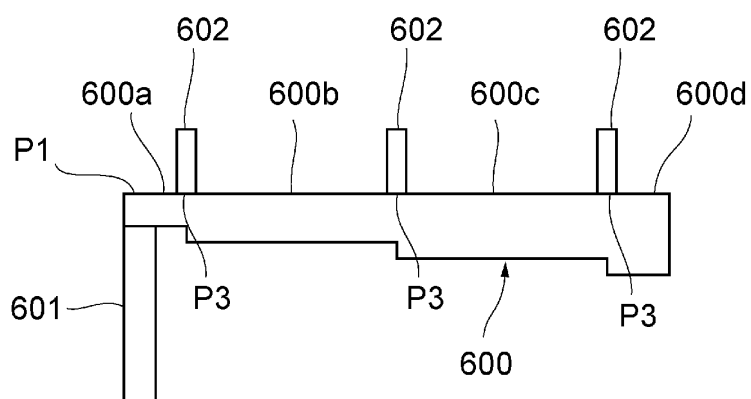
[図26]



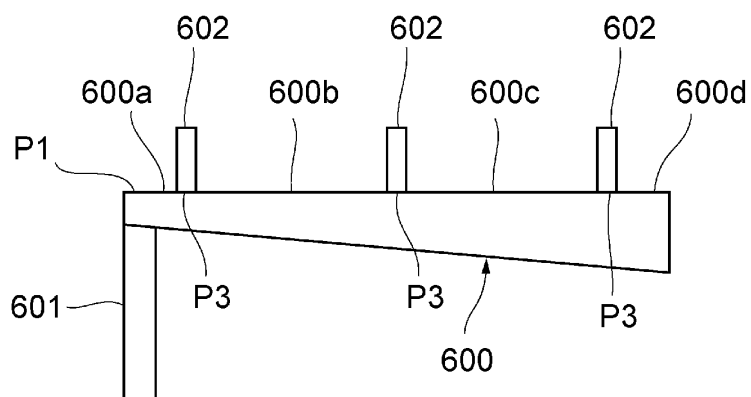
[図27]



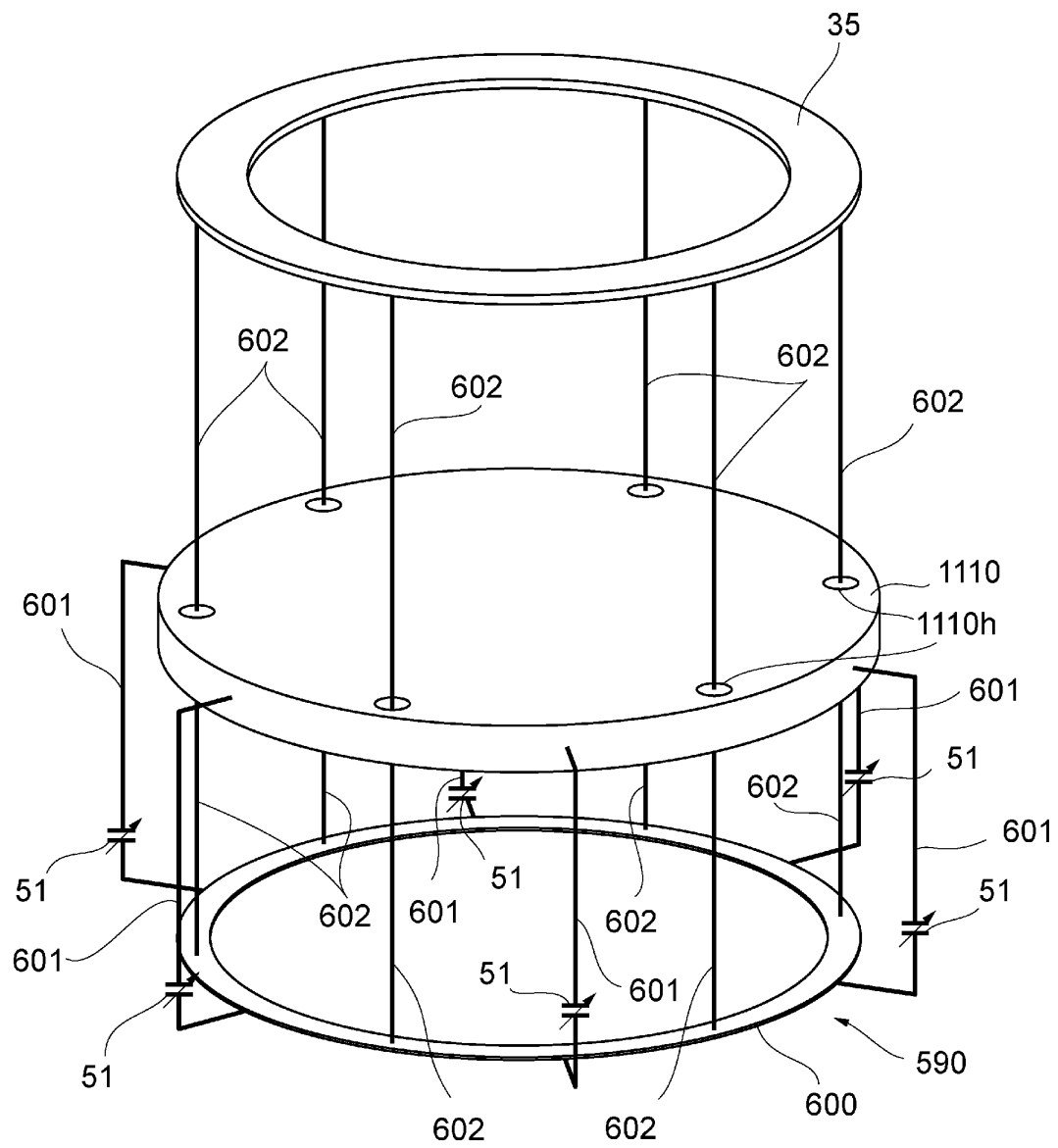
[図28]



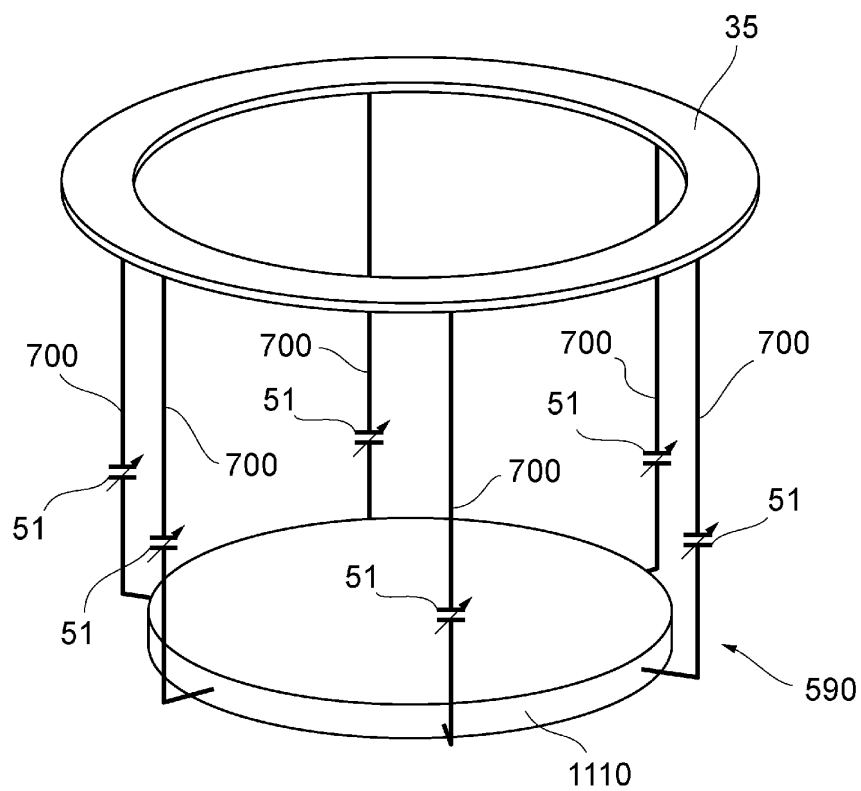
[図29]



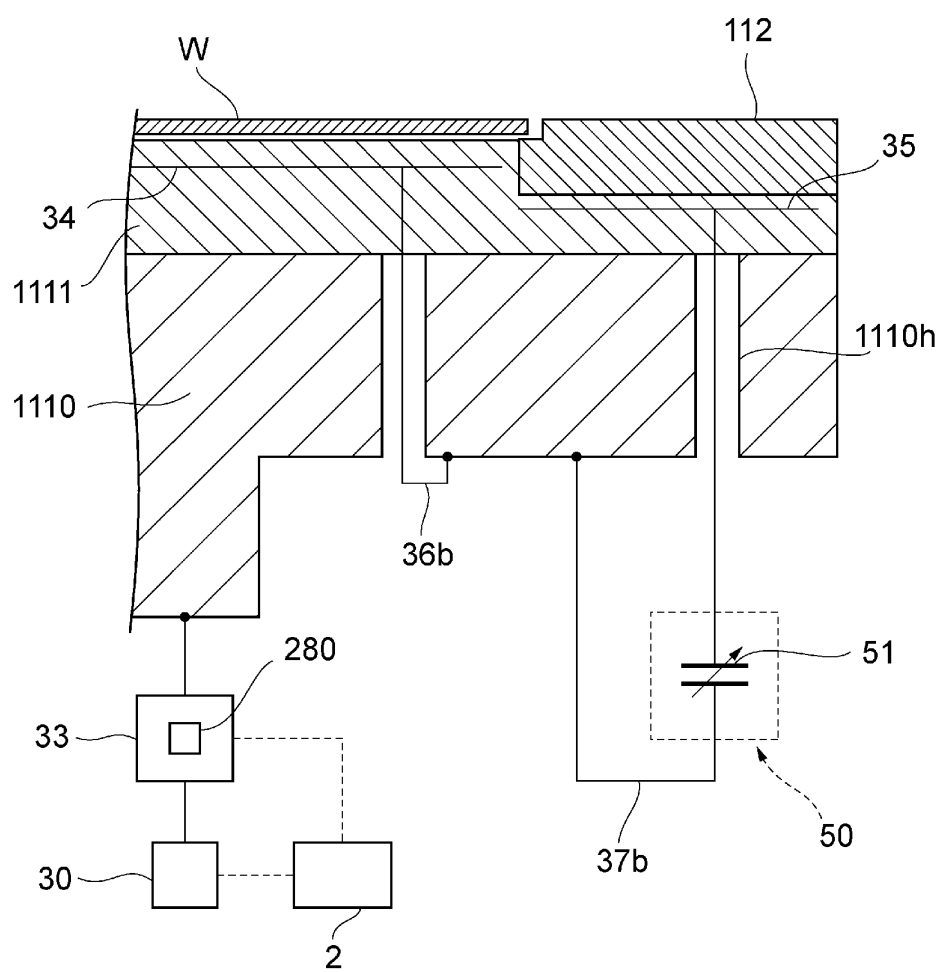
[図30]



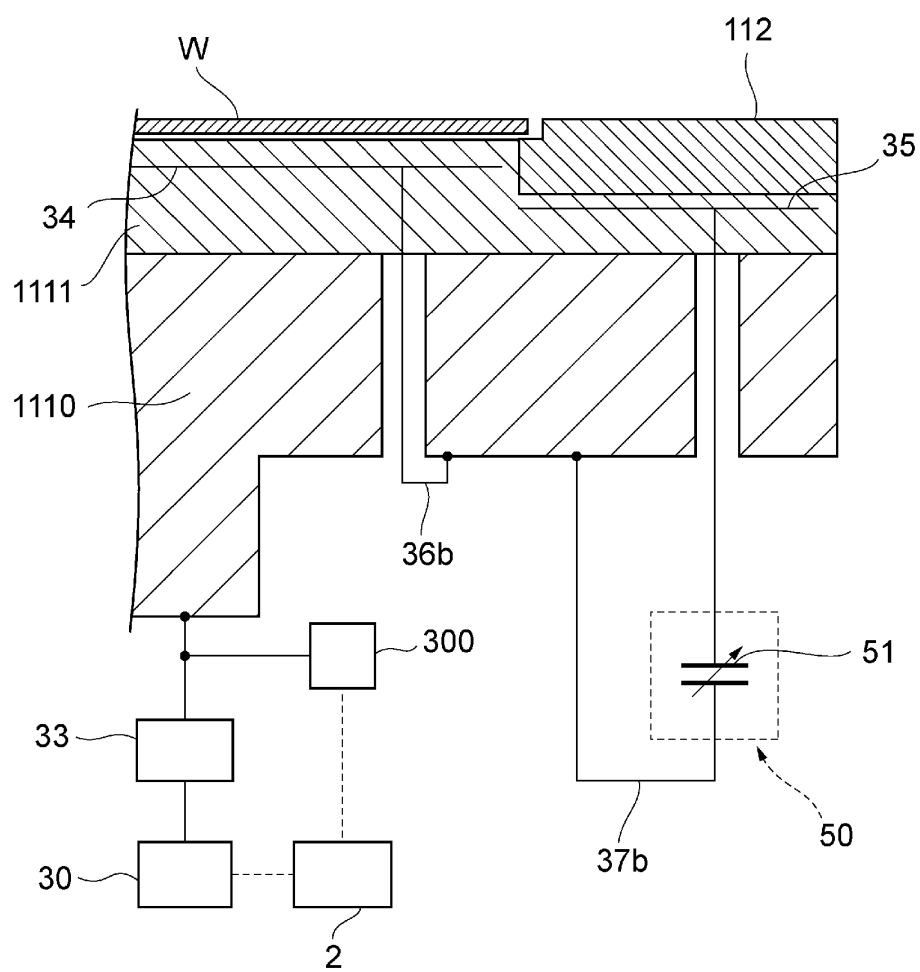
[図31]



[図32]

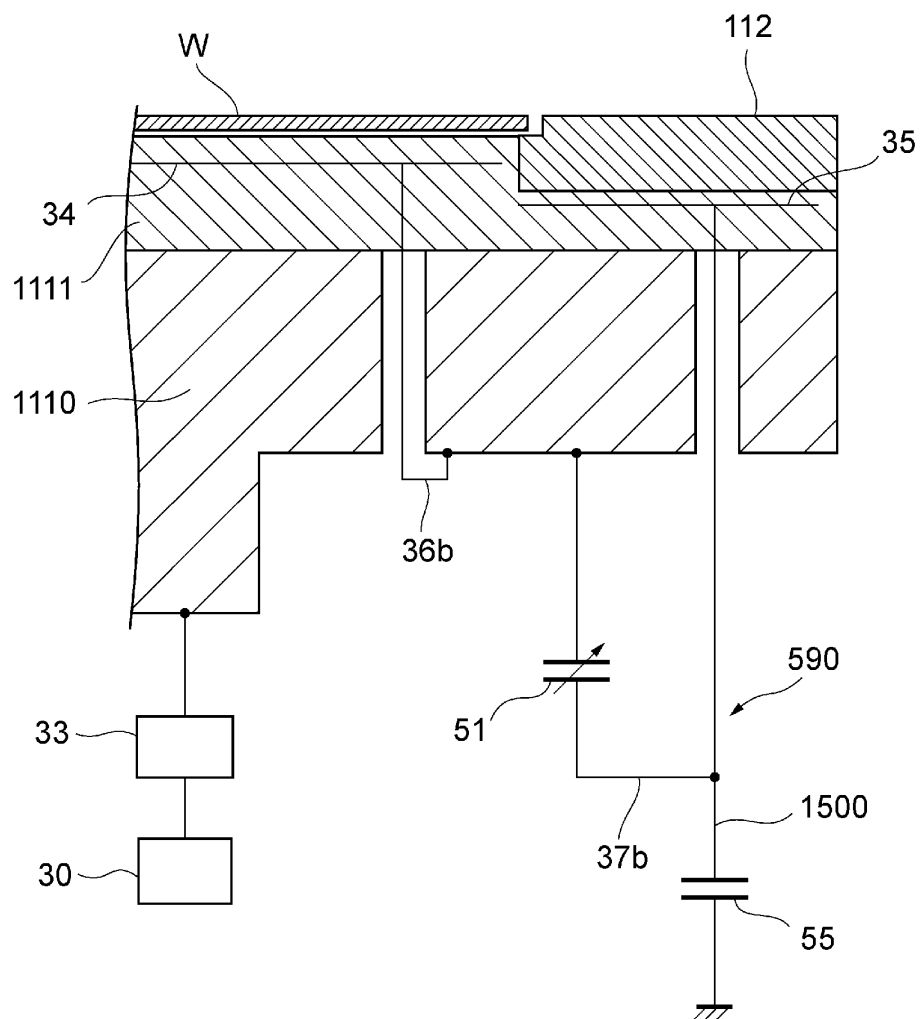


[図33]

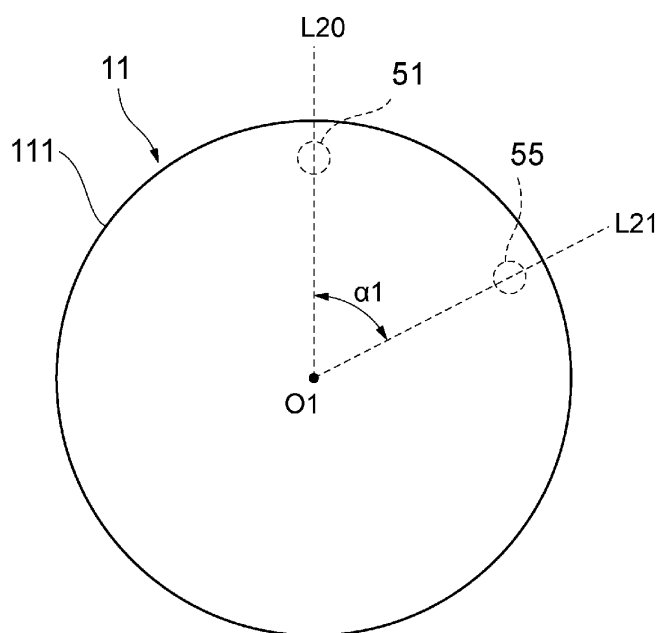




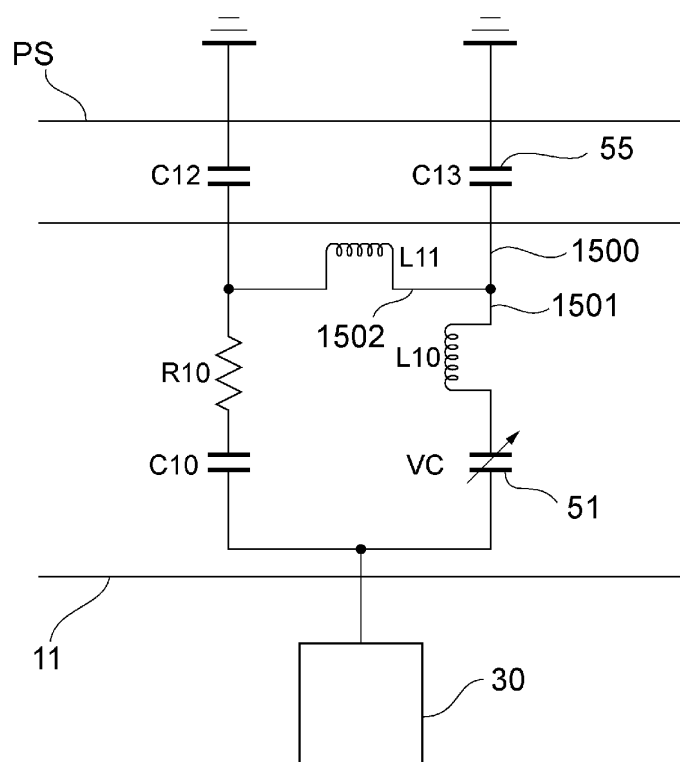
[図35]



[図36]

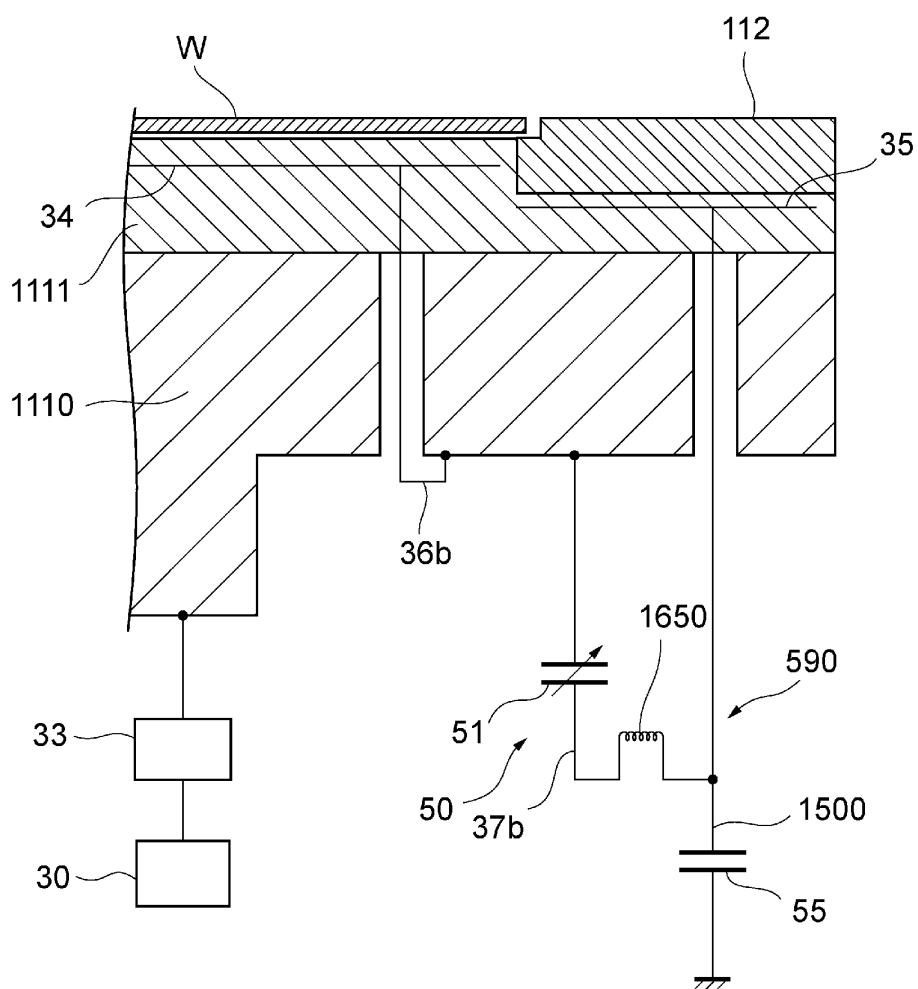


[図37]

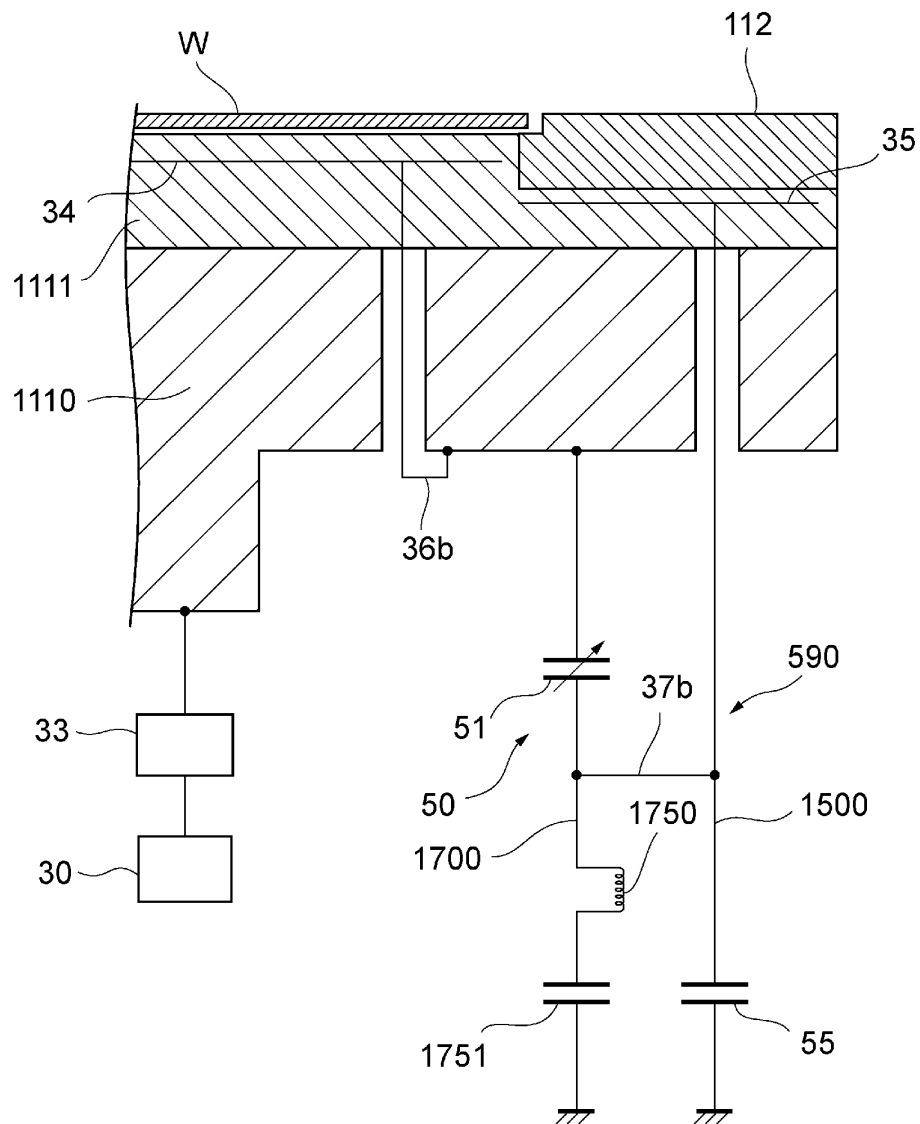




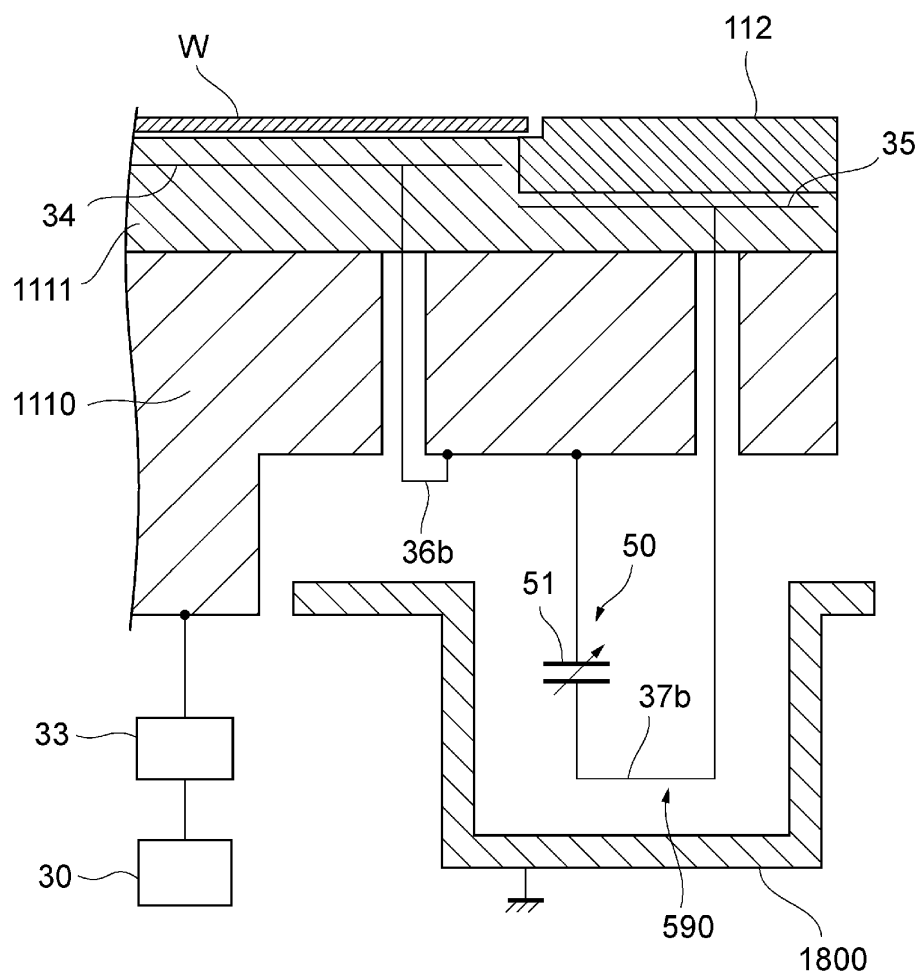
[図39]



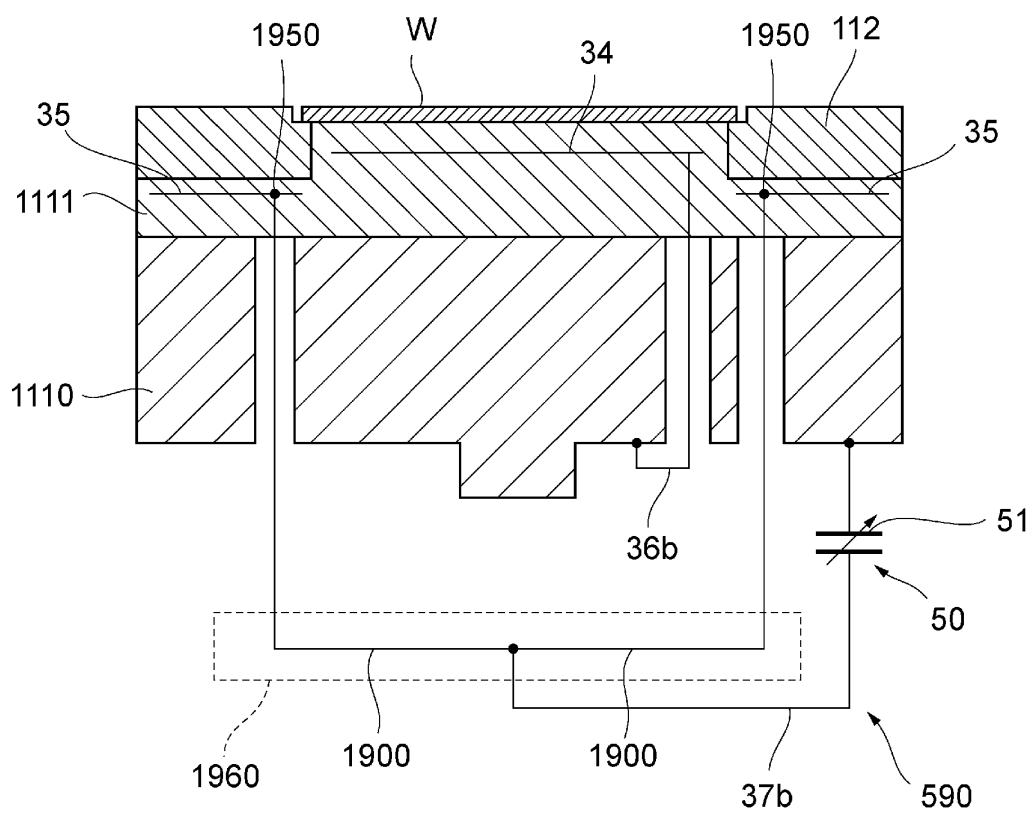
[図40]



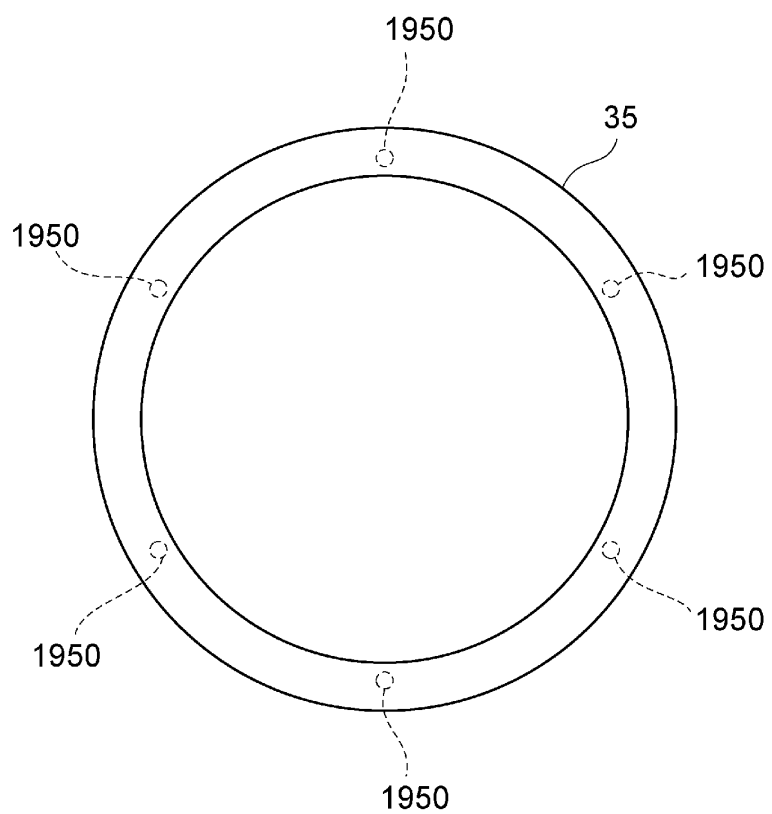
[図41]



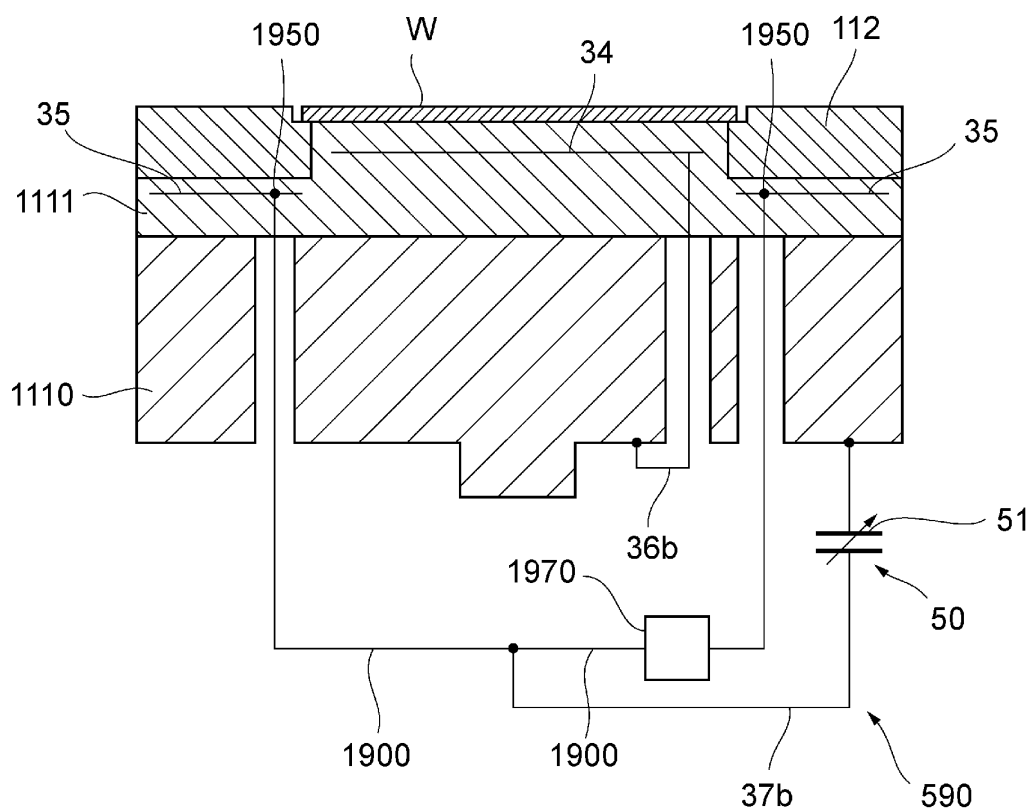
[図42]



[図43]

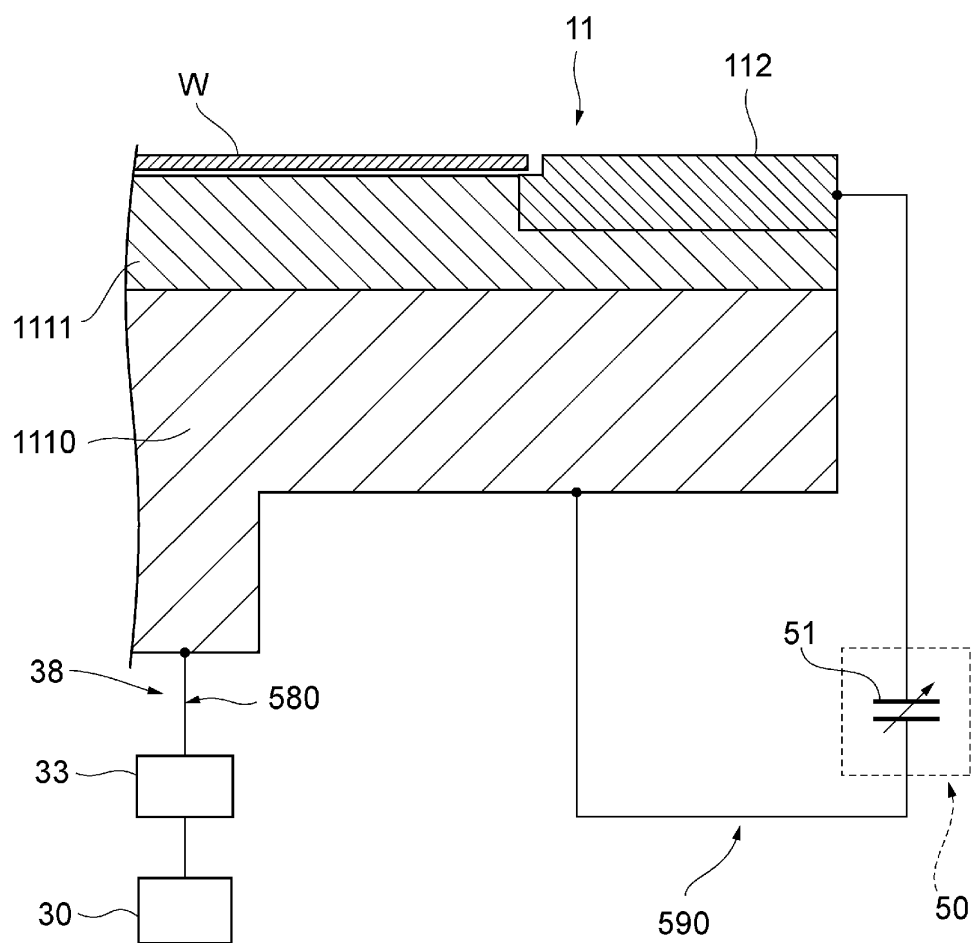


[図44]



A cross-sectional view of a semiconductor device 11. The device features a substrate 30 with a first semiconductor layer 33 and a second semiconductor layer 34. A gate stack 38 is formed on the substrate, with a gate insulating layer 580 and a gate electrode 590. A source/drain region 51 is formed in the second semiconductor layer 34, with a source/drain insulating layer 50. A contact plug 35 is formed in the source/drain region 51, with a contact insulating layer 112. A contact pad 111 is formed on the contact plug 35, with a contact insulating layer 110. A contact pad 111 is also formed on the gate stack 38, with a contact insulating layer 110. A contact pad 111 is also formed on the substrate 30, with a contact insulating layer 110.

[図46]



[図47]

