SEMICONDUCTOR MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This patent application claims priority to Korean Patent Application No. 10-2022-0136796, filed on 21 October 2022, in the Korean Intellectual Property Office, the entire contents of which are hereby incorporated by reference.

TECHNICAL FIELD

[0002] The present disclosure relates to a semiconductor memory device and a method of manufacturing the same, and more particularly, to a semiconductor memory device including a SRAM cell and a method of manufacturing the same.

BACKGROUND

[0003] Semiconductor devices are widely used in an electronic industry because of their small sizes, multi-functional characteristics, and/or low manufacturing costs. Semiconductor devices may be categorized as any one of semiconductor memory devices for storing logical data, semiconductor logic devices for processing logical data, and hybrid semiconductor devices having both the function of the semiconductor memory devices and the function of the semiconductor logic devices. Semiconductor devices with excellent characteristics have been increasingly in demand with the development of the electronic industry. For example, high-reliable, high-speed and/or multi-functional semiconductor devices have been increasingly in demand. To satisfy these demands, semiconductor devices have been highly integrated and structures in semiconductor devices have become more and more complicated.

SUMMARY

[0004] In an aspect, a semiconductor memory device may include a substrate including a first surface and a second surface opposite to the first surface, a first active pattern on the first surface, a first channel pattern on the first active pattern and a first source/drain pattern connected to the first channel pattern, a gate electrode provided on the first channel pattern and extending in a first direction, the gate electrode adjacent to the first source/drain pattern in a second direction intersecting the first direction, a shared contact provided under the first source/drain pattern and the gate electrode and electrically connecting the first source/drain pattern and the gate electrode to each other, and a backside metal layer on the second surface.

[0005] In an aspect, a semiconductor memory device may include a SRAM cell on a substrate. The SRAM cell may include first pull-up/down transistors and second pull-up/down transistors; and a first node connecting a common source/drain of the first pull-up/down transistors to a common gate of the second pull-up/down transistors. The first node may include a shared contact connected to the common source/drain and the common gate to electrically connect the common source/drain and the common gate to each other. The shared contact may be buried in a lower portion of the substrate. The shared contact may include a backside active contact electrically connected to the common source/drain; and a backside gate contact electrically connected to the common gate.

[0006] In an aspect, a semiconductor memory device may include a substrate including a bit cell region; a first active pattern and a second active pattern on the bit cell region, the first active pattern spaced apart from the second active pattern in a first direction; a device isolation layer filling a trench between the first and second

active patterns; a first channel pattern on the first active pattern and a first source/drain pattern connected to the first channel pattern; a second channel pattern on the second active pattern and a second source/drain pattern connected to the second channel pattern; a gate electrode provided on the first channel pattern and extending in the first direction; a gate insulating layer between the gate electrode and the first channel pattern; a gate spacer on at least one sidewall of the gate electrode; a gate capping pattern on the gate electrode; an interlayer insulating layer on the gate capping pattern; an active contact penetrating the interlayer insulating layer so as to be connected to the second source/drain pattern; a first metal layer on the interlayer insulating layer, the first metal layer including a bit line electrically connected to the active contact; and a shared contact provided under the first source/drain pattern and the gate electrode and electrically connecting the first source/drain pattern and the gate electrode to each other.

[0007] In an aspect, a method of manufacturing a semiconductor memory device may include forming an active pattern on a front surface of a substrate; forming a channel pattern and a source/drain pattern on the active pattern; forming a gate electrode extending in a first direction on the channel pattern; forming a backside contact hole exposing the source/drain pattern and the gate electrode through a back surface of the substrate; and forming a shared contact in the backside contact hole. The shared contact may electrically connect the source/drain pattern and the gate electrode to each other.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Features will become apparent to those of skill in the art by describing in detail exemplary embodiments with reference to the attached drawings in which:

[0009] FIG. 1 is an equivalent circuit diagram illustrating a SRAM cell according to some embodiments.

[0010] FIG. 2 is a perspective view illustrating interconnection layers of a semiconductor memory device according to some embodiments.

[0011] FIG. 3A is a plan view of a first surface of a substrate to illustrate a semiconductor memory device according to some embodiments.

[0012] FIG. 3B is a plan view of a second surface of the substrate to illustrate a semiconductor memory device according to some embodiments.

[0013] FIG. 4A is a cross-sectional view taken along lines A-A' of FIGS. 3A and 3B.

[0014] FIG. 4B is a cross-sectional view taken along lines B-B' of FIGS. 3A and 3B.

[0015] FIG. 4C is a cross-sectional view taken along lines C-C' of FIGS. 3A and 3B.

[0016] FIG. 4D is a cross-sectional view taken along lines D-D' of FIGS. 3A and 3B.

[0017] FIG. 4E is a cross-sectional view taken along lines E-E' of FIGS. 3A and 3B.

[0018] FIGS. 5A, 5B, 5C, 6A, 6B, 6C, 7A, 7B, 7C, 8A, 8B, 8C, 9A, 9B, 9C, 9D, 10A, 10B and 10C are cross-sectional views illustrating a method of manufacturing a semiconductor memory device according to some embodiments.

[0019] FIGS. 11, 12, 13, 14 and 15 are cross-sectional views illustrating semiconductor memory devices according to some embodiments.

[0020] FIG. 16A is a plan view of a first surface of a substrate to illustrate a semiconductor memory device according to some embodiments.

[0021] FIG. 16B is a plan view of a second surface of the substrate to illustrate a semiconductor memory device according to some embodiments.

DETAILED DESCRIPTION

[0022] FIG. 1 is an equivalent circuit diagram illustrating a SRAM cell according to some embodiments.

[0023] Referring to FIG. 1, a SRAM cell according to some embodiments may include a first pull-up transistor TU1, a first pull-down transistor TD1, a second pull-up transistor TU2, a second pull-down transistor TD2, a first pass-gate transistor TA1, and a second pass-gate transistor TA2. The first and second pull-up transistors TU1 and TU2 may be PMOS transistors. The first and second pull-down transistors TD1 and TD2 and the first and second pass-gate transistors TA1 and TA2 may be NMOS transistors.

[0024] A first source/drain of the first pull-up transistor TU1 and a first source/drain of the first pull-down transistor TD1 may be connected to a first node N1. A second source/drain of the first pull-up transistor TU1 may be connected to a power line VDD, and a second source/drain of the first pull-down transistor TD1 may be connected to a ground line VSS. A gate of the first pull-up transistor TU1 may be electrically connected to a gate of the first pull-down transistor TD1. The first pull-up transistor TU1 and the first pull-down transistor TD1 may constitute a first inverter. The gates, connected to each other, of the first pull-up and first pull-down transistors TU1 and TD1 may correspond to an input terminal of the first inverter, and the first node N1 may correspond to an output terminal of the first inverter.

[0025] A first source/drain of the second pull-up transistor TU2 and a first source/drain of the second pull-down transistor TD2 may be connected to a second node N2. A second source/drain of the second pull-up transistor TU2 may be connected to the power line VDD, and a second source/drain of the second pull-down

transistor TD2 may be connected to the ground line VSS. A gate of the second pull-up transistor TU2 may be electrically connected to a gate of the second pull-down transistor TD2. Thus, the second pull-up transistor TU2 and the second pull-down transistor TD2 may constitute a second inverter. The gates, connected to each other, of the second pull-up and second pull-down transistors TU2 and TD2 may correspond to an input terminal of the second inverter, and the second node N2 may correspond to an output terminal of the second inverter.

[0026] The first and second inverters may be coupled to each other to constitute a latch structure. In other words, the gates of the first pull-up and first pull-down transistors TU1 and TD1 may be electrically connected to the second node N2, and the gates of the second pull-up and second pull-down transistors TU2 and TD2 may be electrically connected to the first node N1. A first source/drain of the first pass-gate transistor TA1 may be connected to the first node N1, and a second source/drain of the first pass-gate transistor TA1 may be connected to a first bit line BL1. A first source/drain of the second pass-gate transistor TA2 may be connected to the second node N2, and a second source/drain of the second pass-gate transistor TA2 may be connected to a second bit line BL2. Gates of the first and second pass-gate transistors TA1 and TA2 may be electrically connected to a word line WL. Thus, the SRAM cell according to the embodiments may be realized.

[0027] FIG. 2 is a perspective view illustrating interconnection layers of a semiconductor memory device according to some embodiments.

[0028] Referring to FIG. 2, memory cells CE1 to CE4 may be provided on a substrate 100. The memory cells CE1 to CE4 may include first to fourth bit cells CE1 to CE4 arranged in a 2×2 matrix form. Each of the first to fourth bit cells CE1

to CE4 may be the SRAM cell described above with reference to FIG. 1. Detailed structures of the first to fourth bit cells CE1 to CE4 will be described below with reference to FIGS. 3A to 4E.

[0029] The substrate 100 may include a first surface 100A and a second surface 100B opposite to the first surface 100A. The first surface 100A may be a front surface of the substrate 100. The second surface 100B may be a back surface of the substrate 100.

[0030] A first metal layer M1 may be provided on the first surface 100A of the substrate 100. The first metal layer M1 may be a lowermost metal layer of a BEOL layer. A backside metal layer BSM may be provided on the second surface 100B of the substrate 100. The backside metal layer BSM may be an uppermost metal layer of a backside power delivery network layer. Each of the first metal layer M1 and the backside metal layer BSM may include at least one of a conductive metal nitride (e.g., titanium nitride or tantalum nitride) or a metal material (e.g., titanium, tantalum, tungsten, copper, or aluminum).

[0031] The first metal layer M1 may include first bit lines BL1 and second bit lines BL2, which extend in a second direction D2. The first and second bit lines BL1 and BL2 may have line shapes when viewed in a plan view.

[0032] The first metal layer M1 may include word line pads WLP and dummy pads DMP. In some embodiments, the word line pad WLP and the dummy pad DMP may be provided at a side of each of the first and second bit lines BL1 and BL2. The word line pads WLP and the dummy pads DMP may be arranged in the second direction D2. Each of the word line pads WLP and the dummy pads DMP may have an island shape when viewed in a plan view. The word line pad WLP may be

electrically connected to a word line WL in a second metal layer M2. The dummy pad DMP may be a floated metal pattern.

[0033] One of the first bit lines BL1, one of the second bit lines BL2, two of the word line pads WLP and two of the dummy pads DMP may be located on the first bit cell CE1. In some embodiments, at least one or all of the dummy pads DMP may be omitted.

[0034] The backside metal layer BSM may include ground lines VSS and power lines VDD, which extend in the second direction D2. The ground lines VSS and the power lines VDD may be alternately arranged in a first direction D1. Each of the ground lines VSS and the power lines VDD may have a line shape when viewed in a plan view. One of the power lines VDD and two of the ground lines VSS may be located under the first bit cell CE1.

[0035] According to some embodiments, the ground line VSS and the power line VDD may be completely omitted from the BEOL layer, which includes the first metal layer M1 on the first surface 100A. The BEOL layer including the first metal layer M1 on the first surface 100A may include the bit lines BL1 and BL2 and word lines WL but not include the ground line VSS and the power line VDD.

[0036] FIG. 3A is a plan view of a first surface of a substrate to illustrate a semiconductor memory device according to an embodiment. FIG. 3B is a plan view of a second surface of the substrate to illustrate a semiconductor memory device according to some embodiments. FIG. 4A is a cross-sectional view taken along lines A-A' of FIGS. 3A and 3B. FIG. 4B is a cross-sectional view taken along lines B-B' of FIGS. 3A and 3B. FIG. 4C is a cross-sectional view taken along lines C-C' of FIGS. 3A and 3B. FIG. 4D is a cross-sectional view taken along lines D-D' of FIGS.

3A and 3B. FIG. 4E is a cross-sectional view taken along lines E-E' of FIGS. 3A and 3B. Each of the first to fourth bit cells CE1 to CE4 according to the present embodiments may include the SRAM cell according to the circuit diagram of FIG. 1.

[0037] Referring to FIGS. 1, 3A, 3B and 4A to 4E, first and second active patterns AP1 and AP2 may be provided on the first surface 100A of the substrate 100. The substrate 100 may be a semiconductor substrate including silicon, germanium or silicon-germanium, or a compound semiconductor substrate. A device isolation layer ST (see FIG. 4C) may include an insulating material such as a silicon oxide layer.

[0038] The first and second active patterns AP1 and AP2 may be on portions of the substrate 100. A trench TR may be defined between the active patterns AP1 and AP2 adjacent to each other. The device isolation layer ST may fill the trench TR.

[0039] Each of the bit cells CE1 to CE4 may include a pair of the first active patterns AP1 and a pair of the second active patterns AP2. Referring again to FIG. 1, one of the pair of second active patterns AP2 may include a body of the first pass-gate transistor TA1 and a body of the first pull-down transistor TD1. The other of the pair of second active patterns AP2 may include a body of the second pass-gate transistor TA2 and a body of the second pull-down transistor TD2.

[0040] One of the pair of first active patterns AP1 may include a body of the first pull-up transistor TU1. The other of the pair of first active patterns AP1 may include a body of the second pull-up transistor TU2.

[0041] A first channel pattern CH1 may be provided on the first active pattern AP1. A second channel pattern CH2 may be provided on the second active pattern AP2. Each of the first channel pattern CH1 and the second channel pattern CH2 may include a first semiconductor pattern SP1, a second semiconductor pattern SP2 and a

third semiconductor pattern SP3, which are sequentially stacked. The first to third semiconductor patterns SP1, SP2 and SP3 may be spaced apart from each other in a vertical direction (i.e., a third direction D3) (see FIG. 4A).

[0042] Each of the first to third semiconductor patterns SP1, SP2 and SP3 may include silicon (Si), germanium (Ge), or silicon-germanium (SiGe). For example, each of the first to third semiconductor patterns SP1, SP2 and SP3 may include crystalline silicon. Each of the first to third semiconductor patterns SP1, SP2 and SP3 may be a nanosheet.

[0043] A plurality of first source/drain patterns SD1 may be provided on the first active pattern AP1. A plurality of first recesses RS1 (Fig. 7B) may be formed on the first active pattern AP1. The first source/drain patterns SD1 may be provided in the first recesses RS1, respectively. The first source/drain patterns SD1 may be dopant regions having a first conductivity type (e.g., a p-type). The first channel pattern CH1 may be disposed between a pair of the first source/drain patterns SD1. In other words, the first to third semiconductor patterns SP1, SP2 and SP3 stacked sequentially may connect the pair of first source/drain patterns SD1 to each other.

[0044] A plurality of second source/drain patterns SD2 may be provided on the second active pattern AP2. A plurality of second recesses RS2 may be formed on the second active pattern AP2. The second source/drain patterns SD2 may be provided in the second recesses RS2, respectively. The second source/drain patterns SD2 may be dopant regions having a second conductivity type (e.g., an n-type). The second channel pattern CH2 may be disposed between a pair of the second source/drain patterns SD2. In other words, the first to third semiconductor patterns SP1, SP2 and

SP3 stacked sequentially may connect the pair of second source/drain patterns SD2 to each other.

[0045] The first and second source/drain patterns SD1 and SD2 may be epitaxial patterns formed by a selective epitaxial growth (SEG) process. For example, a top surface of each of the first and second source/drain patterns SD1 and SD2 may be located at substantially the same level as a top surface of the third semiconductor pattern SP3. In some implementations, the top surface of each of the first and second source/drain patterns SD1 and SD2 may be higher than the top surface of the third semiconductor pattern SP3.

[0046] The first source/drain patterns SD1 may include a semiconductor element (e.g., SiGe) of which a lattice constant is greater than a lattice constant of a semiconductor element of the substrate 100. Thus, the pair of first source/drain patterns SD1 may provide compressive stress to the first channel pattern CH1 therebetween. The second source/drain patterns SD2 may include the same semiconductor element (e.g., Si) as the substrate 100.

[0047] Each of the first source/drain patterns SD1 may include a buffer layer BFL and a main layer MAL on the buffer layer BFL. Referring again to FIG. 4B, the buffer layer BFL may cover an inner surface of the first recess RS1. In some embodiments, the buffer layer BFL may have a substantially uniform thickness. For example, a thickness, in the third direction D3, of the buffer layer BFL on a bottom of the first recess RS1 may be substantially equal to a thickness, in the second direction D2, of the buffer layer BFL on an inner sidewall of an upper portion of the first recess RS1.

[0048] In certain embodiments, a thickness of the buffer layer BFL may become smaller in a direction from a lower portion of the buffer layer BFL toward an upper portion of the buffer layer BFL. For example, a thickness, in the third direction D3, of the buffer layer BFL on the bottom of the first recess RS1 may be greater than a thickness, in the second direction D2, of the buffer layer BFL on the inner sidewall of the upper portion of the first recess RS1. The buffer layer BFL may have a U-shape along a profile of the first recess RS1.

[0049] The main layer MAL may fill most of a portion of a remaining region of the first recess RS1 except the buffer layer BFL. A volume of the main layer MAL may be greater than a volume of the buffer layer BFL. Each of the buffer layer BFL and the main layer MAL may include silicon-germanium (SiGe). More particularly, the buffer layer BFL may contain a relatively low concentration of germanium (Ge). In some embodiments, , the buffer layer BFL may contain more silicon (Si) than germanium (Ge). A concentration of germanium (Ge) of the buffer layer BFL may range from 0 at% to 10 at%.

[0050] The main layer MAL may contain a relatively high concentration of germanium (Ge). For example, a concentration of germanium (Ge) in the main layer MAL may range from 30 at% to 70 at%. The concentration of germanium (Ge) in the main layer MAL may increase toward the third direction D3. For example, the main layer MAL adjacent to the buffer layer BFL may have a germanium (Ge) concentration of about 40 at%, and an upper portion of the main layer MAL may have a germanium (Ge) concentration of about 60 at%.

[0051] Each of the buffer layer BFL and the main layer MAL may include dopants (e.g., boron, gallium, or indium) for allowing the first source/drain pattern SD1 to be

a p-type. A concentration of the dopants of each of the buffer layer BFL and the main layer MAL may range from 1E18 atom/cm^3 to 5E22 atom/cm^3. The concentration of the dopants in the main layer MAL may be greater than the concentration of the dopants in the buffer layer BFL.

[0052] The buffer layer BFL may prevent a stacking fault between the substrate 100 (i.e., the first active pattern AP1) and the main layer MAL and between the main layer MAL and the first to third semiconductor patterns SP1, SP2 and SP3. If a stacking fault were to occur, a channel resistance could be increased. The buffer layer BFL may protect the main layer MAL during a process of replacing second semiconductor layers SAL with first to third inner electrodes PO1, PO2 and PO3 of a gate electrode GE. For example, the buffer layer BFL may prevent an etching material used for removing the second semiconductor layers SAL from permeating into and etching the main layer MAL.

[0053] Each of the second source/drain patterns SD2 may include silicon (Si). The second source/drain pattern SD2 may further include dopants (e.g., phosphorus, arsenic, or antimony) that allow the second source/drain pattern SD2 to have an n-type conductivity. A concentration of the dopants of the second source/drain pattern SD2 may range from 1E18 atom/cm^3 to 5E22 atom/cm^3.

[0054] Gate electrodes GE may extend in the first direction D1 to intersect the first and second channel patterns CH1 and CH2. The gate electrodes GE may be arranged in the second direction D2. Each of the gate electrodes GE may vertically overlap with corresponding one(s) of the first and second channel patterns CH1 and CH2.

[0055] Referring again to FIG. 4E, the gate electrode GE may include a first inner electrode PO1 disposed between the active pattern AP1 or AP2 and the first

semiconductor pattern SP1, a second inner electrode PO2 disposed between the first semiconductor pattern SP1 and the second semiconductor pattern SP2, a third inner electrode PO3 disposed between the second semiconductor pattern SP2 and the third semiconductor pattern SP3, and an outer electrode PO4 on the third semiconductor pattern SP3.

[0056] The gate electrode GE may be provided on a top surface TS, a bottom surface BS and both sidewalls SW of each of the first to third semiconductor patterns SP1, SP2 and SP3. For example, the transistor according to the present embodiments may be a three-dimensional field effect transistor (e.g., a MBCFET or a GAAFET) in which the gate electrode GE three-dimensionally surrounds a channel.

[0057] A gate cutting pattern CT may divide the gate electrode GE into two gate electrodes GE adjacent to each other in the first direction D1. For example, the gate cutting pattern CT may be disposed between the two gate electrodes GE aligned with each other in the first direction D1. The gate cutting pattern CT may include an insulating material such as silicon oxide, silicon nitride, or a combination thereof.

[0058] Referring again to FIGS. 1, 3A, 3B and 4A to 4E, a pair of gate spacers GS may be disposed on both sidewalls of the outer electrode PO4 of the gate electrode GE, respectively. The gate spacers GS may extend along the gate electrode GE in the first direction D1. Top surfaces of the gate spacers GS may be higher than a top surface of the gate electrode GE. The top surfaces of the gate spacers GS may be coplanar with a top surface of a first interlayer insulating layer 110 to be described below. The gate spacers GS may include at least one of SiCN, SiCON, or SiN. In some implementations, each of the gate spacers GS may include a multi-layer formed of at least two of SiCN, SiCON, or SiN.

[0059] A gate capping pattern GP may be provided on the gate electrode GE. The gate capping pattern GP may extend along the gate electrode GE in the first direction D1. The gate capping pattern GP may include a material having an etch selectivity with respect to first and second interlayer insulating layers 110 and 120 to be described below. For example, the gate capping pattern GP may include at least one of SiON, SiCN, SiCON, or SiN.

[0060] A gate insulating layer GI may be disposed between the gate electrode GE and the first channel pattern CH1 and between the gate electrode GE and the second channel pattern CH2. The gate insulating layer GI may cover the top surface TS, the bottom surface BS and the both sidewalls SW of each of the first to third semiconductor patterns SP1, SP2 and SP3. The gate insulating layer GI may cover a top surface of the device isolation layer ST under the gate electrode GE.

[0061] In some embodiments, the gate insulating layer GI may include a silicon oxide layer, a silicon oxynitride layer, and/or a high-k dielectric layer. The high-k dielectric layer may include a high-k dielectric material of which a dielectric constant is higher than that of a silicon oxide layer. For example, the high-k dielectric material may include at least one of hafnium oxide, hafnium silicon oxide, hafnium zirconium oxide, hafnium tantalum oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, lithium oxide, aluminum oxide, lead scandium tantalum oxide, or lead zinc niobate.

[0062] The gate electrode GE may include a first metal pattern, and a second metal pattern on the first metal pattern. The first metal pattern may be provided on the gate insulating layer GI and may be adjacent to the first to third semiconductor patterns

SP1, SP2 and SP3. The first metal pattern may include a work function metal of adjusting a threshold voltage of a transistor. A desired threshold voltage of the transistor may be obtained by adjusting a thickness and a composition of the first metal pattern. For example, the first to third inner electrodes PO1, PO2 and PO3 of the gate electrode GE may be formed of the first metal pattern corresponding to the work function metal.

[0063] The first metal pattern may include a metal nitride layer. For example, the first metal pattern may include nitrogen (N) and at least one metal selected from a group consisting of titanium (Ti), tantalum (Ta), aluminum (Al), tungsten (W), and molybdenum (Mo). In addition, the first metal pattern may further include carbon (C). In some embodiments, the first metal pattern may include a plurality of stacked work function metal layers.

[0064] The second metal pattern may include a metal having a resistance lower than that of the first metal pattern. For example, the second metal pattern may include at least one metal selected from a group consisting of tungsten (W), aluminum (Al), titanium (Ti), and tantalum (Ta). For example, the outer electrode PO4 of the gate electrode GE may include the first metal pattern and the second metal pattern on the first metal pattern.

[0065] Referring again to FIG. 4A, inner spacers IP may be provided on the second active pattern AP2. The inner spacers IP may be disposed between the second source/drain pattern SD2 and the first to third inner electrodes PO1, PO2 and PO3 of the gate electrode GE, respectively. The inner spacers IP may be in direct contact with the second source/drain pattern SD2. Each of the first to third inner electrodes

PO1, PO2 and PO3 of the gate electrode GE may be spaced apart from the second source/drain pattern SD2 by the inner spacer IP.

[0066] A first interlayer insulating layer 110 may be provided on the first surface 100A of the substrate 100. The first interlayer insulating layer 110 may cover the gate spacers GS and the first and second source/drain patterns SD1 and SD2. A top surface of the first interlayer insulating layer 110 may be substantially coplanar with the top surface of the gate capping pattern GP and the top surface of the gate spacer GS. A second interlayer insulating layer 120 covering the gate capping pattern GP may be disposed on the first interlayer insulating layer 110. A third interlayer insulating layer 130 may be provided on the second interlayer insulating layer 120. A fourth interlayer insulating layer 140 may be provided on the third interlayer insulating layer 130. For example, each of the first to fourth interlayer insulating layers 110 to 140 may include a silicon oxide layer.

[0067] Active contacts AC may penetrate the first and second interlayer insulating layers 110 and 120 so as to be connected to the first and second source/drain patterns SD1 and SD2. Top surfaces of the active contacts AC may be substantially coplanar with a top surface of the second interlayer insulating layer 120. The active contact AC may be a self-aligned contact. In other words, the active contact AC may be formed to be self-aligned by the gate capping pattern GP and the gate spacer GS. For example, the active contact AC may cover at least a portion of a sidewall of the gate capping pattern GP.

[0068] A metal-semiconductor compound layer SC (e.g., a silicide layer) may be disposed between the active contact AC and the source/drain pattern SD1 or SD2 connected thereto. The active contact AC may be electrically connected to the

source/drain pattern SD1 or SD2 through the metal-semiconductor compound layer SC. For example, the metal-semiconductor compound layer SC may include at least one of titanium silicide, tantalum silicide, tungsten silicide, nickel silicide, or cobalt silicide.

[0069] A first via VI1 may be provided on a top surface of the active contact AC. The active contact AC may be electrically connected to one of the first and second bit lines BL1 and BL2 of the first metal layer M1, provided in the third interlayer insulating layer 130, through the first via VI1.

[0070] Dummy contacts DAC may penetrate the first and second interlayer insulating layers 110 and 120 so as to be connected to some of the first and second source/drain patterns SD1 and SD2. The first via VI1 may be omitted on the dummy contact DAC. For example, the dummy contact DAC may not be electrically connected to the first metal layer M1. In certain embodiments, at least one or all of the dummy contacts DAC may be omitted.

[0071] A gate contact GC connected to the gate electrode GE may be provided. The gate contact GC may vertically extend from the top surface of the gate electrode GE to the first metal layer M1. The gate electrode GE may be electrically connected to the word line pad WLP through the gate contact GC.

[0072] In some embodiments, the active contact AC may include a conductive pattern FM and a barrier pattern BM surrounding the conductive pattern FM. For example, the conductive pattern FM may include at least one metal of aluminum, copper, tungsten, molybdenum, or cobalt. The barrier pattern BM may cover sidewalls and a bottom surface of the conductive pattern FM. The barrier pattern BM may include a metal nitride layer, or a metal layer/a metal nitride layer. The metal

layer may include at least one of titanium, tantalum, tungsten, nickel, cobalt, or platinum. The metal nitride layer may include at least one of a titanium nitride (TiN) layer, a tantalum nitride (TaN) layer, a tungsten nitride (WN) layer, a nickel nitride (NiN) layer, a cobalt nitride (CoN) layer, or a platinum nitride (PtN) layer. In some embodiments, the gate contact GC may also include the conductive pattern FM and the barrier pattern BM.

[0073] A second metal layer M2 may be provided in the fourth interlayer insulating layer 140. The second metal layer M2 may include word lines WL extending in the first direction D1. Each of the word lines WL may be electrically connected to the word line pad WLP through a second via VI2.

[0074] Backside active contacts BAC and backside gate contacts BGC may be provided on the second surface 100B of the substrate 100. The backside active contact BAC may extend from the second surface 100B to a lower portion of the source/drain pattern SD1 or SD2 in the third direction D3. The backside active contact BAC may be connected to the source/drain pattern SD1 or SD2.

[0075] The backside gate contact BGC may extend from the second surface 100B to a lower portion of the gate electrode GE in the third direction D3. The backside gate contact BGC may be connected to the gate electrode GE. Each of the backside active contact BAC and the backside gate contact BGC may include the conductive pattern FM and the barrier pattern BM, like the active contact AC.

[0076] In some embodiments, the backside active contacts BAC may include a backside active contact BAC connected to a common source/drain of the first pull-up and first pull-down transistors TU1 and TD1. The backside gate contacts BGC may

include a backside gate contact BGC connected to a common gate of the second pull-up and second pull-down transistors TU2 and TD2.

[0077] The backside active contact BAC and the backside gate contact BGC may be merged with each other to constitute a shared contact BSC. Referring again to FIG. 4B, the gate electrode GE may be electrically connected to the first source/drain pattern SD1 adjacent thereto through the shared contact BSC. In other words, the shared contact BSC may provide an electrical connection path ECN between the gate electrode GE and the first source/drain pattern SD1. The shared contact BSC may correspond to the first node N1 or the second node N2 of FIG. 1.

[0078] According to some embodiments, the shared contact BSC may have the shape in which the backside active contact BAC and the backside gate contact BGC are merged with each other as a single metal contact, as illustrated in FIGS. 4B and 4D. According to certain embodiments, the shared contact BSC may have a shape in which the backside active contact BAC and the backside gate contact BGC are in contact with each other. In other words, an interface between the backside active contact BAC and the backside gate contact BGC may clearly exist.

[0079] The shared contact BSC may not be connected to the backside metal layer BSM to be described later. The shared contact BSC may have a L-shape when viewed in a plan view. The shared contact BSC may electrically connect the gate electrode GE and the first source/drain pattern SD1 which are adjacent to each other in the second direction D2 (see FIG. 4B). The shared contact BSC may electrically connect the first and second source/drain patterns SD1 and SD2 adjacent to each other in the first direction D1 (see FIG. 4D). In other words, the shared contact BSC

may be provided as the L-shape to electrically connect the first source/drain pattern SD1, the second source/drain pattern SD2 and the gate electrode GE to each other.

[0080] A MOL layer according to the present embodiments may include only the active contacts AC, the dummy contacts DAC and the gate contacts GC, illustrated in FIG. 3A. In other words, the shared contact BSC may be omitted in the MOL layer. Since the shared contact BSC is omitted in the MOL layer, a congestion degree of the contacts in the MOL layer may be reduced. In addition, sizes of the contacts in the MOL layer may be increased to reduce resistances in the MOL layer.

[0081] The backside metal layer BSM may be provided on the second surface 100B of the substrate 100. As described with reference to FIG. 2, the backside metal layer BSM may include the ground lines VSS and the power lines VDD, which extend in the second direction D2. A lower insulating layer LIL may be provided between the second surface 100B and the ground and power lines VSS and VDD.

[0082] Referring again to FIG. 4C, each of some of the backside active contacts BAC may be electrically connected to one of the ground and power lines VSS and VDD through a lower via BVI. The ground line VSS may be electrically connected to a corresponding one of the second source/drain patterns SD2 through a corresponding one of the backside active contacts BAC. The power line VDD may be electrically connected to a corresponding one of the first source/drain patterns SD1 through a corresponding one of the backside active contacts BAC.

[0083] A power delivery network layer PDN may be provided under the backside metal layer BSM. The power delivery network layer PDN may include a plurality of lower interconnection lines electrically connected to the ground and power lines VSS and VDD. For example, the power delivery network layer PDN may include an

interconnection network for applying a ground voltage to the ground lines VSS. The power delivery network layer PDN may include an interconnection network for applying a power voltage to the power lines VDD.

[0084] According to embodiments, power interconnection lines for supplying the ground voltage and the power voltage to the bit cells CE1 to CE4 may be disposed under the substrate 100 in the form of the power delivery network layer PDN. Thus, the power interconnection lines may be omitted in the BEOL layer including the first metal layer M1. When the power interconnection lines are omitted in the BEOL layer, a degree of congestion with interconnection lines in the BEOL layer may be reduced. In addition, sizes of the interconnection lines in the BEOL layer may be increased to reduce resistances in the BEOL layer.

[0085] FIGS. 5A to 10C are cross-sectional views illustrating a method of manufacturing a semiconductor memory device according to some embodiments . FIGS. 5A, 6A, 7A, 8A and 9A are cross-sectional views taken along the lines A-A' of FIGS. 3A and 3B. FIGS. 5B, 6B, 7B, 8B, 9B and 10A are cross-sectional views taken along the lines B-B' of FIGS. 3A and 3B. FIGS. 7C, 9C and 10B are cross-sectional views taken along the lines C-C' of FIGS. 3A and 3B. FIGS. 5C, 6C, 8C, 9D and 10C are cross-sectional views taken along the lines E-E' of FIGS. 3A and 3B.

[0086] Referring to FIGS. 5A to 5C, a substrate 100 including first to fourth bit cells CE1 to CE4 may be provided. First semiconductor layers ACL and second semiconductor layers SAL may be alternately formed on the substrate 100. The first semiconductor layers ACL may include one of silicon (Si), germanium (Ge) and silicon-germanium (SiGe), and the second semiconductor layers SAL may include another of silicon (Si), germanium (Ge) and silicon-germanium (SiGe).

[0087] The second semiconductor layer SAL may include a material having an etch selectivity with respect to the first semiconductor layer ACL. For example, the first semiconductor layers ACL may include silicon (Si), and the second semiconductor layers SAL may include silicon-germanium (SiGe). A concentration of germanium (Ge) of each of the second semiconductor layers SAL may range from 10 at% to 30 at%.

[0088] Mask patterns may be formed on the first to fourth bit cells CE1 to CE4 of the substrate 100. Each of the mask patterns may have a line shape or bar shape extending in the second direction D2.

[0089] A patterning process may be performed using the mask patterns as etch masks to form a trench TR defining first active patterns AP1 and second active patterns AP2. For example, the trench TR may be formed between the first and second active patterns AP1 and AP2. The first and second active patterns AP1 and AP2 may have bar shapes extending in the second direction D2 in parallel to each other when viewed in a plan view.

[0090] A stack pattern STP may be formed on each of the first and second active patterns AP1 and AP2. The stack pattern STP may include the first semiconductor layers ACL and the second semiconductor layers SAL, which are alternately stacked. The stack patterns STP may be formed together with the first and second active patterns AP1 and AP2 in the patterning process.

[0091] A device isolation layer ST filling the trench TR may be formed. For example, an insulating layer covering the first and second active patterns AP1 and AP2 and the stack patterns STP may be formed on an entire top surface of the

substrate 100. The insulating layer may be recessed until the stack patterns STP are exposed, thereby forming the device isolation layer ST.

[0092] The device isolation layer ST may include an insulating material (e.g., silicon oxide). The stack patterns STP may be exposed above the device isolation layer ST. In other words, the stack patterns STP may vertically protrude above the device isolation layer ST.

[0093] Referring to FIGS. 6A to 6C, sacrificial patterns PP intersecting the stack patterns STP may be formed on the substrate 100. Each of the sacrificial patterns PP may be formed to have a line shape or bar shape extending in the first direction D1.

[0094] For example, the formation of the sacrificial patterns PP may include forming a sacrificial layer on an entire top surface of the substrate 100, forming hard mask patterns MP on the sacrificial layer, and patterning the sacrificial layer using the hard mask patterns MP as etch masks. The sacrificial layer may include poly-silicon.

[0095] A pair of gate spacers GS may be formed on both sidewalls of each of the sacrificial patterns PP, respectively. The formation of the gate spacers GS may include conformally forming a gate spacer layer on an entire top surface of the substrate 100, and anisotropically etching the gate spacer layer. The gate spacer layer may include at least one of SiCN, SiCON, or SiN. In certain embodiments, the gate spacer layer may be formed of a multi-layer including at least two of SiCN, SiCON, or SiN.

[0096] Referring to FIGS. 7A to 7C, first recesses RS1 may be formed in the stack pattern STP on the first active pattern AP1. Second recesses RS2 may be formed in the stack pattern STP on the second active pattern AP2. The device isolation layer

ST at both sides of each of the first and second active patterns AP1 and AP2 may be further recessed during the formation of the first and second recesses RS1 and RS2 (see FIG. 7C).

[0097] More particularly, the stack pattern STP on the first active pattern AP1 may be etched using the hard mask patterns MP and the gate spacers GS as etch masks to form the first recesses RS1. The first recess RS1 may be formed between a pair of the sacrificial patterns PP. The second recesses RS2 in the stack pattern STP on the second active pattern AP2 may be formed by the same method as the first recesses RS1.

[0098] First to third semiconductor patterns SP1, SP2 and SP3 stacked sequentially may be formed from the first semiconductor layers ACL between the first recesses RS1 adjacent to each other. First to third semiconductor patterns SP1, SP2 and SP3 stacked sequentially may be formed from the first semiconductor layers ACL between the second recesses RS2 adjacent to each other. The first to third semiconductor patterns SP1, SP2 and SP3 between the first recesses RS1 adjacent to each other may constitute a first channel pattern CH1. The first to third semiconductor patterns SP1, SP2 and SP3 between the second recesses RS2 adjacent to each other may constitute a second channel pattern CH2.

[0099] First source/drain patterns SD1 may be formed in the first recesses RS1, respectively. For example, a first selective epitaxial growth (SEG) process may be performed using an inner surface of the first recess RS1 as a seed layer to form a buffer layer BFL. The buffer layer BFL may be grown using the first to third semiconductor patterns SP1, SP2 and SP3 and the substrate 100 exposed by the first

recess RS1 as a seed. For example, the first SEG process may include a chemical vapor deposition (CVD) process or a molecular beam epitaxy (MBE) process.

[00100] The buffer layer BFL may include a semiconductor element (e.g., SiGe) of which a lattice constant is greater than a lattice constant of a semiconductor element of the substrate 100. The buffer layer BFL may contain a relatively low concentration of germanium (Ge). In certain embodiments, the buffer layer BFL may contain silicon (Si) except germanium (Ge). A concentration of germanium (Ge) of the buffer layer BFL may range from 0 at% to 10 at%.

[00101] A second SEG process may be performed on the buffer layer BFL to form a main layer MAL. The main layer MAL may be formed to completely or almost fill the first recess RS1. The main layer MAL may contain a relatively high concentration of germanium (Ge). For example, a concentration of germanium (Ge) of the main layer MAL may range from 30 at% to 70 at%.

[00102] In some embodiments, a third SEG process may be performed on the main layer MAL to form a capping layer. The capping layer may include silicon (Si). A concentration of silicon (Si) of the capping layer may range from 98 at% to 100 at%.

[00103] Dopants (e.g., boron, gallium or indium) for allowing the first source/drain pattern SD1 to have a p-type may be injected in-situ during the formation of the buffer layer BFL and the main layer MAL. In some implementations, after the formation of the first source/drain pattern SD1, the dopants may be injected or implanted into the first source/drain pattern SD1.

[00104] Second source/drain patterns SD2 may be formed in the second recesses RS2, respectively. For example, the second source/drain pattern SD2 may be formed by performing a SEG process using an inner surface of the second recess RS2 as a seed

layer. For example, the second source/drain pattern SD2 may include the same semiconductor element (e.g., Si) as the substrate 100.

[00105] Dopants (e.g., phosphorus, arsenic or antimony) for allowing the second source/drain pattern SD2 to have an n-type may be injected in-situ during the formation of the second source/drain pattern SD2. In some implementations, after the formation of the second source/drain pattern SD2, the dopants may be injected or implanted into the second source/drain pattern SD2.

[00106] In some embodiments, before the formation of the second source/drain pattern SD2, portions of the second semiconductor layers SAL exposed by the second recess RS2 may be replaced with an insulating material to form inner spacers IP. As a result, the inner spacers IP may be formed between the second source/drain pattern SD2 and the second semiconductor layers SAL, respectively.

[00107] Referring to FIGS. 8A to 8C, a first interlayer insulating layer 110 may be formed to cover the first and second source/drain patterns SD1 and SD2, the hard mask patterns MP and the gate spacers GS. For example, the first interlayer insulating layer 110 may include a silicon oxide layer.

[00108] The first interlayer insulating layer 110 may be planarized to expose top surfaces of the sacrificial patterns PP. The planarization of the first interlayer insulating layer 110 may be performed using an etch-back process or a chemical mechanical polishing (CMP) process. The hard mask patterns MP may be completely removed during the planarization process. As a result, a top surface of the first interlayer insulating layer 110 may be substantially coplanar with the top surfaces of the sacrificial patterns PP and top surfaces of the gate spacers GS.

[00109] A region of the sacrificial pattern PP may be selectively opened using a photolithography process. For example, a region of the sacrificial pattern PP between the first and second active patterns AP1 and AP2 adjacent to each other may be selectively opened. The opened region of the sacrificial pattern PP may be selectively etched and thus may be removed. A space formed by the removal of the sacrificial pattern PP may be filled with an insulating material to form a gate cutting pattern CT (see FIG. 8C).

[00110] Remaining exposed portions of the sacrificial patterns PP may be selectively removed. Outer regions ORG exposing the first and second channel patterns CH1 and CH2 may be formed by the removal of the sacrificial patterns PP (see FIG. 8C). The removal of the sacrificial patterns PP may include performing a wet etching process using an etching solution capable of selectively etching poly-silicon.

[00111] The second semiconductor layers SAL exposed through the outer region ORG may be selectively removed to form inner regions IRG (see FIG. 8C). For example, an etching process of selectively etching the second semiconductor layers SAL may be performed to remove the second semiconductor layers SAL while leaving the first to third semiconductor patterns SP1, SP2 and SP3. The etching process may have a high etch rate with respect to silicon-germanium having a relatively high germanium concentration. For example, the etching process may have a high etch rate with respect to silicon-germanium having a germanium concentration greater than 10 at%. Meanwhile, the first source/drain pattern SD1 may be protected by the buffer layer BFL having a relatively low concentration of germanium during the etching process.

[00112] Referring again to FIG. 8C, when the second semiconductor layers SAL are selectively removed, the first to third semiconductor patterns SP1, SP2 and SP3 stacked sequentially may remain on each of the first and second active patterns AP1 and AP2. First to third inner regions IRG1, IRG2 and IRG3 may be formed by the removal of the second semiconductor layers SAL.

[00113] In detail, the first inner region IRG1 may be formed between the active pattern AP1 or AP2 and the first semiconductor pattern SP1, the second inner region IRG2 may be formed between the first semiconductor pattern SP1 and the second semiconductor pattern SP2, and the third inner region IRG3 may be formed between the second semiconductor pattern SP2 and the third semiconductor pattern SP3.

[00114] Referring to FIGS. 9A to 9D, a gate insulating layer GI may be conformally formed on the exposed first to third semiconductor patterns SP1, SP2 and SP3. A gate electrode GE may be formed on the gate insulating layer GI. The gate electrode GE may include first to third inner electrodes PO1, PO2 and PO3 formed in the first to third inner regions IRG1, IRG2 and IRG3, respectively, and an outer electrode PO4 formed in the outer region ORG.

[00115] The gate electrode GE may be recessed to reduce its height. An upper portion of the gate cutting pattern CT may also be slightly recessed during the recessing of the gate electrode GE. A gate capping pattern GP may be formed on the recessed gate electrode GE.

[00116] A second interlayer insulating layer 120 may be formed on the first interlayer insulating layer 110. The second interlayer insulating layer 120 may include a silicon oxide layer. Active contacts AC may be formed to penetrate the second interlayer insulating layer 120 and the first interlayer insulating layer 110, and the active

contacts AC may be electrically connected to the first and second source/drain patterns SD1 and SD2.

[00117] The formation of the active contact AC may include forming a barrier pattern BM, and forming a conductive pattern FM on the barrier pattern BM. The barrier pattern BM may be conformally formed and may include a metal layer/a metal nitride layer. The conductive pattern FM may include a low-resistance metal.

[00118] Referring to FIGS. 10A to 10C, a first metal layer M1 and a second metal layer M2 may be sequentially formed on the second interlayer insulating layer 120. The first metal layer M1 may include first bit lines BL1, second bit lines BL2, word line pads WLP, and dummy pads DMP. A gate contact GC connecting the word line pad WLP and the gate electrode GE may further be formed. The second metal layer M2 may include word lines WL. Even though not shown in FIGS. 10A to 10C, an additional BEOL layer may be formed on the second metal layer M2.

[00119] Backside contact holes BCH may be formed on the second surface 100B of the substrate 100. The backside contact hole BCH may penetrate a portion of the substrate 100 to vertically extend from the second surface 100B to a lower portion of the source/drain pattern SD1 or SD2. The backside contact hole BCH may expose the source/drain pattern SD1 or SD2. At least one of the backside contact holes BCH may expose the gate electrode GE as well as the source/drain pattern SD1 or SD2.

[00120] A contact spacer may be formed on an inner sidewall of each of the backside contact holes BCH. Backside active contacts BAC and backside gate contacts BGC may be formed by filling the backside contact holes BCH with a conductive material. The backside active contact BAC may be electrically connected to the source/drain pattern SD1 or SD2 (see FIG. 10B). A metal-semiconductor compound layer SC

may be formed between the backside active contact BAC and the source/drain pattern SD1 or SD2. The backside gate contact BGC may be electrically connected to the gate electrode GE (see FIG. 10C). One of the backside active contacts BAC and a corresponding one of the backside gate contacts BGC may be connected to each other to form a shared contact BSC (see FIG. 10A).

[00121] Referring again to FIGS. 4A to 4E, a lower insulating layer LIL may be formed on the second surface 100B of the substrate 100. A backside metal layer BSM may be formed on the lower insulating layer LIL. The backside metal layer BSM may include ground lines VSS and power lines VDD. Each of the ground lines VSS and the power lines VDD may be electrically connected to a corresponding one of the backside active contacts BAC through a lower via BVI.

[00122] A power delivery network layer PDN may be formed on the backside metal layer BSM. The power delivery network layer PDN may be formed to apply a ground voltage to the ground lines VSS. The power delivery network layer PDN may be formed to apply a power voltage to the power lines VDD.

[00123] Hereinafter, various embodiments will be described. In the following embodiments, the descriptions to the same technical features as mentioned with reference to FIGS. 3A, 3B and 4A to 4E will not be repeated and differences between the following embodiments and the embodiments of FIGS. 3A, 3B and 4A to 4E will be mainly described, for the purpose of ease and convenience in explanation. FIGS. 11 to 15 are cross-sectional views illustrating semiconductor memory devices according to some embodiments.

[00124] FIG. 11 is a cross-sectional view taken along the lines A-A’ of FIGS. 3A and 3B. Referring to FIG. 11, a second metal layer M2 may further include bit line pads

BLP. Each of the bit line pads BLP may be provided between the word lines WL adjacent to each other. The bit line pad BLP may have an island shape.

[00125] A third metal layer M3 provided on the second metal layer M2 may include upper bit lines UBL. For example, the upper bit lines UBL may include a first upper bit line UBL1 vertically overlapping with the first bit line BL1. The first upper bit line UBL1 may extend in the second direction D2 in parallel to the first bit line BL1. The bit line pads BLP may be arranged in the second direction D2 between the first upper bit line UBL1 and the first bit line BL1.

[00126] The first bit line BL1 may be electrically connected to the first upper bit line UBL1 through second vias VI2, the bit line pads BLP and third vias VI3. Thus, a signal may flow through the first upper bit line UBL1 as well as the first bit line BL1. The signal may flow through two paths (i.e., the first bit line BL1 and the first upper bit line UBL1), and thus a resistance may be reduced. As a result, a speed and electrical characteristics of a semiconductor memory device may be improved.

[00127] FIG. 12 is a cross-sectional view taken along the lines B-B' of FIGS. 3A and 3B. Referring to FIG. 12, the backside gate contact BGC of the shared contact BSC may have a first top surface TOS1, and the backside active contact BAC of the shared contact BSC may have a second top surface TOS2. A level LV1 of the first top surface TOS1 may be different from a level LV2 of the second top surface TOS2. In some embodiments, the level LV1 of the first top surface TOS1 may be higher than the level LV2 of the second top surface TOS2. In certain embodiments, the level LV1 of the first top surface TOS1 may be lower than the level LV2 of the second top surface TOS2.

[00128] FIG. 13 is a cross-sectional view taken along the lines E-E' of FIGS. 3A and 3B. Referring to FIG. 13, the first channel pattern CH1 may have a first width WI1 in the first direction D1. The second channel pattern CH2 may have a second width WI2 in the first direction D1. The first width WI1 may be different from the second width WI2. In some embodiments, the second width WI2 may be greater than the first width WI1. In other words, a size of the channel of the NMOSFET may be greater than a size of the channel of the PMOSFET, and thus driving force of the NMOSFET may be greater than driving force of the PMOSFET.

[00129] FIG. 14 is a cross-sectional view taken along the lines E-E' of FIGS. 3A and 3B. Referring to FIG. 14, a second channel pattern CH2 may further include a fourth semiconductor pattern SP4 in addition to the stacked first to third semiconductor patterns SP1, SP2 and SP3. In other words, the number of nanosheets of the NMOSFET may be greater than the number of nanosheets of the PMOSFET. Thus, the driving force of the NMOSFET may be greater than the driving force of the PMOSFET. Even though not shown in the drawings, as described above with reference to FIG. 13, a width of the nanosheet of the NMOSFET and the number of the nanosheets of the NMOSFET may be greater than a width of the nanosheet of the PMOSFET and the number of the nanosheets of the PMOSFET, respectively.

[00130] FIG. 15 is a cross-sectional view taken along the lines E-E' of FIGS. 3A and 3B. Referring to FIG. 15, each of upper portions of first and second active patterns AP1 and AP2 may have a fin shape vertically protruding above the device isolation layer ST. In other words, each of the first and second active patterns AP1 and AP2 may be an active fin. A gate electrode GE may be provided on a top surface TS and both sidewalls SW of each of first and second channel patterns CH1 and CH2. A

transistor according to the present embodiments may be a three-dimensional field effect transistor (e.g., a FinFET) in which a gate electrode three-dimensionally surrounds a channel.

[00131] FIG. 16A is a plan view of a first surface of a substrate to illustrate a semiconductor memory device according to some embodiments. FIG. 16B is a plan view of a second surface of the substrate to illustrate a semiconductor memory device according to some embodiments.

[00132] Referring to FIGS. 16A and 16B, a read buffer RB adjacent to a bit cell CE in the first direction D1 may further be provided. The read buffer RB may include an NMOSFET. For example, the read buffer RB may include a second active pattern AP2. A width of the second active pattern AP2 of the read buffer RB may be equal to or greater than a width of the second active pattern AP2 of the bit cell CE.

[00133] A first metal layer M1 may further include a read bit line RBL and a read word line pad RWLP, which are provided on the read buffer RB. A gate electrode GE on the read buffer RB may be electrically connected to the read word line pad RWLP through a gate contact GC. A second source/drain pattern SD2 of the read buffer RB may be electrically connected to the read bit line RBL through an active contact AC. Another second source/drain pattern SD2 of the read buffer RB may be electrically connected to the ground line VSS through a backside active contact BAC.

[00134] A SRAM cell according to the present embodiments may include the bit cell CE having six transistors (6T), and the read buffer RB having two transistors (2T). In other words, the SRAM cell of the present embodiments may be an 8T SRAM cell. The backside contacts BAC and BGC and the backside metal layer BSM may also be applied to the 8T SRAM cell.

[00135] According to embodiments, the node of the SRAM cell may include the shared contact provided from the back surface (or backside) of the substrate. Thus, the congestion degree of the MOL layer of the SRAM cell may be reduced and the sizes of the contacts in the MOL layer may be increased, thereby reducing the resistances in the MOL layer. The ground line and the power line of the SRAM cell may be provided in a backside interconnection layer. Thus, the congestion degree of the BEOL layer may be reduced and the sizes of the interconnection lines in the BEOL layer may be increased, thereby reducing the resistances in the BEOL layer. As a result, the electrical characteristics of the semiconductor memory device according to embodiments may be improved.

[00136] By way of summation and review, embodiments may provide a semiconductor memory device with improved electrical characteristics.

[00137] Embodiments may also provide a method of manufacturing the semiconductor memory device with improved electrical characteristics.

[00138] Example embodiments have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. In some instances, as would be apparent to one of ordinary skill in the art as of the filing of the present application, features, characteristics, and/or elements described in connection with a particular embodiment may be used singly or in combination with features, characteristics, and/or elements described in connection with other embodiments unless otherwise specifically indicated. Accordingly, it will be understood by those of skill in the art that various changes in form and details may be made without departing from the spirit and scope of the present invention as set forth in the following claims.

WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a substrate including a first surface and a second surface opposite to the first surface;

a first active pattern on the first surface;

a first channel pattern on the first active pattern and a first source/drain pattern connected to the first channel pattern;

a gate electrode provided on the first channel pattern and extending in a first direction, the gate electrode being adjacent to the first source/drain pattern in a second direction intersecting the first direction;

a shared contact provided under the first source/drain pattern and the gate electrode and electrically connecting the first source/drain pattern and the gate electrode to each other; and

a backside metal layer on the second surface.

2. The semiconductor memory device as claimed in claim 1, wherein the shared contact vertically extends from the second surface to the first source/drain pattern and the gate electrode.

3. The semiconductor memory device as claimed in claim 1 or claim 2, wherein:

the shared contact includes a backside gate contact connected to the gate electrode, and a backside active contact connected to the first source/drain pattern,

the backside gate contact has a first top surface,

the backside active contact has a second top surface, and

a level of the first top surface is different from a level of the second top surface.

4. The semiconductor memory device as claimed in any one of claims 1 to 3, wherein a bottom surface of the shared contact is substantially coplanar with the second surface.

5. The semiconductor memory device as claimed in claim 1 or claim 2, further comprising:

a second active pattern on the first surface;

a second source/drain pattern on the second active pattern; and

a backside active contact provided under the second source/drain pattern and connected to the second source/drain pattern,

wherein the backside active contact is electrically connected to a ground line of the backside metal layer.

6. The semiconductor memory device as claimed in any one of claims 1 to 4, further comprising:

a second active pattern on the first surface;

a second channel pattern on the second active pattern and a second source/drain pattern connected to the second channel pattern;

an active contact provided on the second source/drain pattern and connected to the second source/drain pattern; and

a first metal layer on the active contact,

wherein the first metal layer includes a first bit line, a second bit line, and a word line pad, and

the active contact is electrically connected to one of the first and second bit lines.

7. The semiconductor memory device as claimed in claim 6, wherein the first metal layer further includes a dummy pad.

8. The semiconductor memory device as claimed in claim 6 or claim 7, further comprising:

a second metal layer and a third metal layer that are sequentially stacked on the first metal layer, wherein:

the second metal layer includes word lines and a bit line pad between the word lines,

the third metal layer includes an upper bit line, and

the one of the first and second bit lines is electrically connected to the upper bit line through the bit line pad.

9. The semiconductor memory device as claimed in any one of claims 6 to 8, wherein each of the first and second channel patterns includes semiconductor patterns stacked sequentially, and

wherein a width of each of the semiconductor patterns of the second channel pattern is greater than a width of each of the semiconductor patterns of the first channel pattern.

10. The semiconductor memory device as claimed in any one of claims 6 to 8, wherein each of the first and second channel patterns includes semiconductor patterns stacked sequentially, and

a number of the semiconductor patterns of the second channel pattern is greater than a number of the semiconductor patterns of the first channel pattern.

11. A semiconductor memory device comprising:

a SRAM cell on a substrate,

wherein the SRAM cell includes:

first pull-up/down transistors and second pull-up/down transistors; and

a first node connecting a common source/drain of the first pull-up/down transistors to a common gate of the second pull-up/down transistors,

wherein the first node includes a shared contact connected to the common source/drain and the common gate, the shared contact electrically connecting the common source/drain and the common gate to each other,

the shared contact is buried in a lower portion of the substrate, and

the shared contact includes a backside active contact electrically connected to the common source/drain, and a backside gate contact electrically connected to the common gate.

12. The semiconductor memory device as claimed in claim 11, wherein:

the backside active contact vertically extends from a back surface of the substrate to the common source/drain, and

the backside gate contact vertically extends from the back surface of the substrate to the common gate.

13. The semiconductor memory device as claimed in claim 11, wherein a bottom surface of the shared contact is substantially coplanar with a back surface of the substrate.

14. The semiconductor memory device as claimed in any one of claims 11 to 13, wherein:

the backside gate contact has a first top surface,

the backside active contact has a second top surface, and

a level of the first top surface is different from a level of the second top surface.

15. The semiconductor memory device as claimed in claim 11, further comprising:

a first metal layer on a front surface of the substrate;

a second metal layer on the first metal layer; and

a backside metal layer on a back surface of the substrate,

wherein the SRAM cell further includes:

a first bit line and a second bit line in the first metal layer;

a word line in the second metal layer; and

a ground line and a power line in the backside metal layer.

16. A semiconductor memory device comprising:

a substrate including a bit cell region;

a first active pattern and a second active pattern on the bit cell region, the first active pattern being spaced apart from the second active pattern in a first direction;

a device isolation layer filling a trench between the first and second active patterns;

a first channel pattern on the first active pattern and a first source/drain pattern connected to the first channel pattern;

a second channel pattern on the second active pattern and a second source/drain pattern connected to the second channel pattern;

a gate electrode provided on the first channel pattern and extending in the first direction;

a gate insulating layer between the gate electrode and the first channel pattern;

a gate spacer on at least one sidewall of the gate electrode;

a gate capping pattern on the gate electrode;

an interlayer insulating layer on the gate capping pattern;

an active contact penetrating the interlayer insulating layer so as to be connected to the second source/drain pattern;

a first metal layer on the interlayer insulating layer, the first metal layer including a bit line electrically connected to the active contact; and

a shared contact provided under the first source/drain pattern and the gate electrode and electrically connecting the first source/drain pattern and the gate electrode to each other.

17. The semiconductor memory device as claimed in claim 16, further comprising:

metal-semiconductor compound layers provided between the shared contact and the first source/drain pattern and between the active contact and the second source/drain pattern, respectively.

18. The semiconductor memory device as claimed in claim 16 or claim 17, further comprising:

a backside metal layer provided on a back surface of the substrate,

wherein the backside metal layer includes a ground line and a power line.

19. The semiconductor memory device as claimed in any one of claims 16 to 18, further including:

a second metal layer on the first metal layer,

wherein the second metal layer includes a word line.

20. The semiconductor memory device as claimed in any one of claims 16 to 19, wherein:

the shared contact includes a backside gate contact connected to the gate electrode, and a backside active contact connected to the first source/drain pattern,

the backside gate contact has a first top surface,

the backside active contact has a second top surface, and

a level of the first top surface is different from a level of the second top surface.