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(54) Title: METHOD FOR WRAPPED-GATE MOSFET

(57) **Abstract:** A wrapped-gate transistor includes a substrate having an upper surface and first and second side surfaces opposing to each other. Source and drain regions are formed in the substrate with a channel region therebetween. The channel region extends from the first side surface to the second side surfaces of the substrate. A gate dielectric layer is formed on the substrate. A gate electrode is formed on the gate dielectric layer to cover the channel region from the upper surface and the first and second side surfaces with the gate dielectric therebetween. The substrate is a silicon island formed on an insulation layer of an SOI (silicon-on-insulator) substrate or one a conventional non-SOI substrate, and has four side surfaces includes the first and second side surfaces. The source and drain regions are formed on the portions of the substrate adjoining the third and fourth surfaces which are perpendicular to the first and second side surfaces. The wrapped-gate structure provides a better and quicker potential control within the channel area, which yields steep sub-threshold slope and low sensitivity to the "body-to-source" voltage.



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