ABSTRACT OF THE DISCLOSURE

STACKED CONTAINER CAPACITOR USING CHEMICAL MECHANICAL POLISHING

A method for forming a stacked container capacitor for use within integrated circuits. Formed successively upon a semiconductor substrate is a first dielectric layer, a second dielectric layer and a patterned mask layer. Within an isotropic etch process, the first dielectric layer etches slower than the second dielectric layer. By means of an anisotropic etch process employing the patterned mask layer as a mask, an aperture is etched at least partially through the first dielectric layer. By means of an isotropic etch process employing the patterned mask layer as a mask, the second dielectric layer is etched to yield a ledge formed above the first dielectric layer and below the patterned masking layer. The patterned mask layer is then removed. Formed then into the anisotropically and isotropically etched aperture is a first polysilicon layer, a third dielectric layer and a second polysilicon layer. Finally, the filled isotropically etched aperture is planarized until there is exposed a flange of the first polysilicon layer formed into the ledge.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)