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INDUCTIVELY COUPLED PLASMA REACTOR AND PROCESS

Field of the Invention

This invention relates in general to a plasma process technology, and more particularly, to inductively coupled plasma systems and to associated etching and deposition processes.

Background of the Invention

As semiconductor device technology grows in complexity, more and more device functions are incorporated into smaller and smaller device geometries. Device manufacturers require sophisticated processing apparatus to meet the demands for high precision device ulta-large-scale-integrated (ULSI) device fabrication. However, processing costs correspondingly increase with the complexity of the processing equipment, and the equipment becomes more expensive to purchase and to maintain. To address the increased production costs, manufacturers increase the size of semiconductor substrates upon which integrated circuit devices are formed. By increasing the substrate size the unit cost of production can be reduced. Today, semiconductor wafers having diameters of 8" or more are common in state-of-the-art fabrication facilities. While the increased wafer diameters have enabled manufacturers to fabricate large numbers of devices on a single substrate, great difficulty can be experienced controlling the uniformity of fabrication processes applied to large diameter semiconductor wafers.

In the plasma etching process, many factors can impact the uniformity of etching a material layer deposited on the surface of a semiconductor wafer. These factors include the plasma uniformity, the ion flux uniformity at the wafer surface, the reactant gas supply to the etching system, and the removal of reaction products across the surface of the wafer. Traditional plasma etching reactors are designed primarily with one power source, in which to create the plasma, and one injection point to introduce process gases. By limiting the system to a single power source and gas supply, the etching systems ability to optimize the etch rate uniformity of the process across a large diameter wafer is very minimal.

For example, there is virtually no way in which to spatially vary the etching process across the surface of the semiconductor wafer. Additionally, plasma etching systems are typically provided with a processing chamber having a fixed arrangement of components. Because the chamber design can effect the etching characteristics of specific thin-film materials commonly used in semiconductor fabrication, the particular chamber arrangement dictates that the etching system must be limited to etching only one type or only a few different types of material.

Advanced etching technology, such as electron-cyclotron-resonance (ECR) etching and inductively-coupled-plasma (ICP) etching has been developed to etch semiconductor devices having extremely small feature sizes. These systems operate at much lower pressure than diode systems yet are capable of generating a high density plasma. Systems such as ECR and ICP etching systems also offer an advantage over conventional diode etching systems by eliminating the exposure of the semiconductor substrate to high electrical fields. By decoupling the substrate from the plasma generating elements of the reactor, ion transport efficiency and ion anisotropy can be enhanced yielding greater process control.

In plasma deposition technology, similar uniformity limitations exist as wafer diameters increase. Better deposition uniformity is usually achieved at extremely low operating pressure. However, at low pressure, high density plasmas are required to deposit a thin-film layer on a large diameter substrate having a uniform thickness.

At present, neither plasma etching systems nor plasma deposition systems offer any means of spatially varying the plasma to address etching and deposition uniformity with large diameter semiconductor substrates. Accordingly, further development of reactor design and etching process technology is necessary to uniformly etch material layers overlying large diameter semiconductor wafers.

Summary of the Invention

In practicing the present invention there is provided an inductively coupled plasma reactor and a process for either etching or depositing a material layer using the inductively coupled plasma reactor. The plasma reactor of the invention contains a coaxial multiple coil plasma source

mounted within a reaction chamber. The plasma source is in spaced relationship with a chuck configured for accepting and supporting a semiconductor wafer thereon. The plasma source includes a plurality of channels, each channel having an independently controlled gas supply and an independently controlled RF coil surrounding the channel.

In operation, a semiconductor wafer is placed on the chuck and a gas control system is actuated to charge the reactor with plasma-forming gas. RF power is applied to the independent RF coils and the plasma is ignited within the chamber. The material layer is etched while controlling the etching uniformity by adjusting the RF power and frequency in the coil surrounding each channel, and the gas flow rate and the gas composition emerging from each of the channel within the plasma source. In the same manner, a material layer is deposited onto a substrate while spatially controlling the plasma density and composition. Highly precise and uniform etching and deposition is obtained by independently controlling the plasma density and composition in correspondence with the radial distance along the surface of a semiconductor wafer.

Brief Description of the Drawings

FIG. 1 is a schematic diagram of an inductively coupled plasma reactor arranged in accordance with one embodiment of the invention;

FIG. 2 illustrates, in cross-section, a portion of a plasma source arranged in accordance with the invention;

FIG. 3 illustrates a top view of a gas plenum suitable for delivery of process gases to the plasma source of the invention;

FIG. 4 illustrates, in cross-section, an alternate embodiment of a plasma source used in the inductively coupled plasma reactor illustrated in FIG. 1;

FIG. 5 illustrates in cross-section, a further embodiment of a plasma source suitable for use in the inductively coupled plasma reactor shown in FIG. 1;

FIG. 6 illustrates a top view of a generalized depiction of a semiconductor wafer; and

FIG. 7 illustrates, in cross-section, a portion of a semiconductor wafer having an overlying material layer to be etched in the inductively coupled plasma reactor of the invention.

It will be appreciated that for simplicity and clarity of illustration, elements shown in the FIGURES have not necessarily been drawn to scale. For example, the dimensions of some of the elements are exaggerated relative to each other. Further, where considered appropriate, reference numerals have been repeated among the FIGURES to indicate corresponding elements.

Detailed Description of Preferred Embodiments

The present invention is for an inductively coupled plasma reactor in which the plasma density and composition can be spatially varied within the plasma reactor. To achieve a spatial variance in the plasma density and composition, a coaxial multiple coil inductive plasma source is provided having a variable number of recessed channels. Each channel is surrounded by an independently powered RF coil and contains a process gas orifice. Gas control mechanisms are provided such that the process gas flow rate and composition can be independently varied in each channel within the plasma source.

The present invention also contemplates a process in which a material layer is deposited or etched. In the etching process, the semiconductor wafer is placed on a chuck mounted within the plasma reaction chamber. The chuck is mounted in spaced relationship with the plasma source, such that the center of the semiconductor wafer is opposite the central channel in the plasma source. By positioning the semiconductor wafer relative to the channel configuration of the plasma source, the variable plasma density and composition generated by the plasma source results in localized control of the etch rate across the semiconductor wafer. Thus, the etch rate of a material layer overlying a semiconductor wafer can be independently varied across the diameter of the semiconductor wafer.

In the deposition process, the semiconductor wafer is positioned on the chuck, and a material layer is deposited onto the semiconductor wafer. The positional correspondence with the plasma source enables a

uniformly thick material layer to be deposited by varying the plasma density and composition across the diameter of the semiconductor wafer.

Through the localized control of process gas flow rate and composition, together with the localized control of RF power density and frequency, the inductively coupled plasma reactor of the invention permits an enhanced degree of process parameter control during an etching process. Furthermore, the inventive reactor and process provide a means for high precision control of etch rates or deposition thickness of material layers overlying substrates of large diameter. Accordingly, semiconductor wafers having large diameters can be uniformly processed through the localized plasma density control provided by the present invention.

Shown in FIG. 1 is an ICP reactor 10. Inductively coupled plasma reactor 10 includes a processing chamber 12 housing a chuck 14. A plasma source 16 resides in an upper portion of processing chamber 12 in opposed spatial relationship to chuck 14. Processing chamber 12 is supplied with RF power from an RF power supply system 18. As will subsequently be described, RF power supply system 18 contains a plurality of independent RF power supply generators each capable of operating at an independent power level and frequency. Processing chamber 12 is also supplied with processing gases from a gas supply system 20. As will subsequently be described, gas supply system 20 is capable of supplying processing gas to processing chamber 12 in multiple independent gas feed lines. Vacuum pressure within processing chamber 12 is controlled by vacuum system 22. Reaction products and processing gases are withdrawn from processing chamber 12 through vacuum panel 24, which in a preferred arrangement, resides in processing chamber 12 below chuck 14 and coupled to vacuum line 26. Those skilled in the art will appreciate that other processing chamber designs are possible and that different vacuum port arrangements are possible. In addition, temperature control of chuck 14 can be provided by a cooling system (not shown). Either liquid or gas coolant can be transported through cooling channels embedded in chuck 14.

In operation, a semiconductor wafer 28 is placed on chuck 14 and processing gases are introduced into processing chamber 12 from gas supply system 20. A desired vacuum pressure is obtained within processing chamber 12 by vacuum system 22 and RF power is applied from

RF power supply system 18 igniting a plasma 30. In the case of plasma etching, the bombardment energy of ionized species within plasma 30 upon semiconductor wafer 28 is further controlled by applying an RF bias to chuck 14 from RF bias power supply 32.

As depicted in FIG. 1, plasma source 16 contains numerous channels with each channel supplied by independent gas feed lines 34, 35, and 36. FIG. 2 illustrates a portion of plasma source 16 in exploded cross-sectional view. Gas feed line 36 supplies central channel 38 through an inner gas plenum 40. A gas orifice 42 provides communication between central channel 38 and inner gas plenum 40. Similarly, gas feed line 35 supplies processing gases to first channel 44 through an outer gas plenum 46.

Processing gases are distributed to central channel 38 and first channel 44 through a circular plenum cap 48, shown in top view in FIG. 3. Plenum cap 50 houses inner gas plenum 40 distributing gas to central channel 38. Correspondingly, plenum cap 52 distributes gas to outer gas plenum 46. Gas feed line 36 is attached to plenum cap 50 in a central portion thereof. Gas feed line 35 can be attached to plenum cap 52 at numerous sites, as illustrated in FIG. 3. Similarly, gas orifice 43 is provided at numerous locations around the circular geometry of first channel 44.

As illustrated in FIGs. 2 and 3, first channel 44 is concentric about central channel 38. In one embodiment of the present invention, additional channels within plasma source 16 are also concentrically arranged about central channel 38 and first channel 44. For example, the outer most channel illustrated in FIG. 1 is concentric about first channel 44. By successive concentric arrangement, numerous channels can be configured within plasma source 16 depending upon the desired degree spatial control of plasma 30.

As illustrated in FIG. 2, a central RF coil 54 surrounds central channel 38. Additionally, a first RF coil 56 surrounds first channel 44. Both central RF coil 54 and first RF coil 56 are independently controlled by RF power supply system 18. Each RF coil can supply an independent power level and RF frequency to the processing gases within the enclosed channel. RF coils 54 and 56 are separated from the processing gases within each channel by a dielectric housing 58. Electrical current traversing the RF coils inductively couples with processing gas species to ignite a plasma

within each channel. Those skilled in the art will recognize that by independently powering each RF coil and by independently supplying each channel with processing gases that the plasma density and composition can be independently adjusted in each channel within plasma source 16.

Although the concentric channel design of plasma source 16 provides a substantial degree of control by which the plasma density and composition can be locally varied, additional embodiments of an ICP reactor designed in accordance with the invention are illustrated in FIGs. 4 and 5. The plasma conditions experienced by semiconductor wafer 28 can be further controlled by varying the separation distance between portions of plasma source 16 and the surface of semiconductor wafer 28. As illustrated in FIG. 4, central channel 38 is in close proximity to semiconductor wafer 28, while first channel 44 is vertically separated from semiconductor wafer 28.

An alternate configuration is illustrated in FIG. 5. In this embodiment of the invention, central channel 38 is vertically separated from semiconductor wafer 28 a greater distance than first channel 44. By varying the vertical separation distance between components of plasma source 16 and the semiconductor wafer being etched, an additional degree of control is provided for varying the plasma conditions across the surface of the semiconductor wafer. Furthermore, the variable plasma conditions can be combined with varying degrees of RF bias applied to chuck 14 to enable even more precise control of ion bombardment upon semiconductor wafer 28.

In a further embodiment of the invention, RF shields are positioned outside of each coil in plasma source 16. As illustrated in FIG. 5, a central RF shield 60 surrounds central RF coil 54, and a first RF shield 62 surrounds first RF coil 56. RF shields 60 and 62 minimize the RF interference between the independently powered coils in plasma source 16. The RF shields can be constructed from a conductive material such as aluminum, or alternatively a high-permeability, ferromagnetic material, such as a ferrite material.

Through the selection of proper materials of construction, RF shields 60 and 62 can enhance the magnetic field within each channel by confining the magnetic field to the immediate region of the RF coils that

they surround. Although shields 60 and 62 are depicted in the particular ICP reactor embodiment illustrated in FIG. 5, those skilled in the art will appreciate that shields 60 and 62 can be similarly incorporated into any of the plasma source configurations contemplated by the present invention.

The process control capability of the ICP reactor of the invention as applied to the etching of a material layer on a semiconductor substrate will now be described. Shown in FIG. 6, in top view, is a generalized depiction of semiconductor wafer 28. Semiconductor wafer 28 has a generally circular geometry characterized by a radius "R" and by a perimeter "P." Semiconductor wafer 28 can be further characterized by a plurality of locations 64 positioned on the surface of semiconductor wafer 28 and specified by a radial distance. The radial distance varies from zero to the radial distance of perimeter P.

FIG. 7 illustrates, in cross-section, a portion of semiconductor wafer 28. A material layer 66 overlies the surface of semiconductor wafer 28. The process of the present invention contemplates the removal of many different kinds of materials commonly used in the fabrication of integrated circuit devices. For example, material layer 66 can be a semiconductor material, such as polycrystalline silicon, or a refractory metal silicide, or the like. Additionally, material layer 66 can be a conductive material, such as aluminum, aluminum alloyed with silicon, aluminum alloyed with silicon and copper, elemental copper, and the like. Furthermore, material layer 66 can be a dielectric material, such as silicon dioxide, silicon nitride, silicon oxynitride, boron oxynitride, and the like.

In practicing the present invention, where material layer 66 is a semiconductor material, halogen and halogenated processing gases, such as chlorine, hydrogen chloride, chlorinated halocarbons, fluorine and fluorinated compounds, chlorofluorocarbons, bromine, hydrogen bromide , iodine, hydrogen iodide, and the like, and mixtures thereof can be used to etch the material. Also, where material layer 66 is a dielectric material, fluorine, hydrogen fluoride, fluorinated halocarbons, and the like, and mixtures thereof, can be used to etch the material. Where material layer 66 is a conductive material, processing gases can include fluorinated compounds together with chlorine and chlorinated boron compounds.

To carry out the etching of material layer 66, semiconductor wafer 28 is positioned on chuck 14 of ICP reactor 10 in such a manner that the center point, denoted "C" in FIGs. 6 and 7, is approximately vertically aligned with central channel 38 in plasma source 16. Upon the positional alignment of semiconductor wafer 28 with the concentric channels of plasma source 16, the localized etch rate at location 64 across semiconductor substrate 28 can be independently controlled by the spatially variant plasma conditions generated by plasma source 16. In this manner, radial control of the etch rate of material layer 66 is attained, such that material layer 66 in proximity to the perimeter P is etched simultaneously with portions of material layer 66 at center point C, and at the various location 64 across semiconductor wafer 28.

In the case of plasma deposition, a material layer, such as material layer 66, is deposited onto semiconductor wafer 28. For deposition, processing gases are introduced into processing chamber 12 from gas supply system 20 that will undergo a plasma induced reaction and form a thin-film layer on semiconductor wafer 28. For example, where a semiconductor material, such as polycrystalline silicon is to be deposited, a silicon-containing gas, such as silane, or halogenated silane, such as dichlorosilane, is introduced. Where a dielectric material, such as silicon dioxide or silicon nitride is to be deposited, a processing gas such as tetraethylorthosilane (TEOS), halogenated silane and ammonia, and the like, can be introduced. Furthermore, a refractory metal, or a refractory metal silicide material, and the like can be deposited by introducing a refractory-metal-containing gas.

Those skilled in the art will appreciate that the foregoing is only a representative description of many different processing gases that can be utilized by the present invention to either etch or deposit a material layer in ICP reactor 10. The present invention contemplates the deposition and etching of any and all materials capable of being formed in an ICP reactor.

To carry out the deposition of material layer 66, semiconductor wafer 28 is positioned on chuck 14 of ICP reactor 10 in such a manner that the center point, denoted "C" in FIGs. 6 and 7, is approximately vertically aligned with central channel 38 in plasma source 16. Upon the positional alignment of semiconductor wafer 28 with the concentric channels of plasma source 16, the localized deposition rate at locations 64 across

semiconductor substrate 28 can be independently controlled by the spatially variant plasma conditions generated by plasma source 16. In this manner, radial control of the deposition rate of material layer 66 is attained, such that portions of material layer 66 in proximity to the perimeter P are formed simultaneously with portions of material layer 66 at center point C, and at the various location 64 across semiconductor wafer 28.

It is believed that one of skill in the art, can without further elaboration, practice the present invention and fully realize the operational advantages of the present invention. Accordingly, the following examples are intended to be merely illustrative of the invention, and to not limit the invention in any way whatsoever.

EXAMPLE I

Semiconductor substrate 28 is first subjected to a chemical vapor deposition process to deposit a material layer 66 thereon. Semiconductor substrate 28 is then placed on chuck 14 in ICP reactor 10. Processing gas is selected depending upon the composition of the material layer to be etched. For example, where material layer 66 is polycrystalline silicon, halogen gases, such as chlorine, and hydrogenated halogen gases, such as hydrogen chloride and hydrogen bromide, are introduced together with an inert gas diluent. The total gas flow from gas supply system 20 is adjusted to a value of between 40 and 200 sccm and vacuum system 22 is adjusted to achieve a processing pressure of about 1 to 10 millitorr in processing chamber 12. RF power is then applied from RF power supply system 18 to RF coils 54 and 56 in plasma source 16. Preferably, about 100 to 5000 watts RF is applied to RF coils 54 and 56. Further, about 0 to 5000 watts RF is applied to chuck 14 from RF bias power supply 32. The plasma etching of the material layer is then carried out to completion.

EXAMPLE II

Semiconductor substrate 28 is placed on chuck 14 in ICP reactor 10. Processing gas is selected depending upon the composition of the material layer to deposited. For example, where material layer 66 is epitaxial

silicon, hydrogen and silane are introduced in processing chamber 12 at about a 3:1 flow ratio. The total gas flow from gas supply system 20 is adjusted to a value of about 40 sccm and vacuum system 22 is adjusted to achieve a processing pressure of about 1 to 25 millitorr in processing chamber 12. RF power is then applied from RF power supply system 18 to RF coils 54 and 56 in plasma source 16. Preferably, about 500 to 1500 watts RF is applied to RF coils 54 and 56 at a frequency of about 13.56MHz. Further, about 0 to -60 volts DC is applied to chuck 14 while maintaining chuck 14 at a temperature of about 400 to 700°C. The plasma deposition of the material layer is then carried out to completion.

Thus it is apparent that there has been provided, in accordance with the invention, an inductively coupled plasma reactor and a process for etching a material layer, which fully meet the advantages set forth above. Although the invention has been described and illustrated with reference to specific illustrative embodiments thereof, it is not intended that the invention be limited to those illustrative embodiments. Those skilled in the art will recognize that variations and modifications can be made without departing from the spirit of the invention. For example, the present invention contemplates the etching of material layers having a lithographic pattern previously defined for the purpose of creating various device structures, such as gate electrodes, electrical contacts, electrical interconnects, and the like. Furthermore, the invention contemplates the use of many different kinds of chemical agents for the deposition or etching of a wide variety of materials used to form thin-film layers in semiconductor devices. It is therefore intended to include within the invention all such variations and modifications as fall within the scope of the appended claims and equivalents thereof.

Claims

We claim:

1. A process for fabricating a semiconductor device comprising the steps of:

providing a plasma reactor , the plasma reactor having a first plasma generation region and a second plasma generation region, the first plasma generation region having a perimeter wherein the second plasma generation region surrounds the perimeter of the first plasma generation region;

placing a semiconductor substrate within the plasma reactor ;

using the first plasma generation region and the second plasma generation region to generate a plasma within the plasma reactor ; and

processing the semiconductor substrate in the plasma reactor using the plasma.

2. The process of claim 1, wherein the step of providing the plasma reactor is further characterized as providing an inductively coupled plasma reactor.

3. The process of claim 1, wherein the step of providing the plasma reactor the first plasma generation region and the second plasma generation region are further characterized as being concentric.

4. The process of claim 1, wherein the step of providing the plasma reactor comprises providing a plasma reactor wherein the first plasma generation region is further characterized as comprising a first channel region surrounded by a first coil and the second plasma generation region is further characterized as comprising a second channel region surrounded by a second coil.

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5. The process of claim 1, wherein the step of providing the plasma reactor comprises providing a plasma reactor wherein the first plasma generation region is further characterized as having a first gas supply and the second plasma generation region is further characterized as having second gas supply, wherein the first gas supply has a first gas flow rate and a first gas composition and the second gas supply has a second gas flow rate and a second gas composition.

6. The process of claim 5, wherein the step of processing the semiconductor substrate the first gas flow rate is not equal to the second gas flow rate.

7. The process of claim 5, wherein the step of processing the semiconductor substrate the first gas composition is different from the second gas composition.

8. The process of claim 1, wherein the step of processing the semiconductor substrate is further characterized as etching a layer of material on the semiconductor substrate.

9. The process of claim 1, wherein the step of processing the semiconductor substrate is further characterized as depositing a layer of material on the semiconductor substrate.

10. The process of claim 1, wherein the step of providing the plasma reactor comprises providing a plasma reactor wherein the first plasma generation region is further characterized as being powered by a first power supply and the second plasma generation region is further characterized as being powered by a second power supply, the first power supply supplying a first power to the first plasma generation region and the second power supply supplying a second power to the second plasma generation region.

11. The process of claim 10, wherein the step of processing the semiconductor substrate the first power is not equal to the second power.

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