

Description

This invention relates generally to an apparatus and method for converting voltage magnitudes into digital counts and, more particularly, to an apparatus and method for interfacing a transducer providing a discrete analog voltage with a microcomputer.

The need for analog-to-digital conversion, whereby discrete voltage levels are converted into digital formats, is well known. For example, in digital monitoring and control systems, transducers, used to sense parameters such as temperature and pressure, provide discrete analog voltages which must be converted into digital values for use by the digital monitoring and control equipment. That is, such a transducer converts the temperature or pressure, for example, into a voltage level representative of the magnitude of the parameter. To use this voltage with a digital system which is capable of functioning only in response to two voltage levels representing either a logic zero or a logic one, the transducer signal needs to be converted into a digital format.

We are aware of two general techniques by which digital conversion can be accomplished. Both of these techniques convert the voltage from the transducer into an oscillating signal through a voltage controlled oscillator or the like. In one of these techniques, this oscillating signal gates a counter which thereupon counts another oscillating signal having a known frequency so that the count of the known frequency signal is proportional to the transducer signal. In the other technique, the oscillating signal from the transducer is counted by a counter gated by the oscillating signal of known frequency. In both of these techniques, the gating signal and the counting signal are independent; therefore, to ensure accuracy, an oscillator which is stable over a long period of time needs to be used to provide the signal with the known frequency.

To obviate the necessity of using an oscillator having such long-term stability, there is the need for an improved analog-to-digital conversion technique wherein the gating and counting signals are related so that stability is required only within each counting period. This need has been met to some extent by a technique in which an input analog signal is combined with an oscillating signal of a particular frequency to obtain pulse width modulated signals whose width is proportional to the analog signal. The length of the pulses is measured by reference to clock signals provided by the same oscillator which is used to generate the aforementioned oscillating signal so that any variations in the frequency of signals generated by the oscillator are automatically compensated for. An example of such a technique is disclosed in GB-A-2046485.

It is also desirable for such a technique to provide rapid, high resolution conversion for use by high speed devices, such as microcomputers, in accurately monitoring the parameter or using the information to accurately control a system in response to the detected parameter. It is also desirable for such a technique to have a degree of programmability so that the resolution of the conversion can be controlled.

The present invention aims to reduce or overcome the above-noted and other shortcomings of the prior art by utilizing related gating and counting signals so that long-term stability of the basic oscillator is not required. Furthermore, the present invention can provide rapid, high resolution analog-to-digital conversion, the resolution of which can be programmed in the preferred embodiment.

The present invention provides a method of interfacing a transducer with a microcomputer, comprising:

generating a first oscillating signal (f_{osc}) at a first frequency;

generating from the first oscillating signal a second oscillating signal having a second frequency which is less than the first frequency;

generating a pulse width modulated signal derived from a signal proportional to a signal from the transducer and the second oscillating signal;

supplying the pulse width modulated signal to a counter so that the counter is activated to count during counting periods each defined by a respective pulse of the pulse width modulated signal;

driving the counter with the first oscillating signal so that the counter provides a count of the cycles of the first oscillating signal during each counting period, wherein each count is made consistent with each other count of different counting periods by changes in the pulse width modulated signal responsive to changes in the first frequency;

characterised by integrating the second oscillating signal to generate an integrated signal; comparing the integrated signal with the signal proportional to the signal from the transducer and generating said pulse width modulated signal in response to said compared integrated signal; both resetting and gating the counter with said pulse width modulated signal;

loading each count from the counter into a latch in response to the end of the respective pulse during which the count loaded was made; and

communicating the pulse width modulated signal to the microcomputer and indicating, by the end of the respective pulse during which the count loaded was made, that a count has been loaded into the latch means.

The present invention also provides an apparatus for interfacing a transducer to a microcomputer comprising:

means for providing a voltage in response to an output from the transducer;

oscillator means for generating a first signal having a first frequency;

divider means, connected to said oscillator means, for converting said first signal into a second signal having a second frequency which is less than said first frequency;

means for providing a stream of pulses derived from said second signal and said voltage generated in response to said transducer output, wherein each pulse within said stream has a width directly proportional to said voltage and wherein each pulse is defined at a frequency which automatically changes in response to a change in said first frequency;

a counter including:

an output and a counting input connected to said oscillator means for receiving said first signal and being arranged to provide a count of the cycles of said first signal received through said counting input during each counting period defined by the width of one of the pulses of said stream of pulses, said counting periods being automatically compensated for any change in said first frequency;

characterised by said means for providing a stream of pulses comprising:

integrator means; connected to said divider means, for converting said second signal into an integrated signal;

comparator means for comparing said integrated signal and said voltage and for providing in response thereto said stream of pulses including:

an inverting input connected to said integrator means; and

a non-inverting input connected to said means for connecting to the transducer and for providing a voltage in response to an output from the transducer;

said counter further comprising:

a reset input (R) and a gate input (G), both said reset input and said gate input connected to said comparator means for receiving said stream of pulses; so that for each pulse of said stream of pulses received at both said reset input and said gate input said counter provides through said output said count of the cycles of said first signal received through said counting input during each counting period, and said apparatus further comprising:

latch means, connected to said output of said counter and to said comparator means, for loading a respective count from said counter means into said latch means in response to the end of the same respective pulse during which the respective count was made; means for connecting said latch means to the microcomputer; and

means for connecting said comparator means to the microcomputer so that said stream of pulses provided by said comparator means is communicated to the microcomputer, wherein the end of each respective pulse to which said latch means is responsive also indicates to the microcomputer that a count has been loaded into said latch means.

In order that the invention may be more fully understood, one embodiment thereof will now be described, by way of example only, with reference to the accompanying drawing which shows schematically a circuit diagram of the embodiment which is an arrangement by which a transducer can be interfaced to a microcomputer using a synchronous, ratio-metric, pulse width modulation technique allowing for rapid acquisition of the transducer signal at a resolution limited only by the period of an oscillator. This apparatus can be more generally adapted to convert a voltage magnitude into a digital count; however, for the preferred embodiment described herein, reference will be made to its use with a transducer 2 of a suitable type as known to the art, such as one capable of detecting a temperature or pressure and converting it into an analog voltage output. Associated with the transducer is an amplifier 4, also of suitable type for amplifying the transducer output to an appropriate voltage level to be used with the present invention.

The preferred embodiment of the present invention broadly includes means for providing a clocking signal having a frequency; modulation means, responsive to the clocking signal and to the voltage magnitude from the transducer, for generating another signal having another frequency less than the initial frequency; and counter means, responsive to the clocking signal and the signal from the modulation means, for generating a digital count corresponding to the magnitude of the parameter sensed by the transducer.

The means for providing a clocking signal is shown in the drawing as being particularly provided through an oscillator means 6 for generating the signal at a frequency f_{osc} . The oscillator 6 is of any suitable type as known to the art; however, it does not need to be one having long-term stability because the stability within the preferred embodiment need only be maintained for one period of a signal derived from the clocking signal, which derived signal is shown in the drawing as having a frequency f_M provided within the modulation means in response to the clocking signal.

The derived signal having the frequency f_M is provided through a divider means for converting the clocking signal into the derived signal. In the preferred embodiment the divider means includes a divide-by-N counter 8 which divides the f_{osc} clocking signal provided at a count input of the counter.

8 by a factor N, which in the preferred embodiment is programmable by using a suitable digital counter device as known to the art. The programmability of the counter 8 allows the preferred embodiment to have a variable resolution. In operation, the counter 8 divides the input clocking signal to provide a fifty percent duty cycled square wave signal at its output. As mentioned, the counter 8 can be of a suitable type as known to the art; however, it is preferably one which has, or can be controlled to have, a stable amplitude at its output for accurate control of an integrator means forming another part of the modulation means.

The integrator means is generally identified in the drawing by the reference numeral 10. The integrator means 10 integrates the square wave signal from the counter 8 into an integrated signal having a triangular waveform. In the illustrated embodiment, the integrator means 10 includes an amplifier 12 having an input connected by resistive means, including a resistor 14, to the output of the counter 8. The output and input of the amplifier 12 are interconnected by capacitive means including a capacitor 16. In this configuration for constructing an integrator as known to the art, the integrator means 10 provides an output mathematically characterized as

$$v_o = \frac{1}{RC} \int_{t_1}^{t_2} v dt$$

where the period t_1 to t_2 is one-half a cycle of the signal. This output signal is schematically illustrated in the drawing and identified by the reference numeral 18.

The signal 18 is provided to the inverting input of a comparator means 20 forming still another part of the modulation means of the present invention. The comparator means 20 also has a non-inverting input which is connected to the output of the amplifier 4 for receiving the amplified output from the transducer 2. In the preferred embodiment the comparator means 20 is provided by a suitable differential amplifier suitably constructed to perform the comparison function. In performing this function, the comparator means 20 compares the integrated signal 18 with the voltage magnitude from the amplifier 4 to provide a pulse signal 22 wherein each pulse within the stream of pulses of the signal 22 has a width directly proportional to the output of the transducer 2. This is achieved by having the output from the amplifier 4 set the threshold against which the triangular signal 18 is compared. As the voltage magnitude from the amplifier 4 varies, this varies the point at which the triangular wave 18 causes the comparator means 20 to gen-

erate a pulse of the signal 22. Therefore, the signal 22 may be more specifically referred to as a pulse width modulated signal.

The counter means of the preferred embodiment includes a digital counter 24 of a suitable type as known to the art. The counter 24 has a gate input 26 and a reset input 28, both of which are connected to the modulation means, specifically to the output of the comparator means 20. In the preferred embodiment, the counter 24 is of a type which is reset when a rising edge of the signal 22 is received at the reset input 28 and which is activated to count when the rising edge of the signal 22 is received at the gate input 26.

The counter 24 also includes a counting input 30 which is connected to the oscillator 6 for receiving the clocking signal having the frequency f_{osc} . Therefore, when the counter 24 is reset and gated upon the rising edge of the signal 22, the counter 24 counts at the rate of the clocking signal having the frequency f_{osc} until the next falling edge of the signal 22 is received at the gating input 26, which falling edge deactivates the gating input 26 and the counter 24. Thus, the counter 24 effectively counts the number of periods of the clocking signal received during a count time defined by each pulse of the pulse width modulated signal 22 so that the number of periods counted is proportional to the voltage magnitude setting the threshold at the non-inverting input of the comparator means 20. In the preferred embodiment, the counter 24 has a sufficient number of bits in its output to achieve a count corresponding to the factor N programmed into the counter 8.

From the foregoing description of the construction and operation of the preferred embodiment of the present invention, it is apparent that both the gating and clocking signals, which are used by the counter 24 in generating the ultimate count which is proportional to the output of the transducer 2, are related so that the stability of the oscillator 6 need be maintained only during each counting period defined by each pulse of the signal 22. That is, if the period or frequency of the primary signal changes, the period or frequency of the derived signals controlling the switching of the comparator means 20 (and thus the period or frequency of the signal 22) will similarly change, thereby maintaining automatically compensated control of the counter 24 to provide consistent counts.

To utilize the present invention in specifically interfacing the transducer with a microcomputer, the preferred embodiment of the present invention further includes a latch means 32 for interfacing the digital count with a microcomputer (not shown). The latch means is of any suitable type having a sufficient number of inputs for receiving the number of bits of output from the counter 24. The latch

means 32 also includes a latch or load input connected to the comparator means 20 for receiving the pulse width modulated signal 22. In the preferred embodiment, latching or loading occurs upon the falling edge of each pulse of the signal 22.

The means for communicating with the microcomputer also includes a conductor 34 providing means for connecting the signal 22 to the microcomputer as a data ready signal as indicated in the drawing.

To more specifically illustrate the operation of the present invention, a specific example of signal levels will be described. For example, the integrator means 10 may be constructed so that the signal 18 has a 12-volt peak-to-peak output range between zero and 12 volts. The amplifier 4 can be constructed to provide an output within the range between 1 and 11 volts in response to the output from the transducer 2. This combination of ranges will ensure proper operation of the comparator means 20 in generating the pulse width modulated signal 22.

The counter 8 is suitably programmed to select the desirable divisor, which in this specific example will be selected to be 1,000 to provide a 1/1000-th resolution. The factor N is selected based on the expected rate of change, or slew rate, of the data to ensure adequate accuracy. If f_N is significantly greater than the slew rate, the error will be less than $1/N$.

With the foregoing construction, the method of the present invention is implemented. This method includes generating the clocking signal at the frequency f_{osc} and generating therefrom the signal having the frequency f_N . This f_N signal is integrated so that the signal 18 is provided. The signal 18 and the voltage from the amplifier 4 are compared so that the pulse width modulated signal 22 is generated. This pulse width modulated signal 22 gates the counter 24, which is then driven by the clocking signal having the frequency f_{osc} so that the counter 24 counts at the f_{osc} rate only during periods when the counter 24 is gated on by the pulse width modulated signal. Once a count is established, it can be communicated, such as to a microcomputer, through the latch means 32 upon the falling edge of a pulse within the signal 22, which pulse indicates to the microcomputer that data have been latched in the latch means 32.

Thus, the present invention provides an analog-to-digital conversion apparatus and method which provides rapid, high resolution interfacing of a transducer. The technique utilizes an oscillator, the long-term stability of which is not critical. In the preferred embodiment the resolution is programmable.

Claims

1. A method of interfacing a transducer with a microcomputer, comprising:
 - generating a first oscillating signal (f_{osc}) at a first frequency;
 - generating from the first oscillating signal a second oscillating signal having a second frequency which is less than the first frequency;
 - generating a pulse width modulated signal (22) derived from a signal proportional to a signal from the transducer and the second oscillating signal;
 - supplying the pulse width modulated signal (22) to a counter so that the counter is activated to count during counting periods each defined by a respective pulse of the pulse width modulated signal;
 - driving the counter with the first oscillating signal so that the counter provides a count of the cycles of the first oscillating signal during each counting period, wherein each count is made consistent with each other count of different counting periods by changes in the pulse width modulated signal responsive to changes in the first frequency;
 - characterised by integrating the second oscillating signal to generate an integrated signal; comparing the integrated signal with the signal proportional to the signal from the transducer and generating said pulse width modulated signal in response to said compared integrated signal; both resetting and gating the counter with said pulse width modulated signal;
 - loading each count from the counter into a latch in response to the end of the respective pulse during which the count loaded was made; and
 - communicating the pulse width modulated signal to the microcomputer and indicating, by the end of the respective pulse during which the count loaded was made, that a count has been loaded into the latch means.
2. An apparatus for interfacing a transducer (2) to a microcomputer comprising:
 - means (4) for providing a voltage in response to an output from the transducer (2);
 - oscillator means (6) for generating a first signal having a first frequency;
 - divider means (8), connected to said oscillator means (6), for converting said first signal into a second signal having a second frequency which is less than said first frequency;
 - means for providing a stream of pulses (22) derived from said second signal and said voltage generated in response to said transducer output, wherein each pulse within said

means 32 also includes a latch or load input connected to the comparator means 20 for receiving the pulse width modulated signal 22. In the preferred embodiment, latching or loading occurs upon the falling edge of each pulse of the signal 22.

The means for communicating with the microcomputer also includes a conductor 34 providing means for connecting the signal 22 to the microcomputer as a data ready signal as indicated in the drawing.

To more specifically illustrate the operation of the present invention, a specific example of signal levels will be described. For example, the integrator means 10 may be constructed so that the signal 18 has a 12-volt peak-to-peak output range between zero and 12 volts. The amplifier 4 can be constructed to provide an output within the range between 1 and 11 volts in response to the output from the transducer 2. This combination of ranges will ensure proper operation of the comparator means 20 in generating the pulse width modulated signal 22.

The counter 8 is suitably programmed to select the desirable divisor, which in this specific example will be selected to be 1,000 to provide a 1/1000-th resolution. The factor N is selected based on the expected rate of change, or slew rate, of the data to ensure adequate accuracy. If f_N is significantly greater than the slew rate, the error will be less than $1/N$.

With the foregoing construction, the method of the present invention is implemented. This method includes generating the clocking signal at the frequency f_{osc} and generating therefrom the signal having the frequency f_N . This f_N signal is integrated so that the signal 18 is provided. The signal 18 and the voltage from the amplifier 4 are compared so that the pulse width modulated signal 22 is generated. This pulse width modulated signal 22 gates the counter 24, which is then driven by the clocking signal having the frequency f_{osc} so that the counter 24 counts at the f_{osc} rate only during periods when the counter 24 is gated on by the pulse width modulated signal. Once a count is established, it can be communicated, such as to a microcomputer, through the latch means 32 upon the falling edge of a pulse within the signal 22, which pulse indicates to the microcomputer that data have been latched in the latch means 32.

Thus, the present invention provides an analog-to-digital conversion apparatus and method which provides rapid, high resolution interfacing of a transducer. The technique utilizes an oscillator, the long-term stability of which is not critical. In the preferred embodiment the resolution is programmable.

Claims

1. A method of interfacing a transducer with a microcomputer, comprising:
 - generating a first oscillating signal (f_{osc}) at a first frequency;
 - generating from the first oscillating signal a second oscillating signal having a second frequency which is less than the first frequency;
 - generating a pulse width modulated signal (22) derived from a signal proportional to a signal from the transducer and the second oscillating signal;
 - supplying the pulse width modulated signal (22) to a counter so that the counter is activated to count during counting periods each defined by a respective pulse of the pulse width modulated signal;
 - driving the counter with the first oscillating signal so that the counter provides a count of the cycles of the first oscillating signal during each counting period, wherein each count is made consistent with each other count of different counting periods by changes in the pulse width modulated signal responsive to changes in the first frequency;
 - characterised by integrating the second oscillating signal to generate an integrated signal; comparing the integrated signal with the signal proportional to the signal from the transducer and generating said pulse width modulated signal in response to said compared integrated signal; both resetting and gating the counter with said pulse width modulated signal;
 - loading each count from the counter into a latch in response to the end of the respective pulse during which the count loaded was made; and
 - communicating the pulse width modulated signal to the microcomputer and indicating, by the end of the respective pulse during which the count loaded was made, that a count has been loaded into the latch means.
2. An apparatus for interfacing a transducer (2) to a microcomputer comprising:
 - means (4) for providing a voltage in response to an output from the transducer (2);
 - oscillator means (6) for generating a first signal having a first frequency;
 - divider means (8), connected to said oscillator means (6), for converting said first signal into a second signal having a second frequency which is less than said first frequency;
 - means for providing a stream of pulses (22) derived from said second signal and said voltage generated in response to said transducer output, wherein each pulse within said



stream has a width directly proportional to said voltage and wherein each pulse is defined at a frequency which automatically changes in response to a change in said first frequency;

a counter (24) including:

an output and a counting input (30) connected to said oscillator means (6) for receiving said first signal and being arranged to provide a count of the cycles of said first signal received through said counting input during each counting period defined by the width of one of the pulses of said stream of pulses, said counting periods being automatically compensated for any change in said first frequency;

characterised by said means for providing a stream of pulses comprising:

integrator means (10); connected to said divider means (8), for converting said second signal into an integrated signal;

comparator means (20) for comparing said integrated signal and said voltage and for providing in response thereto said stream of pulses (22) including:

an inverting input connected to said integrator means (10); and

a non-inverting input connected to said means (4) for connecting to the transducer and for providing a voltage in response to an output from the transducer;

said counter (24) further comprising:

a reset input (R) and a gate input (G), both said reset input and said gate input connected to said comparator means (20) for receiving said stream of pulses; so that for each pulse of said stream of pulses received at both said reset input and said gate input said counter (24) provides through said output said count of the cycles of said first signal received through said counting input during each counting period, and said apparatus further comprising:

latch means (32), connected to said output of said counter (24) and to said comparator means (20), for loading a respective count from said counter means (24) into said latch means (32) in response to the end of the same respective pulse during which the respective count was made; means for connecting said latch means (32) to the microcomputer; and

means (34) for connecting said comparator means (20) to the microcomputer so that said stream of pulses provided by said comparator means is communicated to the microcomputer, wherein the end of each respective pulse to which said latch means is responsive also indicates to the microcomputer that a count has been loaded into said latch means.

Patentansprüche

1. Verfahren zum Koppeln eines Wandlers mit einem Mikrocomputer, bei welchem Verfahren ein erstes oszillierendes Signal (f_{osc}) bei einer ersten Frequenz erzeugt wird;
ein zweites oszillierendes Signal mit einer zweiten Frequenz, die kleiner als die erste Frequenz ist, aus dem ersten oszillierenden Signal erzeugt wird;
ein pulsbreitenmoduliertes Signal (22) erzeugt wird, das von einem Signal, das einen von dem Wandler ausgehenden Signal proportional ist, und dem zweiten oszillierenden Signal abgeleitet wird;
das pulsbreitenmodulierte Signal (22) einem Zähler zugeführt wird, derart, daß der Zähler während Zählzeiten zum Zählen eingeschaltet ist, die jeweils durch einen Impuls des pulsbreitenmodulierten Signals bestimmt sind;
der Zähler mit dem ersten oszillierenden Signal angesteuert wird, derart, daß der Zähler eine Zählung der Perioden des ersten oszillierenden Signals während jeder Zählzeit liefert, wobei jede Zählung mit jeder anderen Zählung aus anderen Zählzeiten dadurch konsistent gemacht wird, daß das pulsbreitenmodulierte Signal durch Ansprechen auf Änderungen in der ersten Frequenz geändert wird;
gekennzeichnet durch Integrieren des zweiten oszillierenden Signals zur Erzeugung eines integrierten Signals; Vergleichen des integrierten Signals mit dem Signal, das dem vom Wandler ausgehenden Signal proportional ist, und Erzeugen des pulsbreitenmodulierten Signals unter Ansprechen auf das aus dem integrierten Signal erhaltene Vergleichssignal; Rückstellen und Ansteuern des Zählers mit dem pulsbreitenmodulierten Signal;
Laden jeder Zählung des Zählers in einen Zwischenspeicher unter Ansprechen auf das Ende jeweils des Impulses, während dessen die geladene Zählung erfolgte; und
Übertragen des pulsbreitenmodulierten Signals auf den Mikrocomputer und Anzeigen, daß eine Zählung in den Zwischenspeicher geladen worden ist, durch das Ende jeweils des Impulses, während dessen die geladene Zählung erfolgte.
2. Vorrichtung zur Kopplung eines Wandlers (2) mit einem Mikrocomputer, enthaltend
Mittel (4) zur Erzeugung einer Spannung unter Ansprechen auf einen Ausgang aus dem Wandler (2);
Oszillatormittel (6) zur Erzeugung eines ersten Signals mit einer ersten Frequenz;
mit den Oszillatormitteln (6) verbundene Teiler-





mittel (8) zur Umwandlung des ersten Signals in ein zweites Signal mit einer zweiten Frequenz, die kleiner als die erste Frequenz ist; Mittel zur Erzeugung eines Impulsstroms (22) aus dem zweiten Signal und der Spannung, die unter Ansprechen auf den Wandlerausgang erzeugt wurde, wobei jeder Impuls innerhalb des Stromes eine der Spannung direkt proportionale Breite hat und jeder Impuls durch eine Frequenz bestimmt ist, die sich unter Ansprechen auf eine Änderung der ersten Frequenz automatisch ändert;

einen Zähler (24) mit:

einem Ausgang und einem Zähleingang (30), der zum Empfang des ersten Signals mit den Oszillatormitteln (6) verbunden und so eingerichtet ist, daß er eine Zählung der Perioden des ersten Signals, das über den Zähleingang erhalten wird, während jeder Zählzeit liefert, die durch die Breite eines der Impulse aus dem Impulsstrom bestimmt ist und in denen jede Änderung der ersten Frequenz automatisch kompensiert wird;

gekennzeichnet durch Mittel zur Erzeugung eines Impulsstroms, die umfassen:

Integratormittel (10), die mit den Teilmitteln (8) verbunden sind und das zweite Signal in ein integriertes Signal umwandeln;

Vergleichermittel (20), die das integrierte Signal und die Spannung vergleichen und unter Ansprechen darauf den Impulsstrom (22) erzeugen, enthaltend:

einen mit den Integratormitteln (10) verbundenen invertierenden Eingang; und

einen nichtinvertierenden Eingang, der mit den Mitteln (4) zur Verbindung mit dem Wandler und zur Erzeugung einer Spannung unter Ansprechen auf einen Ausgang aus dem Wandler verbunden ist;

dadurch, daß der Zähler (24) ferner umfaßt:

einen Rückstelleingang (R) und einen Steuereingang (G), die beide zum Erhalt des Impulsstroms an die Vergleichermittel (20) angeschlossen sind; so daß der Zähler (24) für jeden Impuls aus dem am Rückstelleingang und am Steuereingang empfangenen Impulsstrom am Ausgang die Zählung der Perioden des ersten Signals liefert, das während jeder Zählzeit über den Zähleingang empfangen wurde, und dadurch, daß die Vorrichtung weiter aufweist:

mit dem Ausgang des Zählers (24) und den Vergleichermitteln (20) verbundene Zwischenspeichermittel (32) zur Ladung jeweils einer Zählung von den Zählermitteln (24) in die Zwischenspeichermittel (20) unter Ansprechen auf das Ende jeweils des Impulses, während dessen die betreffende Zählung erfolgte; Mittel zur

Verbindung der Zwischenspeichermittel (32) mit dem Mikrocomputer; und Mittel (34) zur Verbindung der Vergleichermittel (20) mit dem Mikrocomputer, so daß der von den Vergleichermitteln gelieferte Impulsstrom zum Mikrocomputer übertragen wird, wobei das Ende jeweils desjenigen Impulses, auf den die Zwischenspeichermittel ansprechen, ebenfalls dem Mikrocomputer angezeigt, daß eine Zählung in die Zwischenspeichermittel geladen worden ist.

Revendications

1. Procédé pour relier un transducteur et un micro-calculateur, comportant les étapes consistant à :

engendrer un premier signal oscillant (f_{osc}) à une première fréquence;

engendrer à partir du premier signal oscillant un second signal oscillant ayant une seconde fréquence qui est plus petite que la première fréquence;

engendrer un signal modulé en largeur d'impulsion dérivé à partir d'un signal proportionnel à un signal provenant du transducteur et du second signal oscillant;

transmettre le signal modulé en largeur d'impulsion (22) vers un compteur de telle sorte que le compteur soit activé pour compter pendant des périodes de comptage définies chacune par une impulsion respective du signal modulé en largeur d'impulsion;

piloter le compteur à l'aide du premier signal oscillant de telle sorte que le compteur fournisse un comptage des cycles du premier signal oscillant pendant chaque période de comptage, dans lequel chaque comptage est rendu cohérent avec chaque autre comptage de différentes périodes de comptage par modification du signal modulé en largeur d'impulsion en réponse à des modifications de la première fréquence;

caractérisé en ce qu'on intègre le second signal oscillant pour engendrer un signal intégré; on compare le signal intégré au signal proportionnel au signal provenant du transducteur et on engendre ledit signal modulé en largeur d'impulsion en réponse audit signal intégré comparé; on réinitialise et on déclenche à la fois le compteur à l'aide dudit signal modulé en largeur d'impulsion;

on charge chaque comptage provenant du compteur dans un registre en réponse à la fin de l'impulsion respective pendant laquelle le comptage chargé a été réalisé, et

on communique le signal modulé en largeur d'impulsion au micro-calculateur et on

indique, par la fin de l'impulsion respective pendant laquelle le comptage chargé a été réalisé, qu'un comptage a été chargé dans les moyens formant registre.

2. Dispositif pour relier un transducteur (2) à un micro-calculateur comportant :

des moyens (4) pour fournir une tension en réponse à une sortie provenant du transducteur (2);

des moyens (6) formant oscillateur pour engendrer un premier signal ayant une première fréquence;

des moyens (8) formant diviseur, reliés auxdits moyens (6) formant oscillateur, pour convertir ledit premier signal en un second signal ayant une seconde fréquence qui est plus petite que ladite première fréquence;

des moyens pour fournir un train d'impulsions (22) dérivé dudit second signal et de ladite tension engendrée en réponse à ladite sortie de transducteur, dans lequel chaque impulsion située à l'intérieur dudit train a une largeur directement proportionnelle à ladite tension et dans lequel chaque impulsion est définie à une fréquence qui change de manière automatique en réponse à un changement de ladite première fréquence;

un compteur (24) comportant :

une sortie et une entrée (30) de comptage reliées auxdits moyens (6) formant oscillateur pour recevoir ledit premier signal et agencées pour fournir un comptage des cycles dudit premier signal reçu à travers ladite entrée de comptage pendant chaque période de comptage définie par la largeur d'une des impulsions dudit train d'impulsions, lesdites périodes de comptage étant compensées de manière automatique pour tout changement de ladite première fréquence;

caractérisé en ce que lesdits moyens pour fournir un train d'impulsions comportent :

des moyens (10) formant intégrateur, reliés auxdits moyens (8) formant diviseur, pour convertir ledit second signal en un signal intégré,

des moyens (20) formant comparateur pour comparer ledit signal intégré et ladite tension et pour fournir en réponse ledit train d'impulsions (22) comportant :

une entrée inverseuse reliée auxdits moyens (10) formant intégrateur, et

une entrée non inverseuse reliée auxdits moyens (4) de connexion au transducteur et pour fournir une tension en réponse à une sortie provenant du transducteur;

ledit compteur (24) comportant en outre:

une entrée de réinitialisation (R) et une

entrée (G) de déclenchement à la fois ladite entrée de réinitialisation et ladite entrée de déclenchement étant reliées auxdits moyens (20) formant comparateur pour recevoir ledit train d'impulsions, de telle sorte que pour chaque impulsion dudit train d'impulsions reçue à la fois au niveau de ladite entrée de réinitialisation et de ladite entrée de déclenchement ledit compteur (24) fournit à travers ladite sortie ledit comptage de cycles dudit premier signal reçu à travers ladite entrée de comptage pendant chaque période de comptage, et ledit dispositif comportant en outre :

des moyens (32) formant registre, reliés à ladite sortie dudit compteur (24) et auxdits moyens (20) formant comparateur, pour charger un comptage respectif provenant desdits moyens (24) formant compteur dans lesdits moyens (32) formant registre en réponse à la fin de la même impulsion respective pendant laquelle le comptage respectif a été réalisé, des moyens pour relier lesdits moyens (32) formant registre au micro-calculateur, et

des moyens (34) pour relier lesdits moyens (20) formant comparateur au micro-calculateur de telle sorte que ledit train d'impulsions fourni par lesdits moyens formant comparateur soit communiqué au micro-calculateur, dans lequel la fin de chaque impulsion respective pour laquelle lesdits moyens formant registre sont sensibles indique également au micro-calculateur qu'un comptage a été chargé dans lesdits moyens formant registre.

