

A METHOD OF FABRICATING A COMPOSITE SUBSTRATE WITH IMPROVED ELECTRICAL PROPERTIES

The present invention relates to a method of low temperature fabrication of a substrate referred to as "hybrid" or "composite", of the type comprising at least one buried insulating layer, i.e. interposed between a support substrate and an active layer of semiconductor material derived from a source substrate.

More precisely, the invention relates to a method of obtaining a composite substrate as mentioned above, with substantially improved electrical properties. Said substrates are used in the fields of optics, electronics, and optoelectronics.

In the description and claims below, the term "insulator" designates an electrically insulating material optionally having high dielectric permittivity.

Further, the composite substrates envisaged by the method of the invention are all characterized in that they cannot undergo high temperature heat treatment without damage. They can be subdivided into two groups.

The first group comprises composite substrates wherein at least one of the substrates between the donor substrate and the receiving substrate cannot be exposed to a temperature defined as "raised", or even to a high temperature.

Several types of such donor or receiving substrates can be distinguished:

a) those including elements that might diffuse:

The "raised" temperature is then the temperature beyond which diffusion of the element becomes damaging. This is the case with substrates including:

- doping profiles (of boron or arsenic, for example);
- buried metallic layers (ground plane, buried gates); or
- stacks of semiconductor layers having sharp interfaces that need to be preserved (silicon (Si) on

silicon germanium (SiGe), or silicon (Si) on germanium (Ge));

b) those which are unstable or liquid at high temperature:

5 • germanium, for example, has a melting temperature of about 900°C and cannot be subjected to temperatures higher than 750°C or even higher than 600°C;

10 • substrates comprising layers with strain state that is to be retained (relaxed, or strained in tension or in compression) and which could be perturbed if the substrate were exposed to a high temperature.

The second group comprises composite substrates which cannot be exposed to a raised temperature after bonding the source substrate onto the support substrate:

15 a) either because of differences between the coefficients of thermal expansion of those two materials. This is particularly the case with substrates of the "silicon on quartz" type known by the acronym "SOQ";

20 b) or when the diffusion of elements from one substrate towards another is to be avoided.

More precisely, the electrical properties which the method of the invention is intended to improve are:

25 • charge density (known by the abbreviation "Qbox") in the buried insulating layer. Obtaining a value of less than 5×10^{11} charges per cm^2 is desirable;

30 • breakdown voltage, i.e. the voltage beyond which the resistivity of the insulator falls sharply. Obtaining maximum values is desirable. As an example, for a buried silicon oxide layer, a preferred value is as close as possible to 10 MV/cm [megavolts/centimeter];

35 • hole and/or electron mobility in the active layer. As an illustrative example, it would be desirable to obtain an electron mobility of more than $500 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ [$\text{centimeter}^2 \cdot \text{volt}^{-1} \cdot \text{second}^{-1}$] in silicon doped with boron at a concentration of the order of 10^{15} atoms/ cm^3 ;

 • "DIT", or "density of interface trap" value, which designates the trap density at an interface between two

layers. In the context of the present invention, an improvement is sought in DIT values at the interface between the buried insulating layer and the active layer, and optionally, in DIT values at the interface between
5 the insulating layer and a neighboring layer.

The description below focuses on the DIT value since it is one of the principal parameters on which the substrate formation steps of the invention have an influence. Further, that parameter has an effect on
10 mobility. However, the invention in general aims to improve the electrical performance of the final substrate.

Traps have the capacity to retain or release charge carriers at interfaces. They have an extremely
15 deleterious impact on the electrical properties of future electronic components which will be produced on composite substrate.

The density of traps at an interface, referred to below as the "DIT value" for simplification, is expressed
20 as the number of traps/eV.cm². The higher the DIT value, the worse the electrical properties of the substrate.

As an example, a value of 10¹².eV⁻¹.cm⁻² is a high value which corresponds to poor electrical properties for the substrate. Currently, the best DIT values obtained
25 are of the order of 10¹⁰.eV⁻¹.cm⁻² for interfaces between very good quality oxides, known as "gate oxides", and their support. Such oxides are found, for example, in transistors, memories, capacitors, and other types of components forming integrated circuits.

30 Figures 1A to 1E illustrate the various steps of one mode of fabricating an SOI type substrate, which is known in the art.

As shown in Figures 1A and 1B, that method consists in oxidizing a source substrate **Sou** to form a layer of
35 oxide **Oxy** at its surface, then in carrying out atomic species implantation to define an active layer **Cact**. The

oxide layer is generally fairly thick, of the order of 150 nm [nanometers].

After bonding to a support substrate **Sup** (Figure 1C) and detaching the remainder of the source substrate **Sou** (Figure 1D), a composite substrate is obtained comprising an oxide layer **Oxy** interposed between a support and an active layer, and which has a contact interface with each of them, with respective reference numerals I_1 and I_2 (Figure 1D).

Finally, it may be formed on the upper surface of the composite substrate obtained, a layer intended to protect that surface during finishing heat treatments carried out on the substrate. Hence, the substrate is covered with a protective layer **Cpr** and there is an interface I_3 between that protective layer **Cpr** and the active layer **Cact**.

From the prior art, methods are already known which can improve, i.e. reduce, DIT values, at certain interfaces of a composite substrate.

One of them, known by the acronym "FGA" for "forming gas anneal", consists in carrying out a repair/recovery heat treatment of interfaces at a low temperature, of the order of 450°C, in an atmosphere containing hydrogen and a neutral gas.

However, when such a method is carried out at 450°C, its effect regarding improvement to the DIT value is exerted solely on the interface I_3 between the protective layer **Cpr** and an active layer **Cact** and not on the interfaces I_1 and I_2 , or only very slightly. That FGA treatment method loses effectiveness at each interface which is encountered. Thus, it is relatively ineffective for deep-lying interfaces.

A further possibility consists in carrying out an annealing heat treatment at high temperature, i.e. above 900°C or even above 1000°C. Such a treatment may improve the DIT value at the interface I_2 , but cannot be applied to a certain number of substrates, as is discussed below.

This applies to certain structures formed by bonding, or to composite substrates containing materials that are unstable at high temperature, such as germanium (Ge) or strained Si (sSi), for example.

5 This also applies to substrates formed from a plurality of materials having significant differences in thermal expansion coefficient (silicon on quartz, for example) or substrates containing elements that should not be allowed to diffuse, for example doping profiles or
10 a structure including a metallic ground plane.

Thus, it is not possible to apply any DIT improvement treatments employing high temperatures to that type of structure.

In addition, it is also necessary to use for their
15 fabrication, bonding techniques which do not necessitate high temperature heat treatments.

Hence, from the article by Suni et al, "*Effect of plasma activation on hydrophilic bonding of Si and SiO₂*", Electrochemical Society Proceedings, Volume 2001-27, pp
20 22-30, a solution is known which consists in preceding the step of bringing the surfaces to be bonded into intimate contact, by a step of plasma activation of at least one of the surfaces to be bonded, namely that of the support **Sup** and/or of the source **Sou**.

25 A high bonding energy is thus obtained at the interface **I₁**, close to 1 J/m² [joule/meter²], even after an anneal at 200°C for just 1 hour.

However, plasma activation deteriorates the electrical characteristics of the interface **I₁**, and in
30 particular its DIT values, in a fairly significant manner.

Reference in this regard should be made to the article by K. Schjölberg-Henriksen et al, "*Oxide charges induced by plasma activation for wafer bonding*", Sensors and Actuators A 102 (2002), 99-105, which shows the
35 negative effect of plasma activation on the electrical properties of substrates.

Further, that article also shows that it is possible to correct the deleterious effects of plasma activation on the electrical properties of substrates by a subsequent "FGA" type annealing treatment. That article
5 shows that for a good quality oxide, produced on a silicon substrate, the DIT value is of the order of several $10^{10} \cdot \text{eV}^{-1} \cdot \text{cm}^{-2}$ after plasma activation, but that unfortunately the bonding forces after the "FGA" treatment are reduced by more than 50%.

10 However, it is also important to produce a strong bond in a composite structure when subsequent thinning of one of the constituent layers is envisaged, to avoid problems with non transferred zones.

The invention aims to overcome the above-mentioned
15 disadvantages of the prior art.

More precisely, its aim is to provide a method of producing a composite substrate including a buried insulating layer, which layer has good electrical properties principally at the interface with the active
20 layer which it supports.

More particularly, this method is applicable to composite substrates in which at least one layer cannot sustain heat treatments at raised temperatures of close to 400°C or 500°C , or even at high temperatures, i.e.
25 900°C or more.

Finally, said method must also be able to produce a composite substrate in which the transferred active layer adheres very strongly to the insulating layer on which it rests.

30 To this end, the invention relates to a method of fabricating a composite substrate with improved electrical properties, of the type comprising at least one thin insulating layer, interposed between a first substrate, termed the "support", and a layer of
35 semiconductor material, termed the "active layer".

In accordance with the invention, said method comprises, in the following order, the steps of:

- forming or depositing an insulating layer on a second substrate, termed the "source substrate", and optionally an insulating layer on said support substrate;
 - recovery heat treatment of said insulating layer and optionally of said insulating layer formed on the support substrate;
 - plasma activation of at least one of the two faces intended to be bonded together, selected from the front face of the insulating layer of the source substrate and the front face of the support substrate or the front face of the insulating layer of the support substrate;
 - bonding, by molecular bonding, said support substrate together with said source substrate, such that said insulating layer is located between said support substrate and said source substrate; and
 - lifting off a portion, termed the "back", of said source substrate, to retain only a thickness of material constituting said active layer and to produce said composite substrate.
- 20 In accordance with other advantageous and non-limiting characteristics of the invention, taken alone or in combination:
- the recovery heat treatment comprises an FGA type treatment carried out by annealing in an atmosphere of neutral gas and hydrogen, at a temperature in the range 25 400°C to 600°C, for a period in the range from about thirty minutes to two hours;
 - the recovery heat treatment comprises a heat treatment at a temperature of more than 900°C, in a neutral gas atmosphere, optionally in the presence of 30 oxygen, for about 30 minutes to 1 hour;
 - the recovery heat treatment comprises a RTA type heat treatment carried out for several seconds to several minutes, approximately;
 - 35 • the plasma activation treatment consists in introducing the substrate to be treated into an activation chamber and exposing it therein for about 5

seconds to 60 seconds to a plasma formed from a pure gas selected from oxygen (O_2), nitrogen (N_2), argon (Ar) and helium (He) or a mixture of said gases, said gas being introduced into the chamber at a flow rate in the range 10 standard cubic centimeters per minute (sccm) to 1000 sccm, the established pressure in the chamber being in the range 10 milliTorr (mTorr) to 200 mTorr, the plasma being initiated then maintained by applying radiofrequency power in the range 100 watts (W) to 3000 W;

- the insulating layer is an oxide;
- the insulating layer is a high permittivity dielectric material;
- the high permittivity dielectric material is selected from the group consisting of hafnium dioxide (HfO_2), yttrium oxide (Y_2O_3), strontium and titanium trioxide ($SrTiO_3$), alumina (Al_2O_3), zirconium dioxide (ZrO_2), tantalum pentoxide (Ta_2O_5), titanium dioxide (TiO_2), their nitrides, and their silicides;
- the back portion of the source substrate is lifted off by grinding and/or polishing;
- the method comprises forming a zone of weakness inside the source substrate prior to the plasma activation step and lifting off the back portion of the source substrate, by detachment along said zone of weakness;
- the zone of weakness is obtained by atomic species implantation inside the source substrate;
- said active layer is produced from a material selected from silicon, germanium, and strained silicon;
- the method includes a step of doping all or part of one of the source or support substrates.

Other characteristics and advantages of the invention become apparent from the following description made with reference to the accompanying drawings, which represent a possible implementation in an indicative but non-limiting manner.

In these drawings:

• Figures 1A to 1E are diagrams representing the various steps in the fabrication of an SOI type substrate, in accordance with a known prior art
5 implementation;

• Figures 2A to 2F are diagrams representing the various steps in the fabrication method in accordance with a first implementation of the invention;

• Figures 3A to 3G are diagrams representing
10 variations of the above method.

The various steps of the method of fabricating a composite substrate of the invention are described briefly with reference to Figure 2.

Referring to Figure 2A, it can be seen that the
15 method uses a first substrate 1, termed the "support substrate", and a second substrate 2, termed the "source substrate".

The upper faces of support 1 and source 2 substrates respectively carry reference numerals 10 and 20.

20 As can be seen in Figure 2B, an insulating layer is then formed or deposited on at least the source substrate 2 and optionally on the support substrate 1.

The insulating layer present on the support substrate 1 carries reference numeral 31, and that
25 present on the source substrate 2 carries reference numeral 32.

The free surfaces or front faces of the insulating layers 31, 32 respectively carry reference numerals 310 and 320.

30 The interface between the insulating layer 31 and the support substrate 1 carries the reference numeral 311 and that between the layers 32 and 2 carries the reference 321.

35 As can be seen better in Figure 2C, a heat treatment is then carried out on the source substrate 2 covered with the insulating layer 32, to "recover" said layer 32, i.e. to improve its electrical characteristics and those

of the interface 321. Throughout the remainder of the description and claims, this treatment is termed "recovery heat treatment".

5 If the insulating layer 31 is present on the support substrate 1, it may optionally also undergo a recovery heat treatment.

Figure 2D illustrates the plasma activation step which is carried out over at least one of the two faces intended to be bonded to each other, i.e. over at least
10 one of the faces 320, 310 or 10 (in the absence of the insulating layer 31).

Bonding by molecular bonding of the two substrates 1 and 2 is then carried out so that their front faces 10, 20 face each other (see Figure 2E). The bonding
15 interface has reference numeral 5.

Finally, a portion termed the "back" portion of the source substrate 2 is lifted off to retain only a thickness of that material which constitutes an active layer 21 in the final composite substrate, which has
20 reference numeral 4 (see Figure 2F).

The various steps in the method and the materials selected are described below in greater detail.

In the composite substrate 4, the substrate 1 acts as a mechanical support, as is usually the case in the
25 art.

Further, it is also possible for the support substrate 1 to contain elements which will be constituents of the final electronic components (such as electrodes, a ground plane, a channel, etc).

30 The support substrate 1 is advantageously produced from a semiconductor material.

The active layer 21 of the composite substrate 4 is derived from source substrate 2, as is described below. Said source substrate 2 is also formed from semiconductor
35 material.

Purely by way of illustrative example, various examples of materials that may be used as substrates 1 and 2 are listed below:

• support substrate 1: silicon (Si), silicon carbide (SiC), germanium (Ge), any epitaxially grown layer, for example a layer of germanium (Ge), silicon germanium (SiGe) or gallium nitride (GaN) on a silicon substrate, or even a layer of strained silicon;

• source substrate 2: silicon (Si), germanium (Ge), silicon carbide (SiC), gallium nitride (GaN), silicon germanium (SiGe), gallium arsenide (AsGa), or indium phosphide (InP).

It should be noted that the substrates 1 and 2 may also be multilayered.

The invention is of particularly application to producing composite substrates including a layer that does not tolerate raised or high temperature heat treatments. Examples of materials that can be mentioned that can be a constituent of substrates 1 or 2 are as follows: strained silicon, germanium, a metallic or doped layer, or contiguous layers of semiconductors which are capable of diffusing into each other.

The insulating layers 31, 32 are selected, for example, from layers of oxide or nitride, such as silicon oxide (SiO_2) or silicon nitride (Si_3N_4); germanium oxynitride ($\text{Ge}_x\text{O}_y\text{N}_z$), aluminum nitride (AlN); high permittivity (high k) dielectric materials such as hafnium dioxide (HfO_2), yttrium oxide (Y_2O_3), strontium and titanium trioxide (SrTiO_3), alumina (Al_2O_3), zirconium dioxide (ZrO_2), tantalum pentoxide (Ta_2O_5), titanium dioxide (TiO_2), their nitrides, and their silicides.

The nature of each insulating layer 31 or 32 is selected as a function of the nature of the materials used for the support substrate 1 and the source substrate 2. Further, the insulator 32 is selected in order to optimize the electrical properties of the interface 321.

By way of example, to produce a final substrate 4 of the GeOI (germanium on insulator) type, a thin layer of silicon oxide may be formed on the silicon support substrate and a layer of HfO_2 on the germanium source substrate.

Preferably, the insulators 31, 32 are of excellent quality as regards their electrical properties. More precisely, the insulator 32 has DIT values at interface 321 which are as low as possible.

By way of illustrative example, when the layers 1 and 2 are formed from silicon and the insulating layers 31, 32 are formed from silicon dioxide, the DIT values at interface 321 are $10^{11} \cdot \text{eV}^{-1} \cdot \text{cm}^{-2}$ or less, or even $10^{10} \cdot \text{eV}^{-1} \cdot \text{cm}^{-2}$ or less.

Next, when the insulator is an oxide, it is formed with all precautions taken to form oxides of optimum quality, such as gate oxides. Reference in this regard should be made to the article by Green et al, "*Ultrathin (<4nm) SiO_2 and Si-O-N gate dielectric layers for silicon microelectronics: Understanding the processing, structure and physical and electrical limits*", Journal of Applied Physics, volume 90, n° 5, 1 September 2001, pages 2086 ff.

The surfaces of substrates 1 and 2 on which the oxide is to be formed are prepared by deep cleaning, for example using a treatment in an "RCA" chemical, to prevent any contamination.

"RCA" treatment consists in treating the surfaces in succession with the following:

- a first solution known by the acronym "SC1" (standard clean 1), which comprises a mixture of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and deionized water;

- a second solution known by the acronym "SC2" (standard clean 2), which comprises a mixture of hydrochloric acid (HCl), hydrogen peroxide (H_2O_2) and deionized water.

The oxides are then obtained by an oxidation heat treatment respectively of the support substrate 1 and/or the source substrate 2.

5 The insulating layers 31, 32 may also be obtained by low pressure chemical vapor deposition (LPCVD) or by an atomic layer deposition (ALD) method.

Recovery heat treatment:

10 Said recovery treatment may be carried out in a variety of manners, as shown in Figure 2C.

A first possibility consists of carrying out an "FGA" (forming gas anneal) type thermal anneal.

15 Preferably, said FGA treatment is carried out in an atmosphere of a neutral gas and hydrogen, at a temperature in the range 400°C to 600°C, preferably close to 450°C, for a period in the range from thirty minutes to about two hours, preferably about 90 minutes.

Said treatment is carried out, for example, in a tube furnace under a controlled atmosphere.

20 The insulating layer which underwent said treatment thus has relatively low "DIT" values at the interface with the substrate on which it has been formed.

The "DIT" values achieved are below $10^{11} \text{.eV}^{-1} \text{.cm}^{-2}$, or even below a few $10^{10} \text{.eV}^{-1} \text{.cm}^{-2}$.

25 A second possibility consists of carrying out a high temperature thermal anneal, i.e. at a temperature of more than 900°C, or even 1100°C, in an atmosphere of a neutral gas (for example argon) or a neutral gas and oxygen, for about 30 minutes to 1 hour. Said treatment is carried
30 out, for example, in a tube furnace under a controlled atmosphere.

This second possibility is clearly only employed if one of the two substrates can tolerate such treatments and said treatment is only applied to the substrate,
35 optionally covered with an insulating layer, which can tolerate it.

Said high temperature treatment may optionally be carried out as a complement to the FGA treatment, and preferably before it.

5 Finally, it should be noted that in a variation, the two types of thermal anneal cited above may be carried out in rapid thermal annealing (RTA) equipment. The approximate duration of the recovery anneal method is thus from several seconds to several minutes, typically 30 seconds.

10

Plasma activation treatment:

The plasma activation treatment (Figure 2D) is carried out under conditions which preserve the electrical characteristics and in particular the DIT
15 values of the interface between the insulating layer and the neighboring layer (if such a layer exists). In fact, these values have already been reduced (and thus improved) at the end of the preceding recovery treatment.

"Plasma activation" of a surface is defined as
20 exposing that surface to a plasma, which may in particular be carried out in a vacuum or atmospheric pressure chamber.

Said activation is carried out by controlling various exposure parameters such as the nature, the flow
25 rate or the pressure of the gas supplying the chamber inside which activation is carried out, as well as the applied power.

In the context of the invention, the substrate covered with the insulating layer to be activated is
30 introduced into the chamber, then a pure gas, typically oxygen (O_2), optionally nitrogen (N_2), argon (Ar) or helium (He) or a mixture of said gases, such as oxygen and helium, oxygen and argon or helium and nitrogen, for example, is sent into the chamber, from which the plasma
35 is generated once the power is applied.

The flow rate of the gas used is a function of the volume of the activation chamber and the size of the substrate.

Preferably, the gas is sent in at a flow rate in the
5 range 10 sccm to 1000 sccm. By way of example, a flow rate of 75 sccm is used for a 200 mm diameter substrate is used, and 200 sccm is used for a 300 mm diameter substrate.

The established pressure in the chamber during
10 plasma treatment is controlled, so that it is in the range 10 mTorr to 200 mTorr, typically close to 50 mTorr (1 mTorr being equal to 1.33×10^{-1} Pa).

The plasma is initiated then maintained by applying RF (radiofrequency) power in the range 100 W to 2000 W,
15 preferably close to 250 W in the case of 200 mm diameter substrates and in the range 100 W to 3000 W, preferably close to 500 W in the case of 300 mm diameter substrates.

The surface of the face to be bonded is then exposed to the plasma for about 5 to 60 seconds, preferably 10 to
20 30 seconds.

It is also appropriate to limit the exposure time for the plasma treatment to what is strictly necessary.

Preferably, this is less than one minute, or better still less than 30 seconds. Prolonged exposure would
25 risk causing an accumulation of electric charges in the insulator and an increase in the charge density of the insulator (QBOX), which will counter the improvements in electrical performances discussed in the introduction.

30 Lifting off the back portion of the source substrate:

Said lifting may, for example, be carried out by grinding and/or polishing.

In a variation, said back portion is lifted off by forming a zone of weakness.

35 This variation is illustrated in Figures 3A to 3G, in which elements identical to those described above carry the same reference numerals.

The zone of weakness 22 formed inside the source substrate 2 delimits the active layer 21 from a back portion 23.

5 The zone 22 may be formed by a porous zone; in this regard, reference should be made to the article by K. Sakaguchi et al, "*Eltran® by splitting porous Si layers*", The ElectroChemical Society Inc PV99-3, Silicon-on-insulator technology and devices, P.L. Hemment, pp 117-121.

10 However, the zone 22 is advantageously formed by implantation of light atomic species, preferably hydrogen and/or helium ions, so as not to deteriorate the oxide 32 (see Figure 2C).

15 Reference regarding implantation conditions should be made to the article by C. Maleville and C. Mazuré, "*Smart Cut™ technology: from 300 nm ultrathin SOI production to advanced engineered substrates*", Solid State Electronics 48 (2004), 1055-1063, which describes the SmartCut™ method used here.

20 When atomic species implantation is used, this is carried out after the recovery heat treatment of Figure 3B.

25 The step for detachment of the back portion 23 along the zone 22 consists of applying stress of thermal or mechanical origin, for example an anneal treatment or introducing a blade to said zone of weakness 22.

Two particular implementations will now be described.

30 EXAMPLE 1: Preparation of a substrate the active layer of which comprises a ground plane (known by the acronym "GP-SOI", or "ground plane silicon on insulator")

This example will be described with reference to Figures 3A to 3G.

35 A silicon support substrate 1 was covered with a deposit of a thin layer 60 about 1 μm [micrometer] thick,

highly doped with boron (see Figures 3A and 3B), to define a ground plane therein.

This highly doped layer had a front face 600 for bonding (see Figure 3C). It was polished or smoothed to
5 reduce the roughness of said surface 600 and render it compatible with bonding.

As shown in Figure 3D, the support substrate 1 covered with the doped layer 60 then underwent a high temperature thermal annealing treatment (RTA), typically
10 at 1050°C for about 10 seconds.

Further, a silicon source substrate 2 was used, oxidized by dry oxidation, to cover it with a layer 32 of SiO₂ about 50 nanometers (50 nm) thick.

The layer 32 then underwent an FGA type recovery
15 treatment, at 450°C, for about 1h30, (see Figure 3B). The oxide 32 had DIT values of several 10¹⁰.eV⁻¹.cm⁻².

As can be seen in Figure 3C, the substrate 2 underwent hydrogen ion implantation using a dose of
20 5.5 × 10¹⁶ H⁺/cm², and an implantation energy of 37 keV, to define the zone of weakness 22.

The free surface 320 of the oxide layer 32 underwent plasma activation (Figure 3E). The substrate 2 was 300 mm diameter, and the following parameters were used:
25 oxygen plasma, 200 sccm flow rate, 500 W power, 50 mTorr pressure, for 30 seconds.

After bonding by molecular bonding (Figure 3F) and detachment of the back portion of the source substrate by heat treatment close to 500°C for a short period, the composite substrate shown in Figure 3G was obtained. It
30 should be noted that the post-bonding heat treatment was deliberately limited to prevent any boron from diffusing into the oxide or into the active layer, which would run the risk of reducing the electrical performance.

Said composite substrate had DIT values of several
35 10¹⁰.eV⁻¹.cm⁻².

EXAMPLE 2: Preparation of a composite substrate
comprising an active layer of silicon on a stack of oxide
and quartz

5 The same source substrate 2 as that used in Example
1 was employed and it underwent the same treatments, with
the exception of the recovery treatment which was carried
out by a high temperature anneal at 1100°C, and the
formation of the zone of weakness was carried out by co-
implantation of helium ($1.5 \times 10^{16} \text{ He}^+/\text{cm}^2$) and hydrogen
10 ($1 \times 10^{16} \text{ H}^+/\text{cm}^2$).

Further, a quartz support substrate 1 was used the
front face 10 of which underwent plasma activation using
the parameters used in Example 1 for substrate 2.

15 The composite substrate obtained had DIT values at
the interface between the oxide and the silicon of the
order of several $10^{10} \text{ eV}^{-1}.\text{cm}^{-2}$.

 In accordance with the invention, the fact that the
recovery treatment was carried out systematically prior
to plasma activation meant that the bonding energy was
20 not reduced but the "DIT" values were kept extremely low.
Bonding was thus strong, and subsequent thinning of the
source substrate was facilitated.

CLAIMS

1. A method of fabricating a composite substrate (4) with improved electrical properties, of the type comprising at least one thin insulating layer (32), interposed between
5 a first substrate (1), termed the "support", and a layer of semiconductor material (21), termed the "active layer", characterized in that it comprises, in the following order, the steps of:
- forming or depositing an insulating layer (32) on
10 a second substrate (2), termed the "source substrate", and optionally an insulating layer (31) on said support substrate (1);
 - recovery heat treatment of said insulating layer (32) and optionally of said insulating layer (31) formed
15 on the support substrate (1);
 - plasma activation of at least one of the two faces intended to be bonded together, selected from the front face (320) of the insulating layer (32) of the source substrate (2) and the front face (10) of the support
20 substrate (1) or the front face (310) of the insulating layer (31) of the support substrate (1);
 - bonding, by molecular bonding, said support substrate (1) together with said source substrate (2), such that said insulating layer (32) is located between
25 said support substrate (1) and said source substrate (2); and
 - lifting off a portion (23), termed the "back", of said source substrate (2), to retain only a thickness of material constituting said active layer (21) and to
30 produce said composite substrate (4).
2. A method according to claim 1, characterized in that the recovery heat treatment comprises an FGA type treatment carried out by annealing in an atmosphere of
35 neutral gas and hydrogen, at a temperature in the range 400°C to 600°C, for a period in the range from about thirty minutes to two hours.

3. A method according to claim 1 or claim 2,
characterized in that the recovery heat treatment
comprises a heat treatment at a temperature of more than
5 900°C, in a neutral gas atmosphere, optionally in the
presence of oxygen, for about 30 minutes to 1 hour.

4. A method according to claim 2 or claim 3,
characterized in that the recovery heat treatment
10 comprises a RTA type heat treatment carried out for
several seconds to several minutes, approximately.

5. A method according any preceding claim, characterized
in that the plasma activation treatment consists in
15 introducing the substrate to be treated into an
activation chamber and exposing it therein for about 5
seconds to 60 seconds to a plasma formed from a pure gas
selected from oxygen (O₂), nitrogen (N₂), argon (Ar) and
helium (He) or a mixture of said gases, said gas being
20 introduced into the chamber at a flow rate in the range
10 sccm to 1000 sccm, the established pressure in the
chamber being in the range 10 mTorr to 200 mTorr, the
plasma being initiated then maintained by applying
radiofrequency power in the range 100 W to 3000 W.

25

6. A method according any preceding claim, characterized
in that the insulating layer (31, 32) is an oxide.

7. A method according to any one of claims 1 to 5,
30 characterized in that the insulating layer (31, 32) is a
high permittivity dielectric material.

8. A method according to claim 7, characterized in that
the high permittivity dielectric material is selected
35 from the group consisting of hafnium dioxide (HfO₂),
yttrium oxide (Y₂O₃), strontium and titanium trioxide
(SrTiO₃), alumina (Al₂O₃), zirconium dioxide (ZrO₂),

tantalum pentoxide (Ta_2O_5), titanium dioxide (TiO_2), their nitrides and their silicides.

5 9. A method according any preceding claim, characterized in that the back portion (23) of the source substrate (2) is lifted off by grinding and/or polishing.

10 10. A method according to any one of claims 1 to 8, characterized in that it comprises forming a zone of weakness (22) inside the source substrate (2) prior to the plasma activation step and lifting off the back portion (23) of the source substrate (2), by detachment along said zone of weakness (22).

15 11. A method according to claim 10, characterized in that the zone of weakness (22) is obtained by atomic species implantation inside the source substrate (2).

20 12. A method according any preceding claim, characterized in that said active layer (21) is produced from a material selected from silicon, germanium and strained silicon.

25 13. A method according any preceding claim, characterized in that the method includes a step of doping all or part of one of the source (2) or support (1) substrates.