CHIP SELF-TEST METHOD AND APPARATUS, STORAGE MEDIUM, AND ELECTRONIC DEVICE

ABSTRACT

The present disclosure relates to the technical field of chips, and provides a chip self-test method and apparatus, a storage medium, and an electronic device. The method is applied to an integrated circuit including a first processor. The method includes: writing self-test information from a non-volatile memory into a tightly-coupled memory; writing the self-test information from the tightly-coupled memory into a register of a self-test control unit; and in response to the register of the self-test control unit being updated with the self-test information, sending, by the self-test control unit, a first test instruction to the first processor to be self-tested, so as to trigger, based on the first test instruction, the first processor to enter a self-test mode.

(FIG. 2)