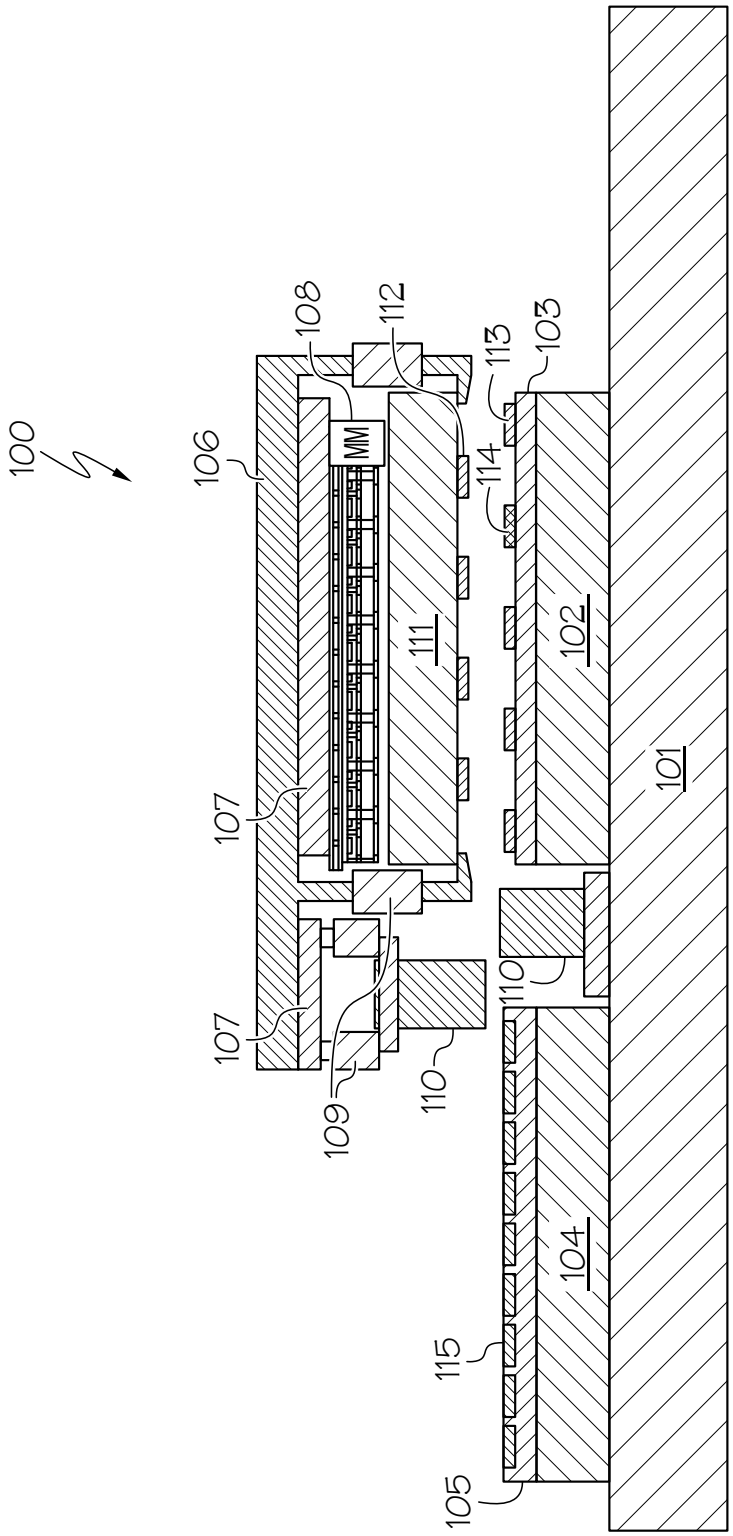
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FIG. 1

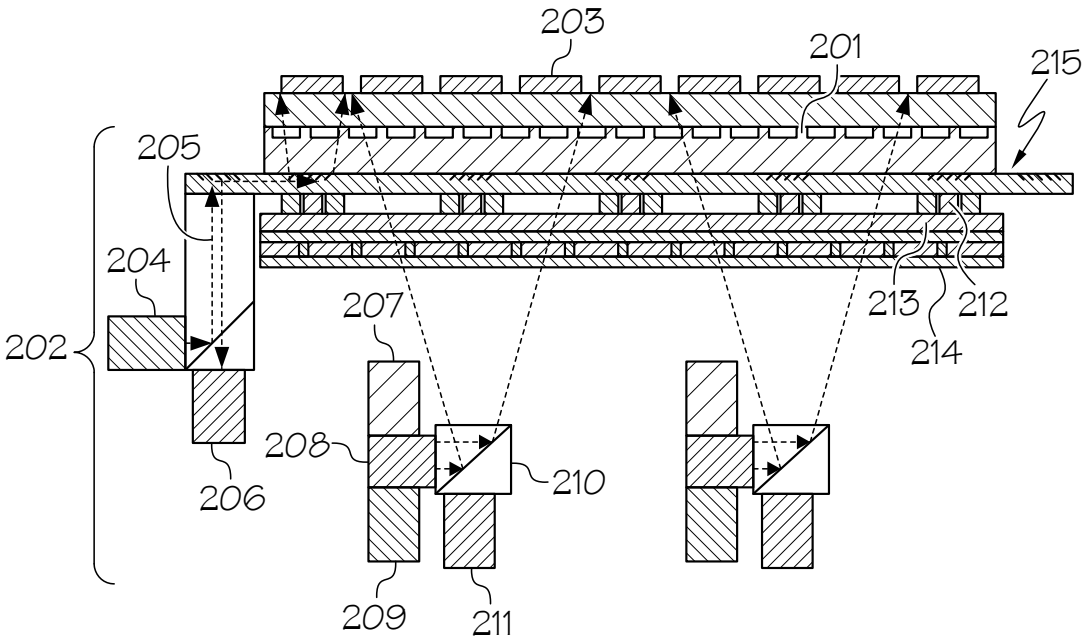
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FIG. 2A

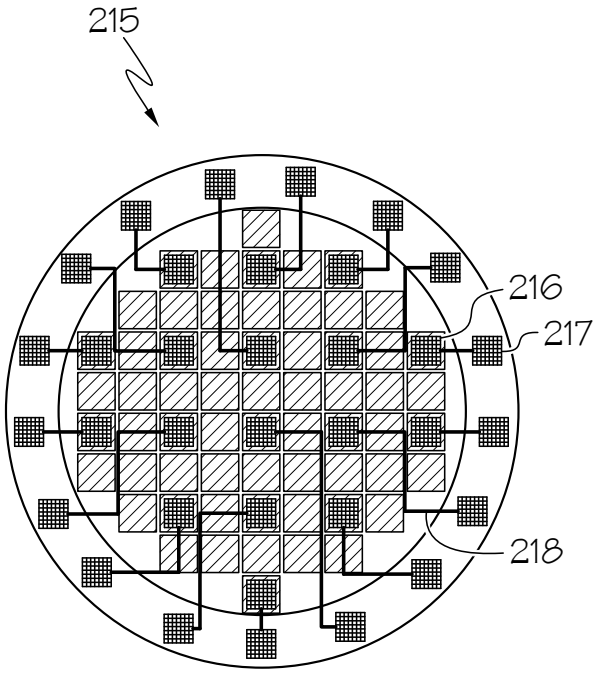
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FIG. 2B

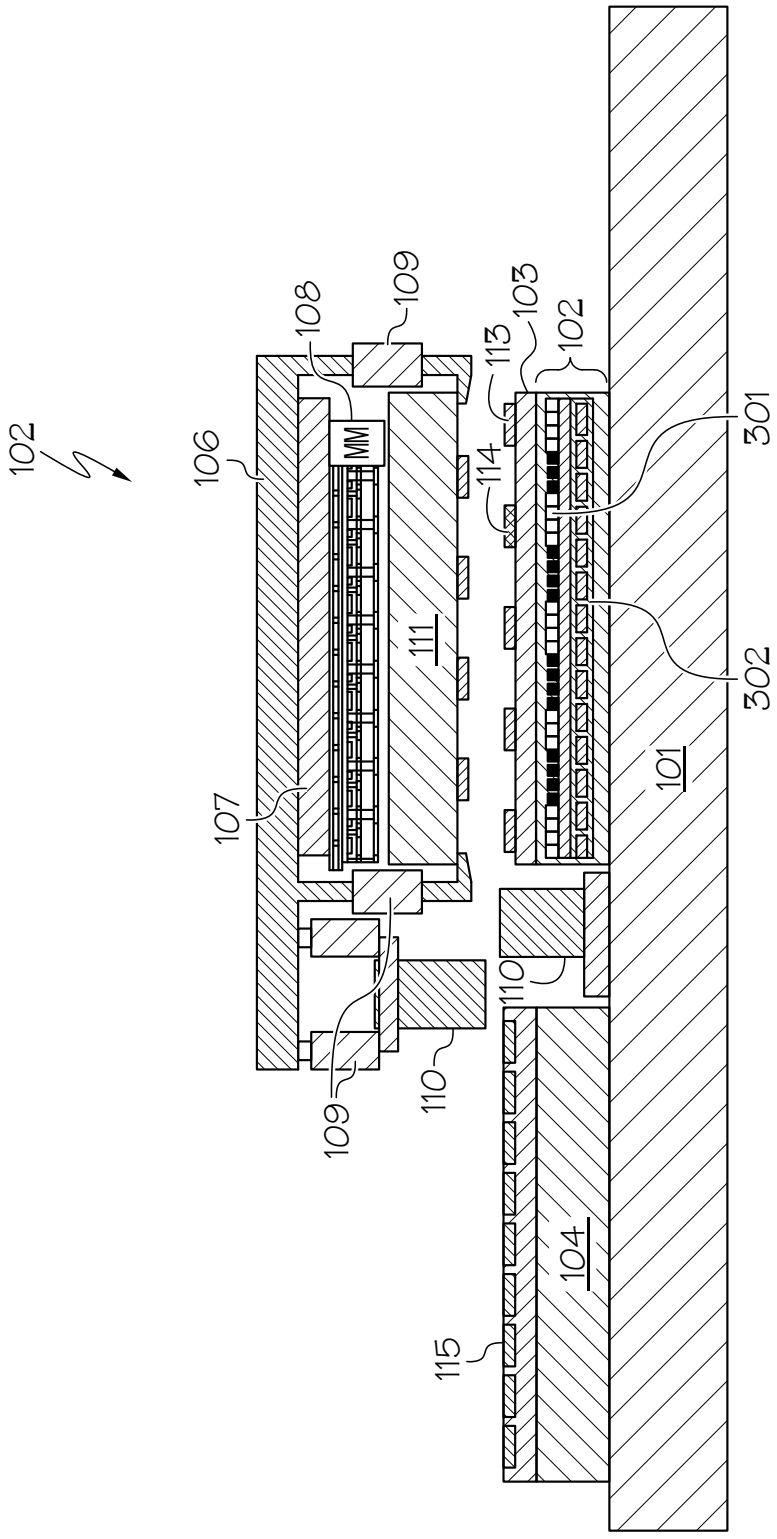
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FIG. 3

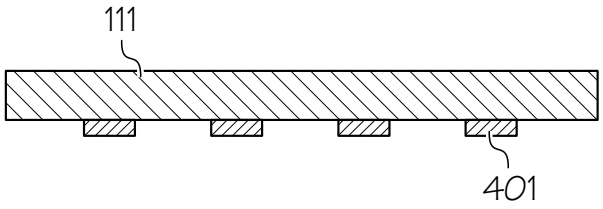
111
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FIG. 4A

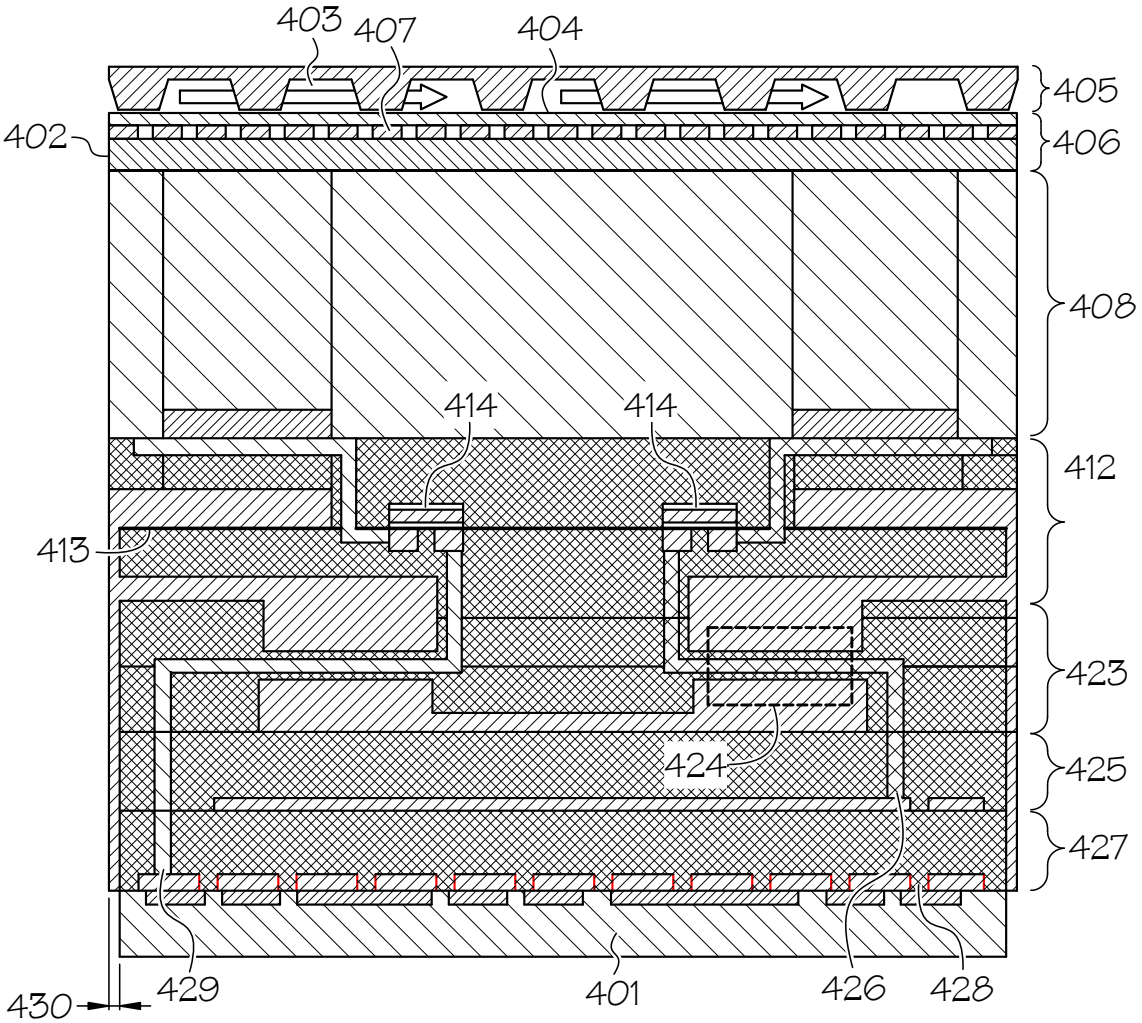
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FIG. 4B

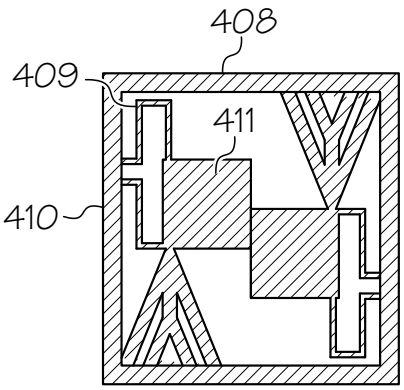


FIG. 4C

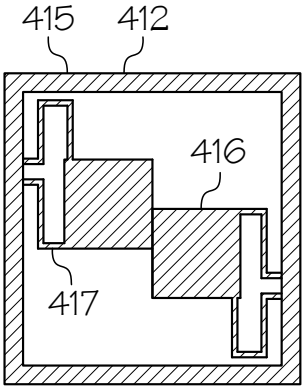


FIG. 4D

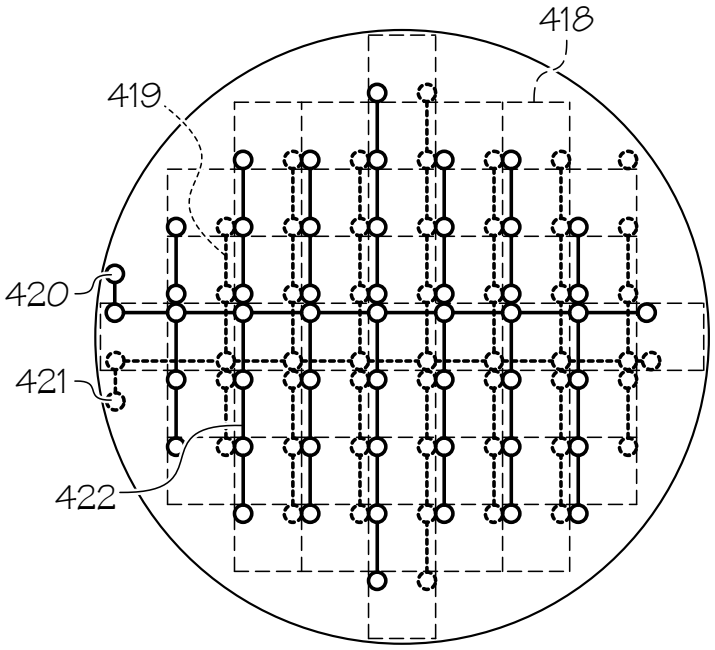
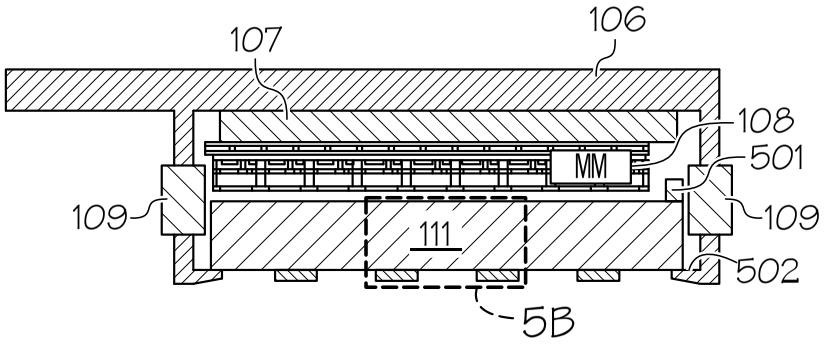


FIG. 4E


107
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501
MM
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502
5B

FIG. 5A

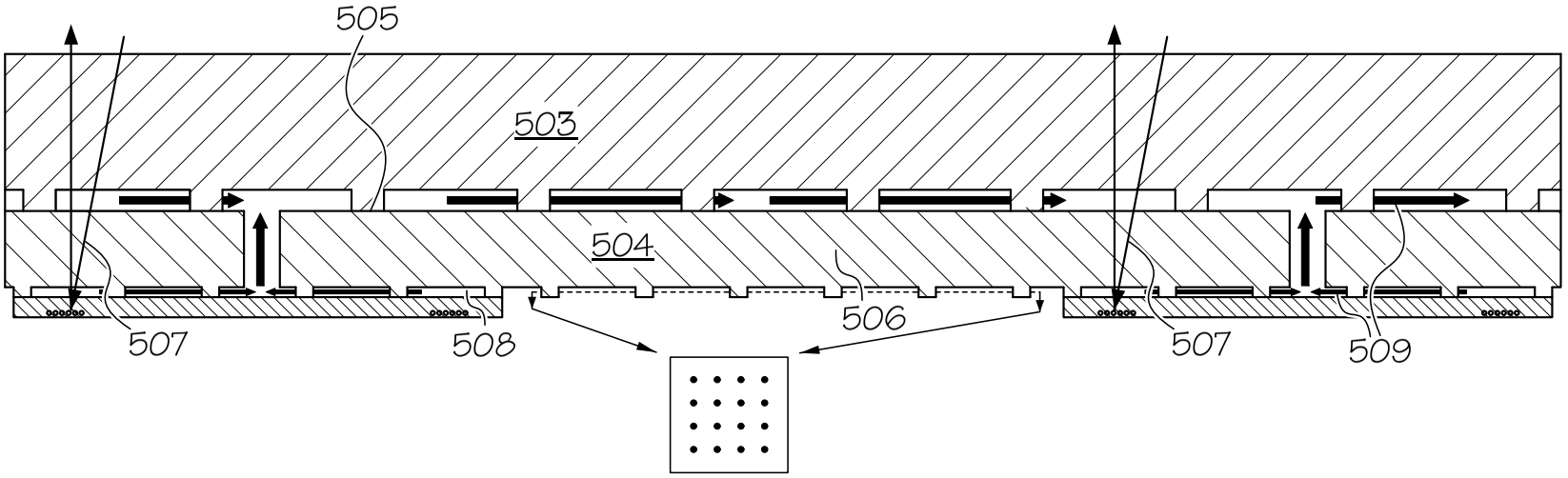
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FIG. 5B

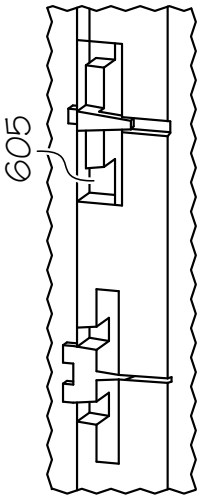


FIG. 6C

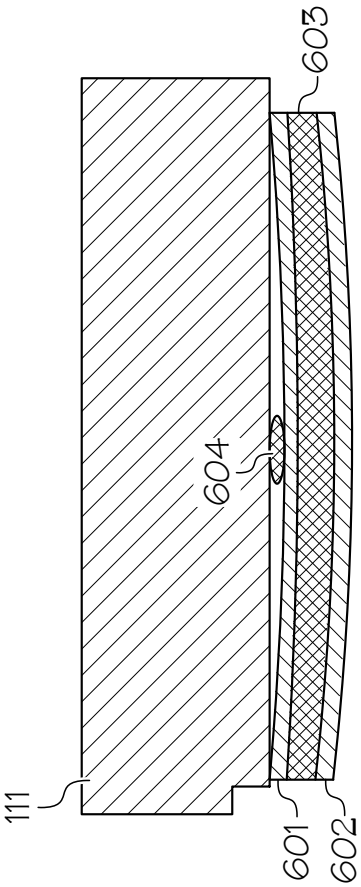


FIG. 6A

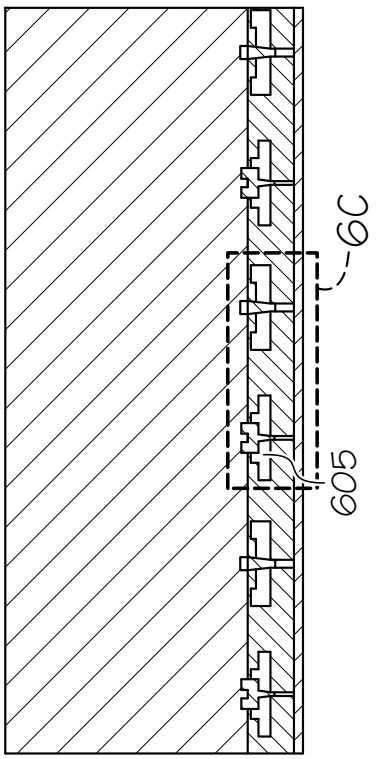


FIG. 6B

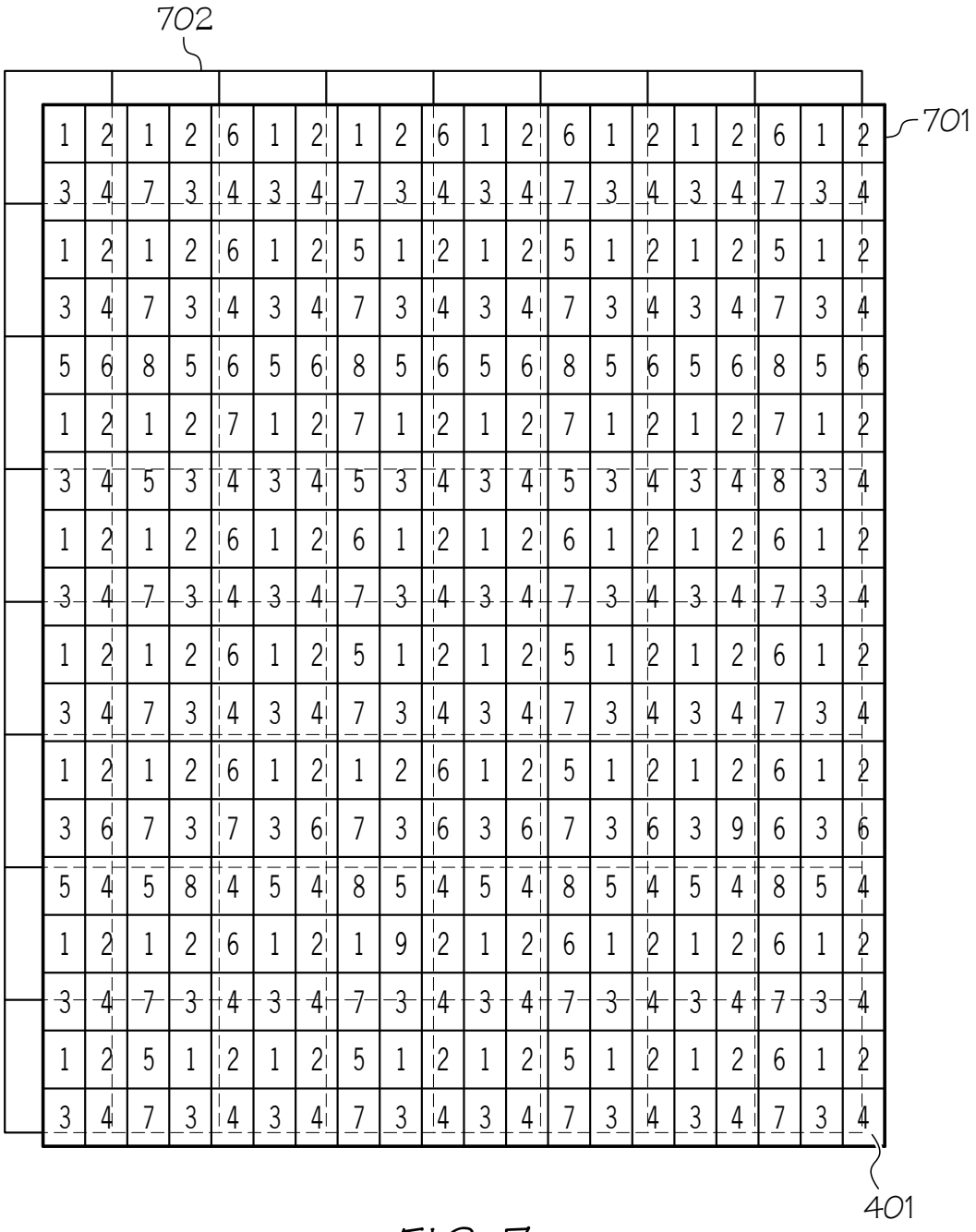
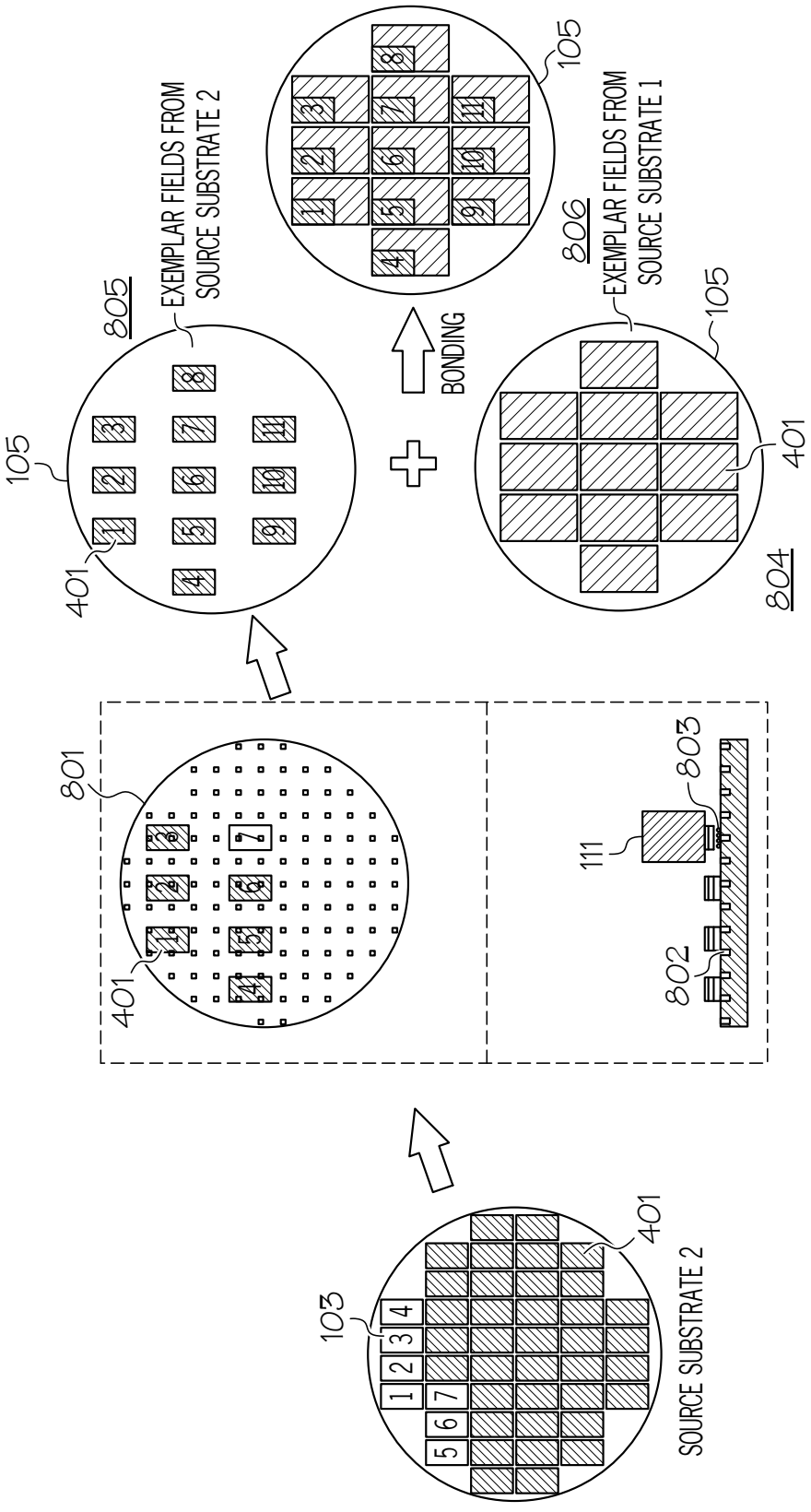


FIG. 7


103
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111
803
802
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EXEMPLAR FIELDS FROM SOURCE SUBSTRATE 2
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401
BONDING
806
EXEMPLAR FIELDS FROM SOURCE SUBSTRATE 1
105
401
804

FIG. 8

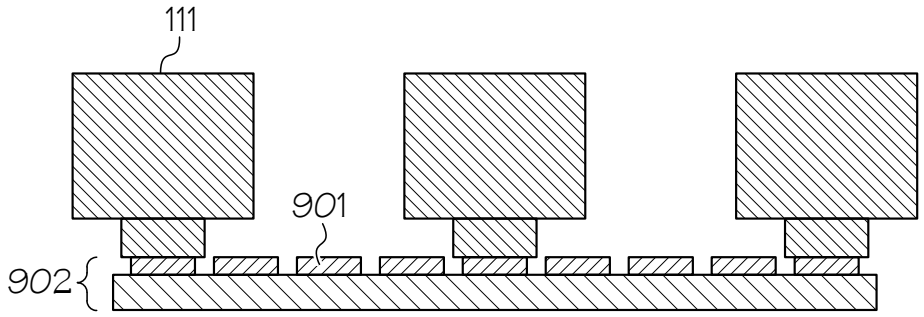


FIG. 9

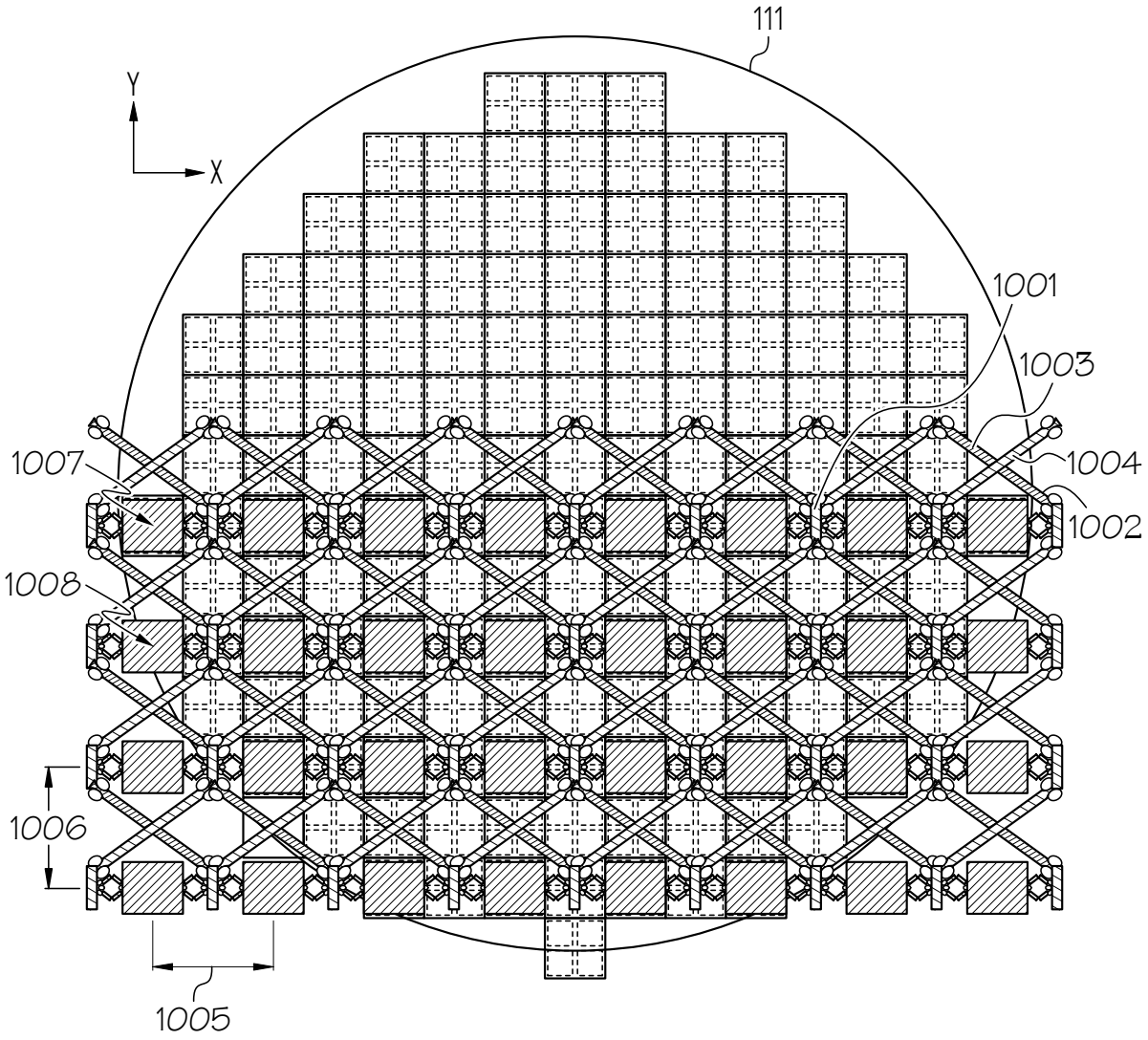


FIG. 10

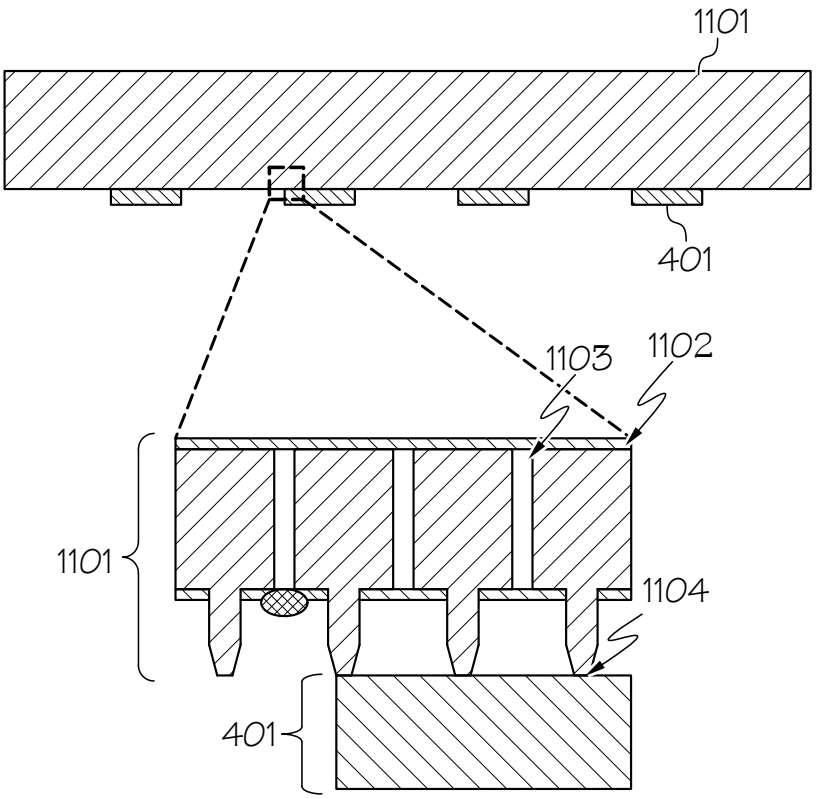


FIG. 11A

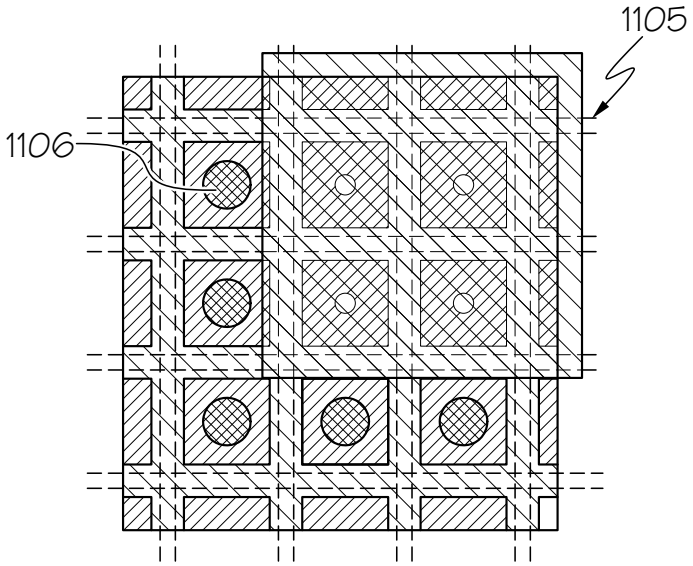


FIG. 11B

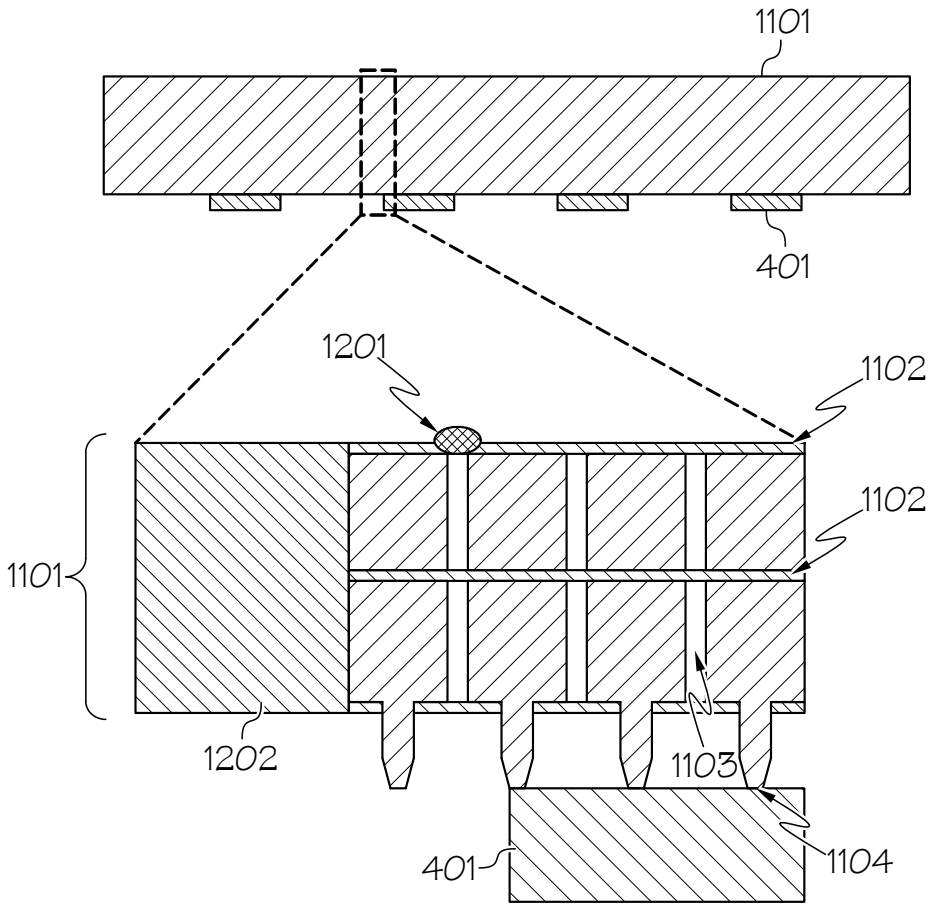


FIG. 12A

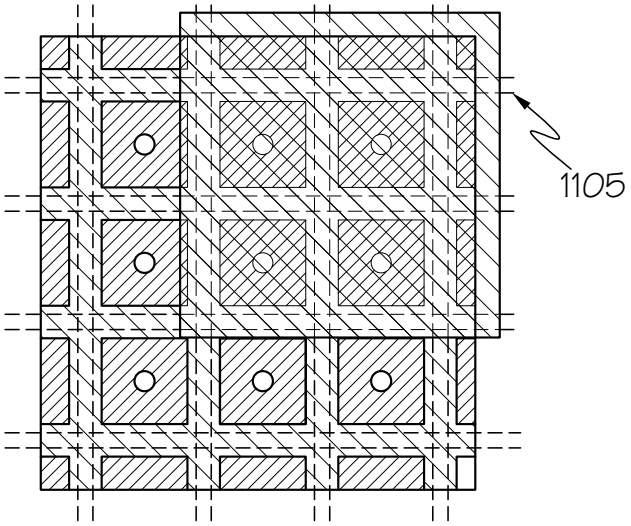


FIG. 12B

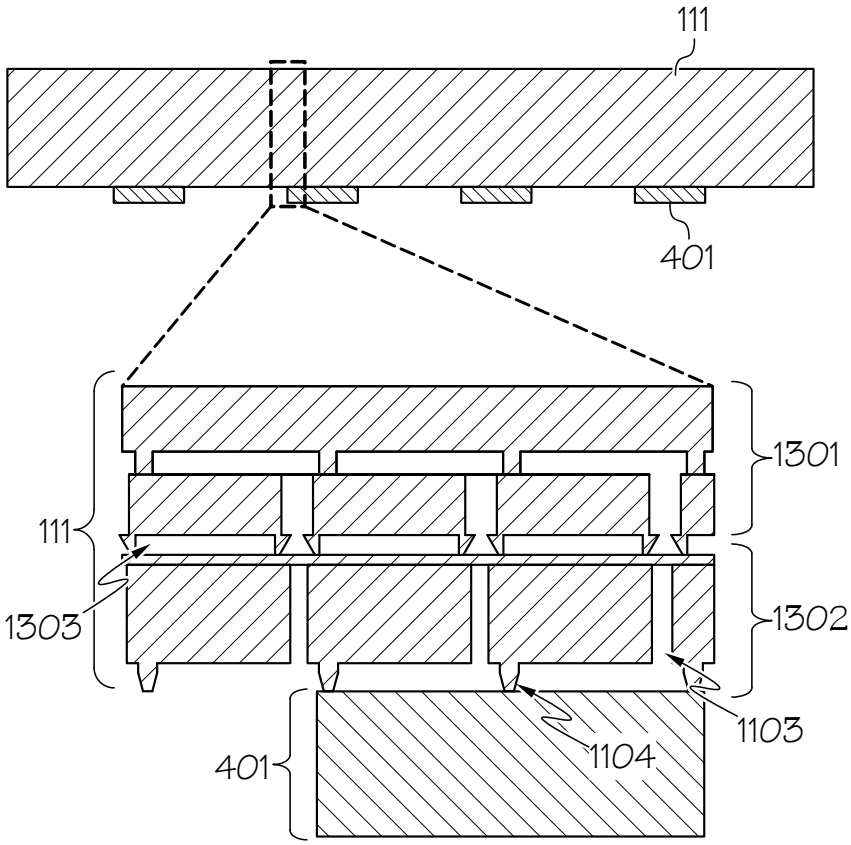


FIG. 13A

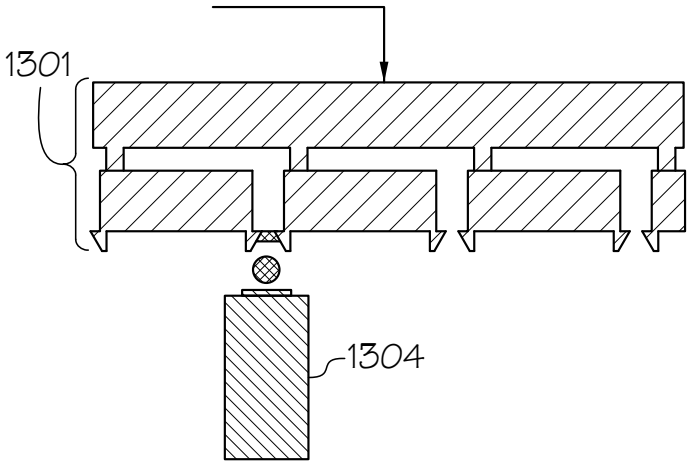


FIG. 13B

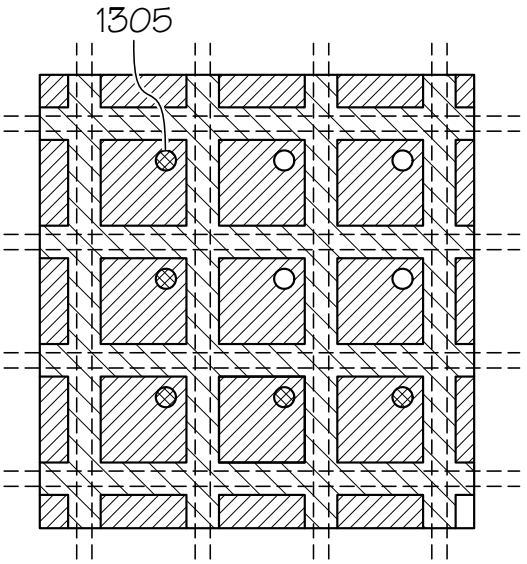


FIG. 13C

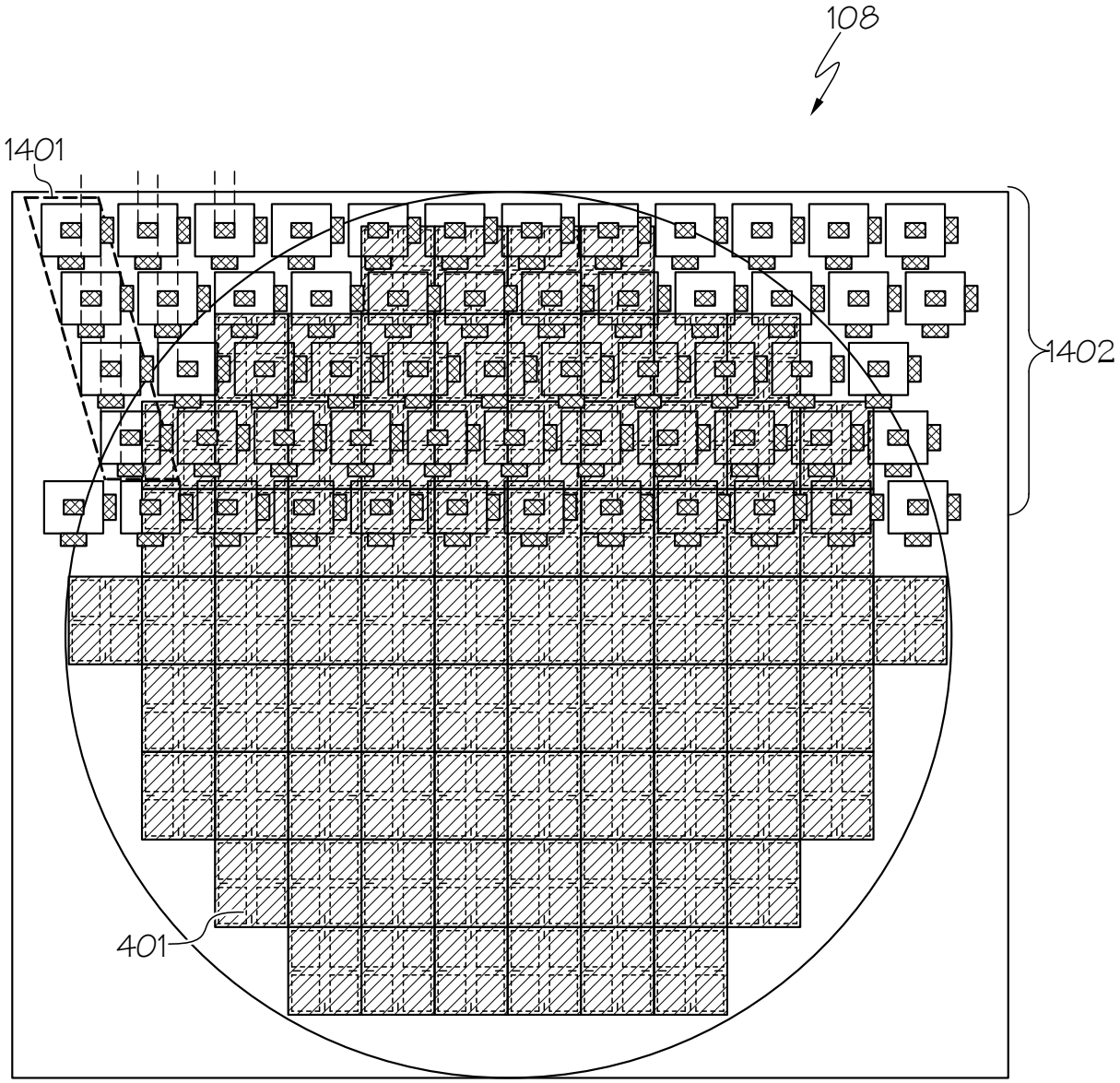


FIG. 14

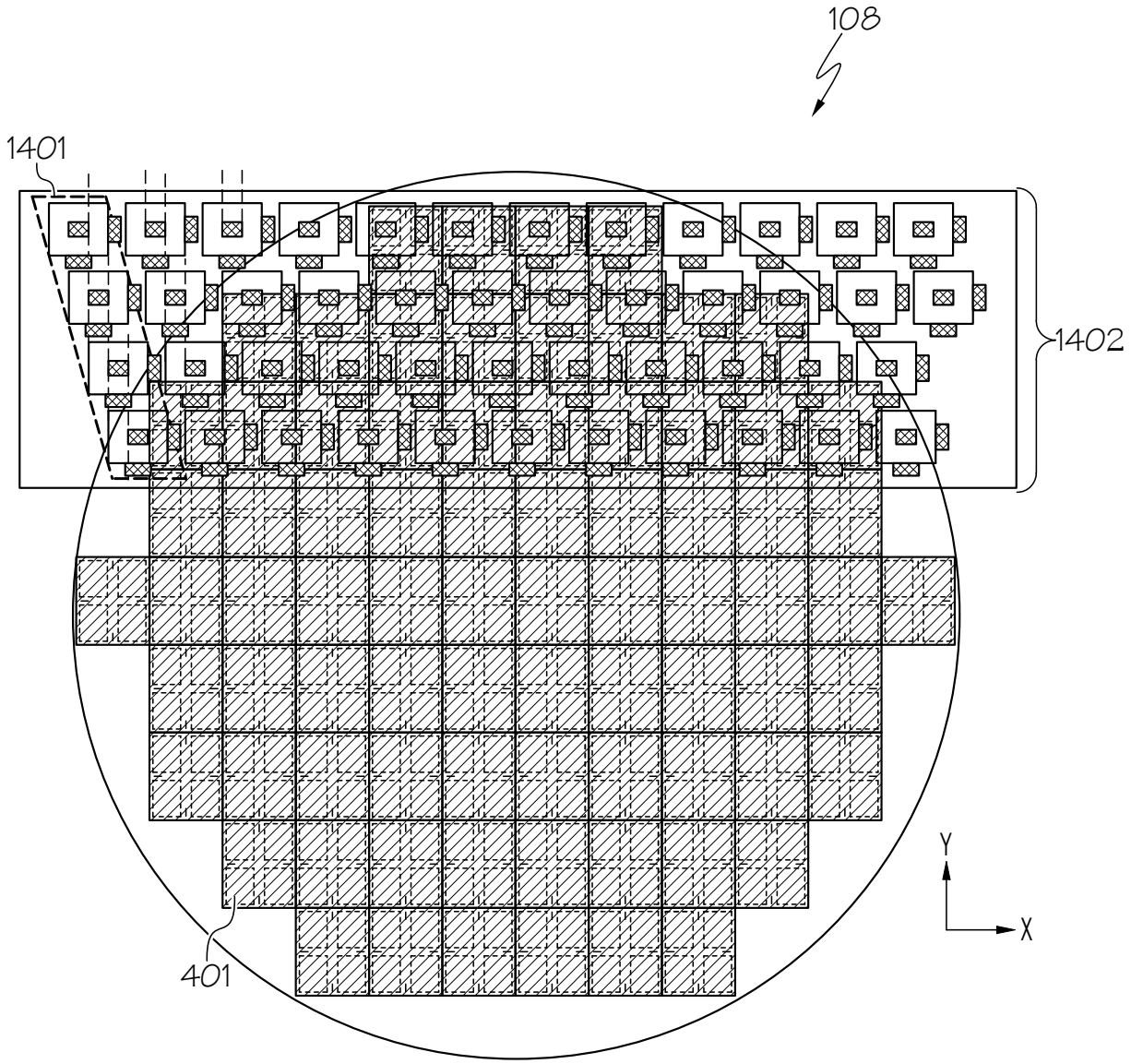


FIG. 15

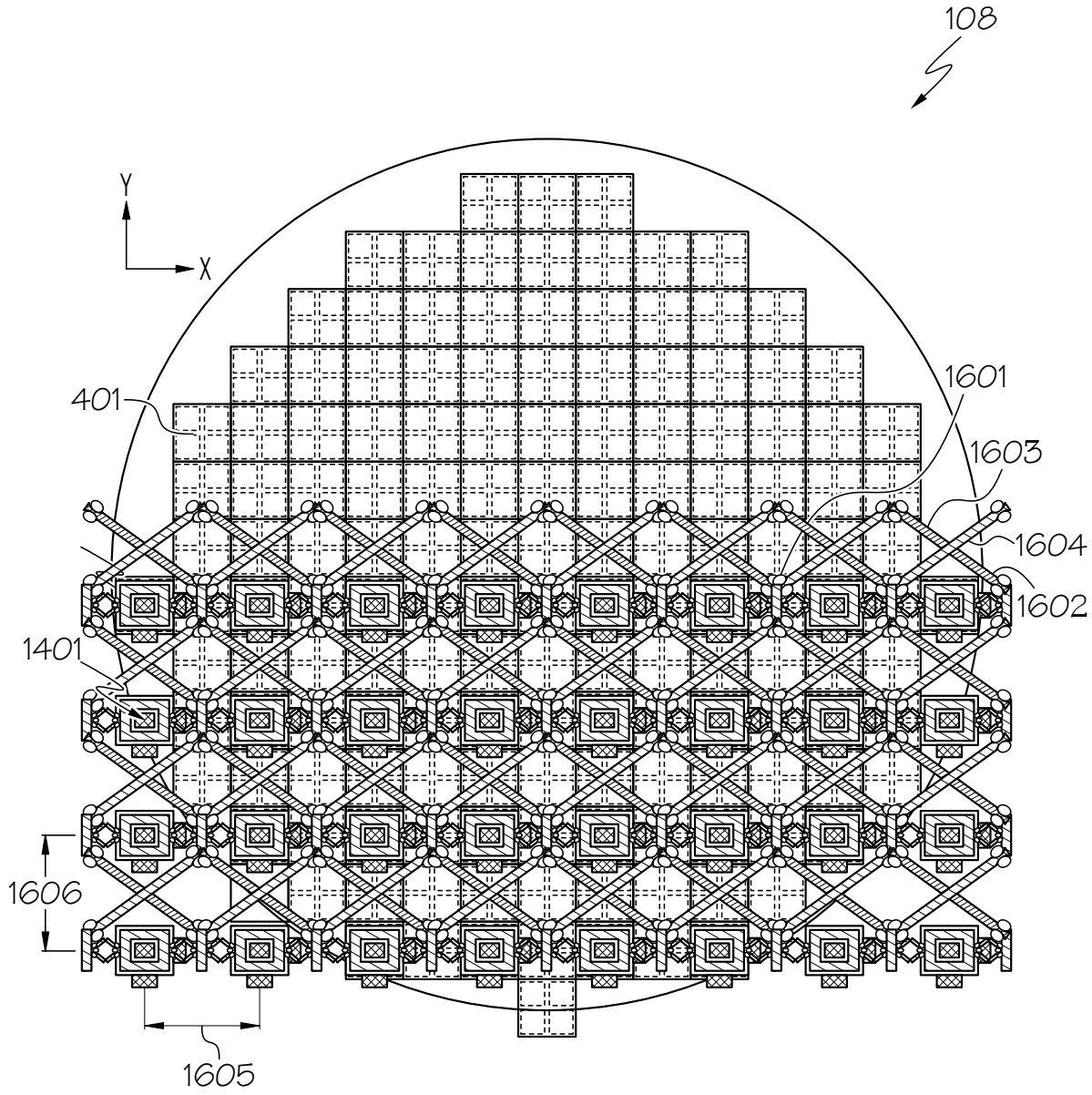


FIG. 16

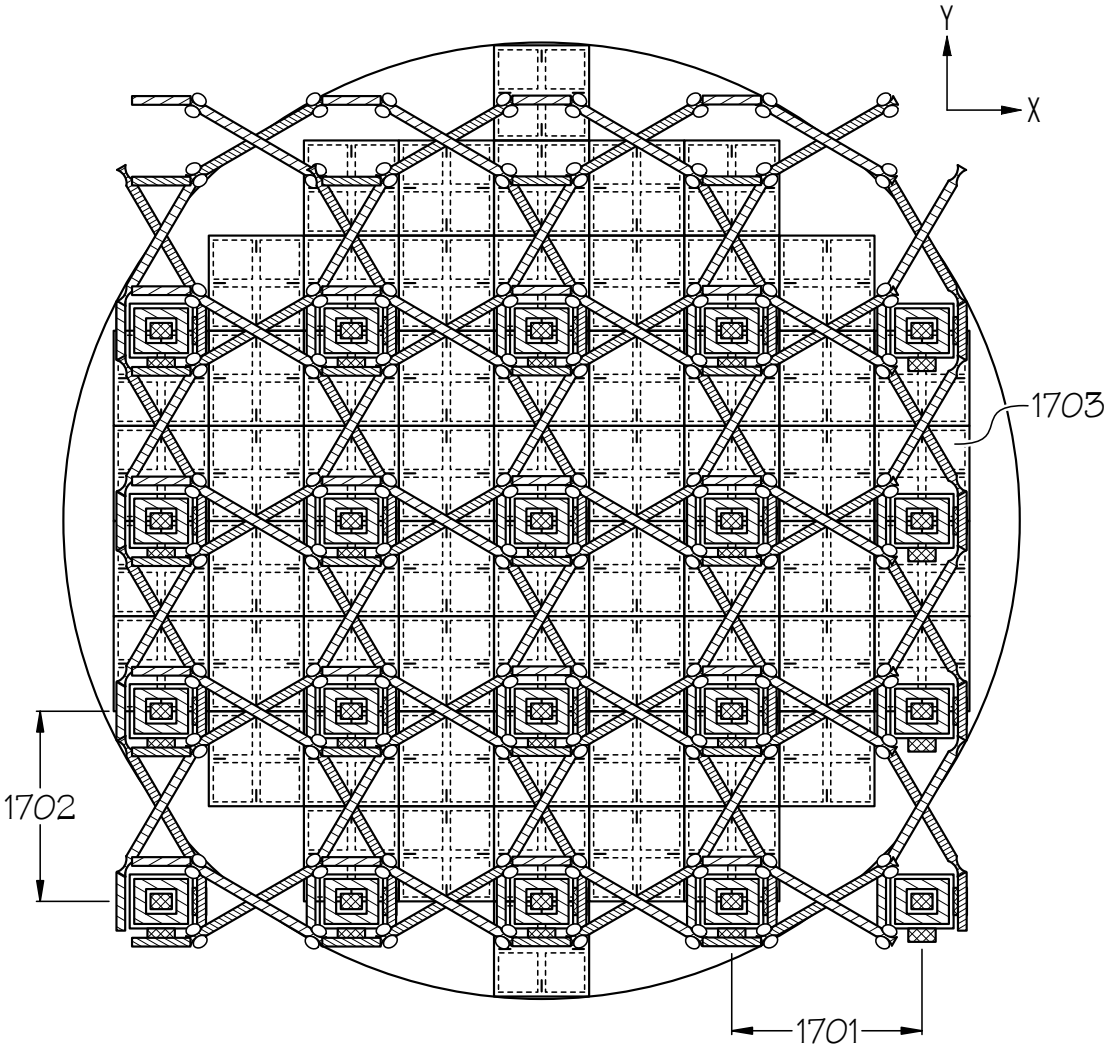


FIG. 17

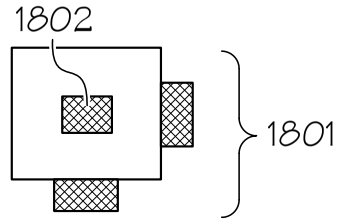


FIG. 18A

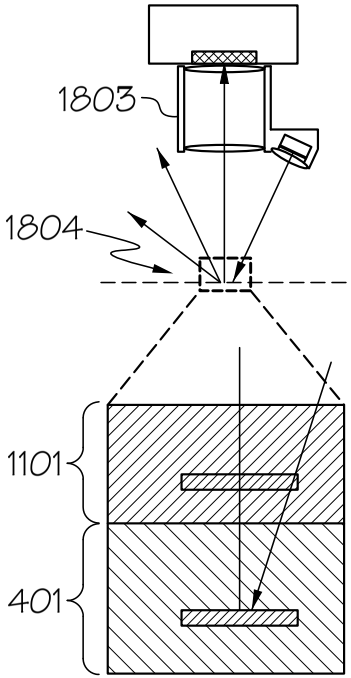


FIG. 18B

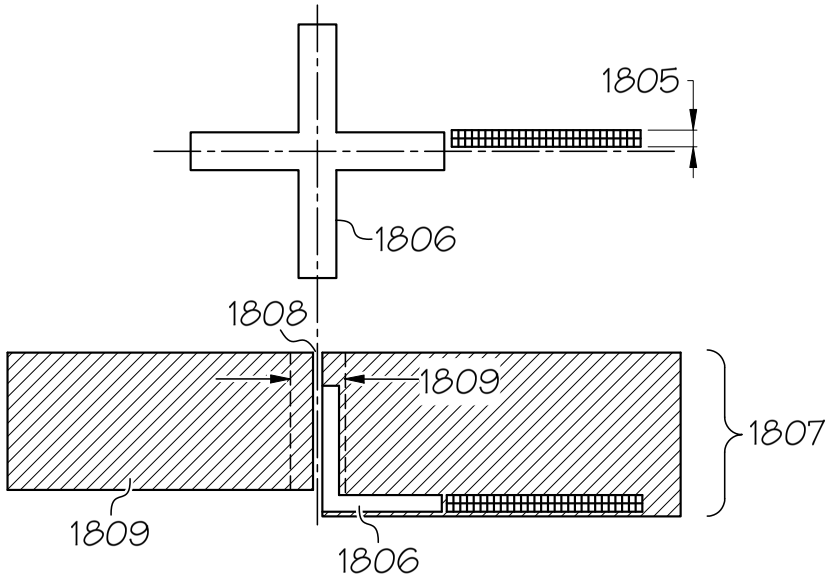


FIG. 18C

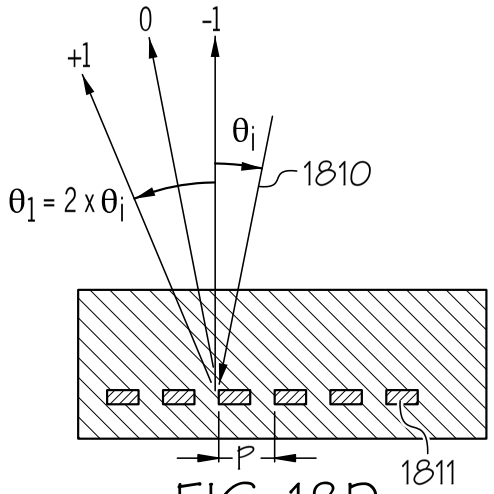


FIG. 18D

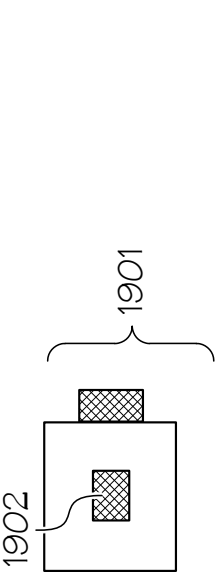


FIG. 19A

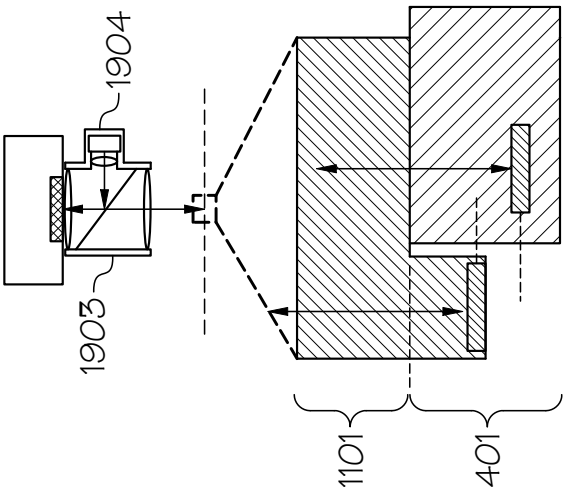


FIG. 19B

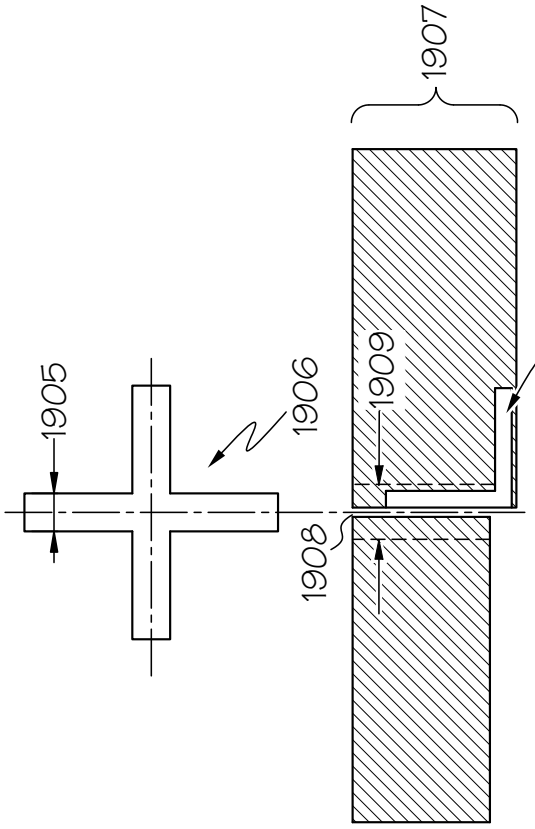


FIG. 19C

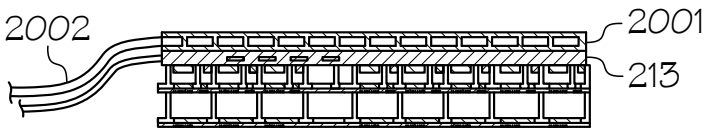


FIG. 20A

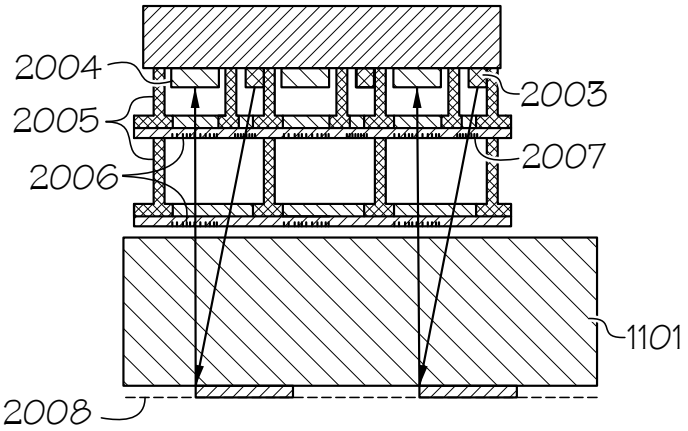


FIG. 20B

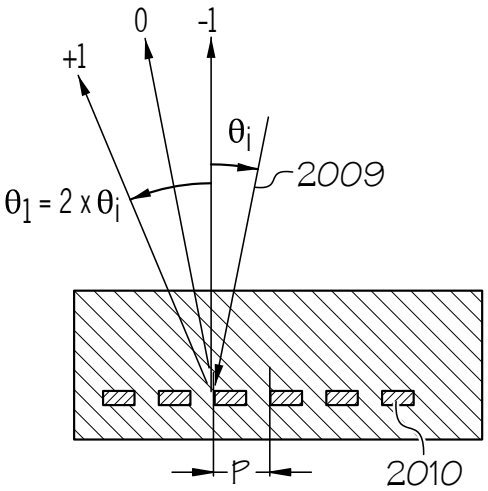


FIG. 20C

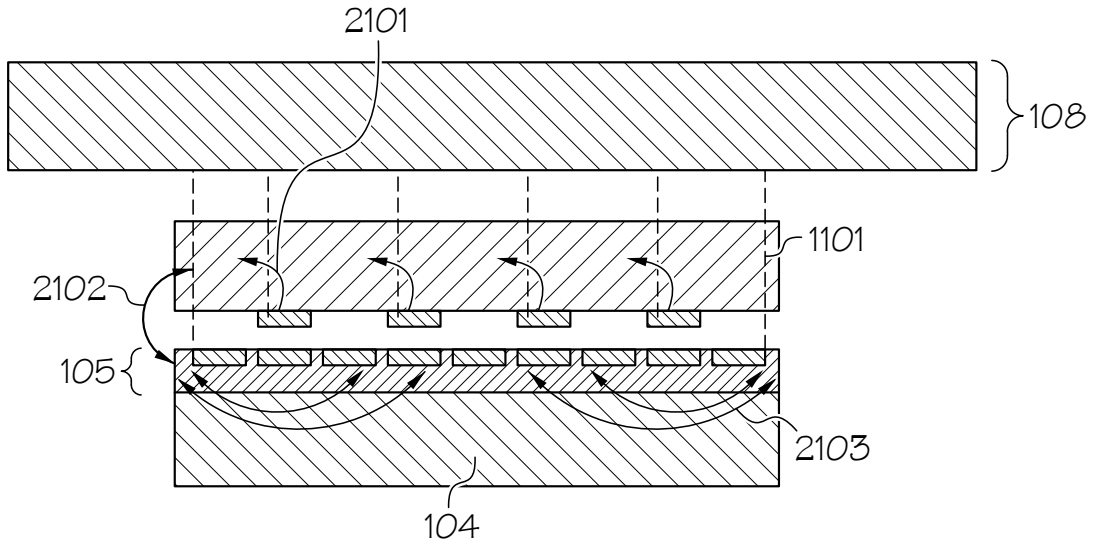


FIG. 21

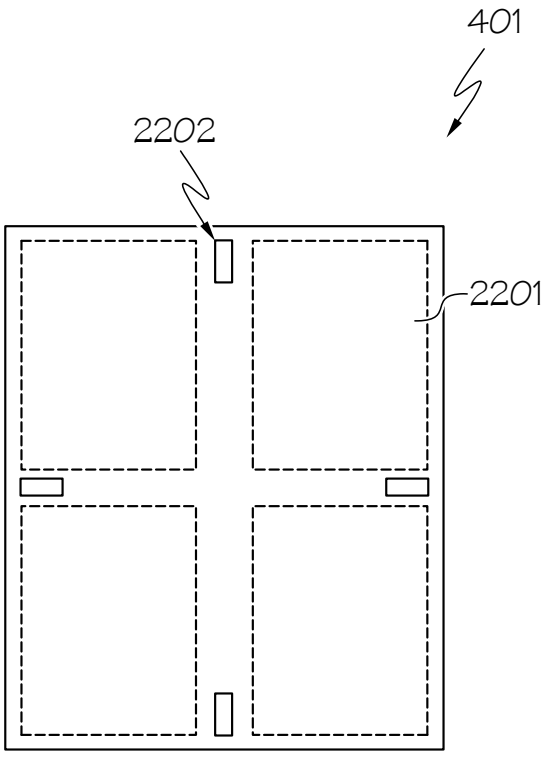


FIG. 22

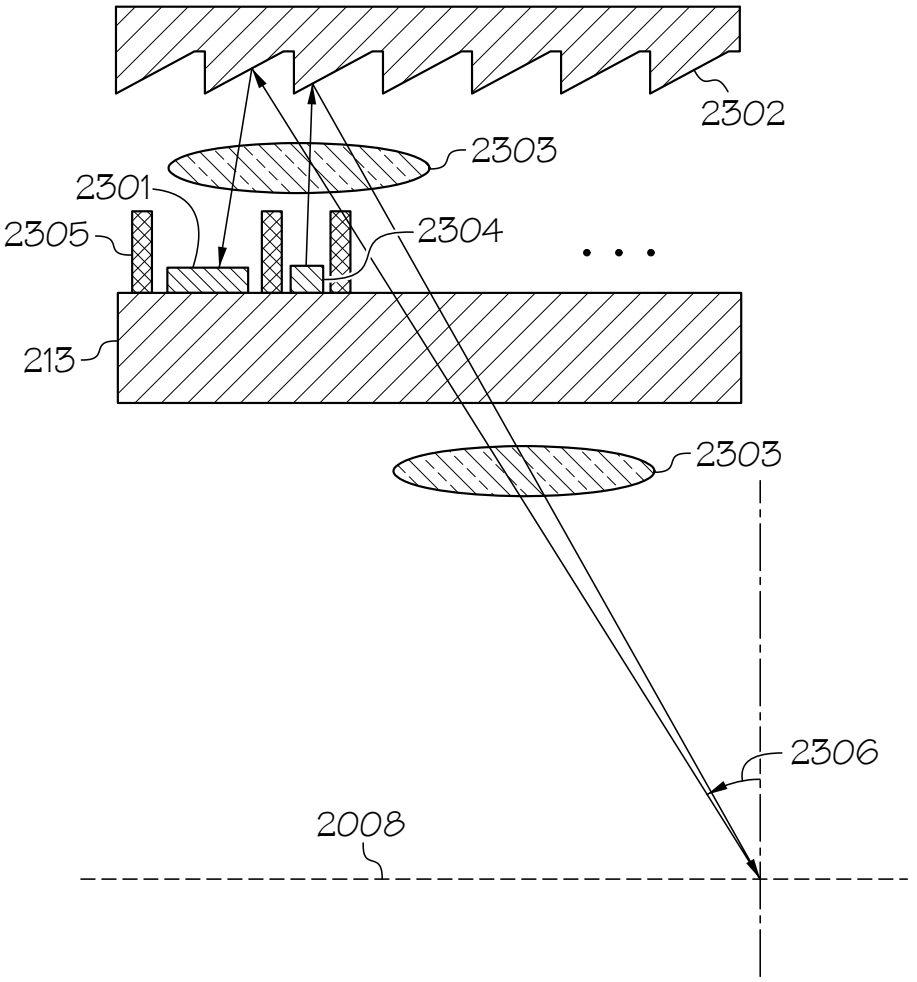


FIG. 23

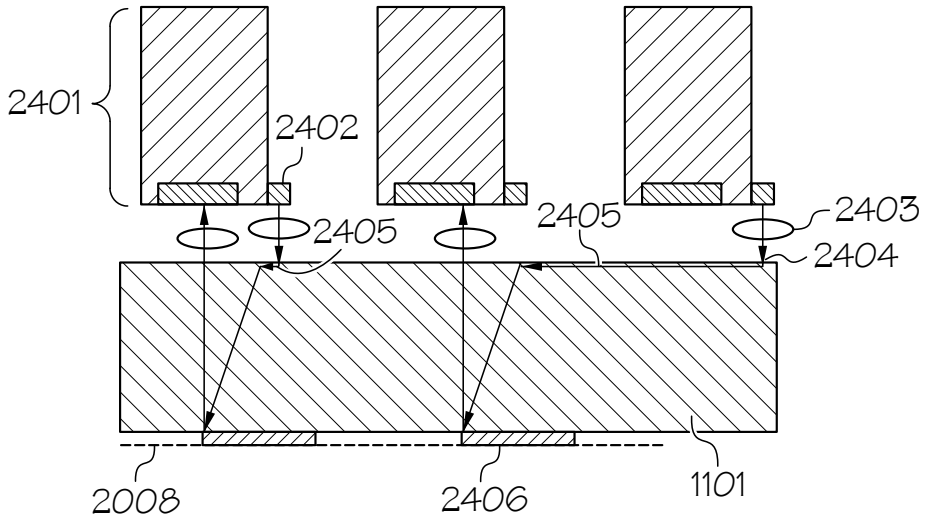


FIG. 24

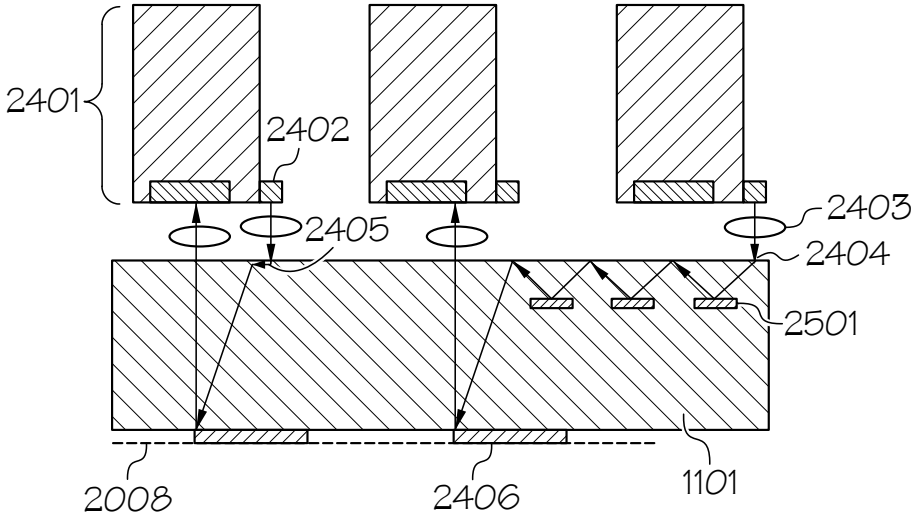


FIG. 25

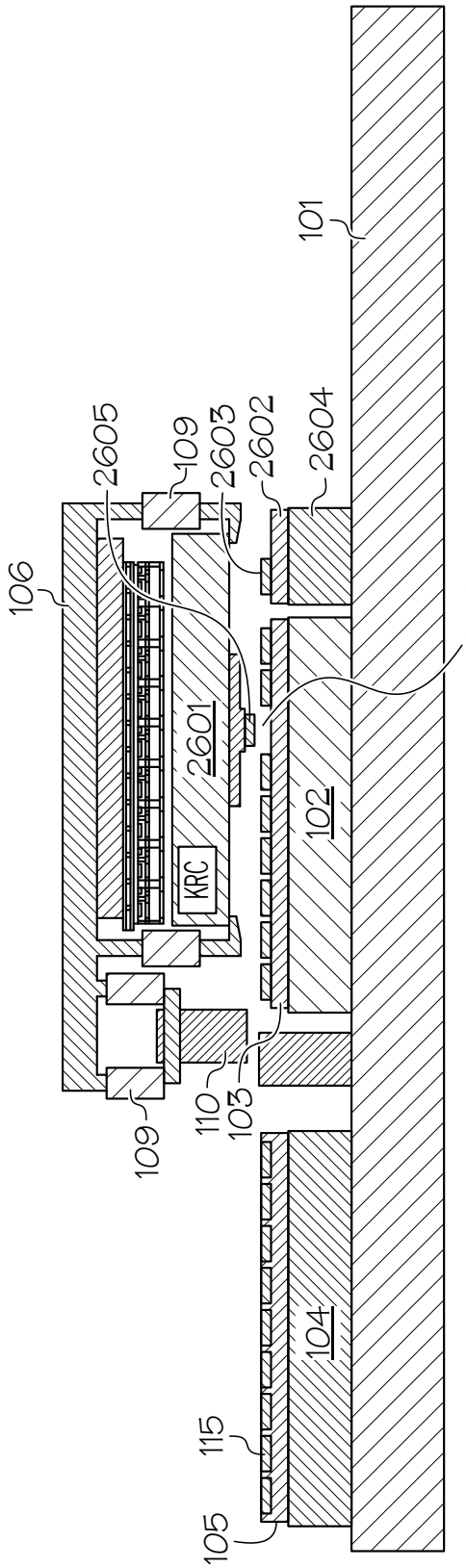


FIG. 26A

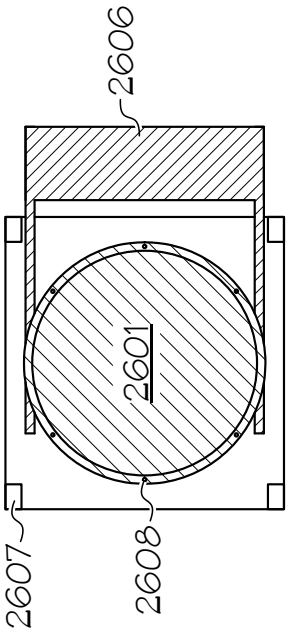


FIG. 26B

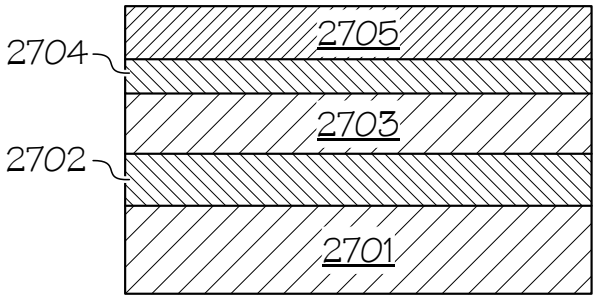


FIG. 27A

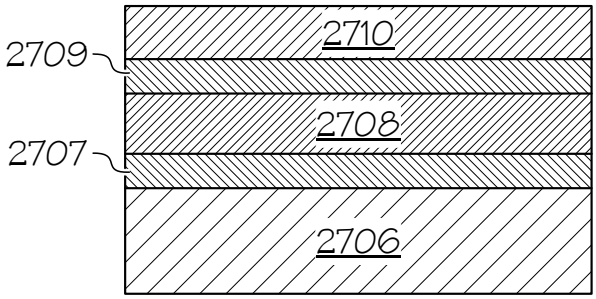


FIG. 27B

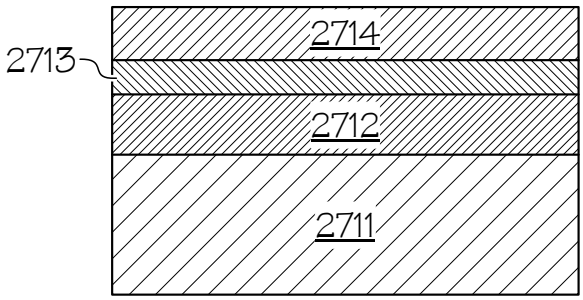


FIG. 27C

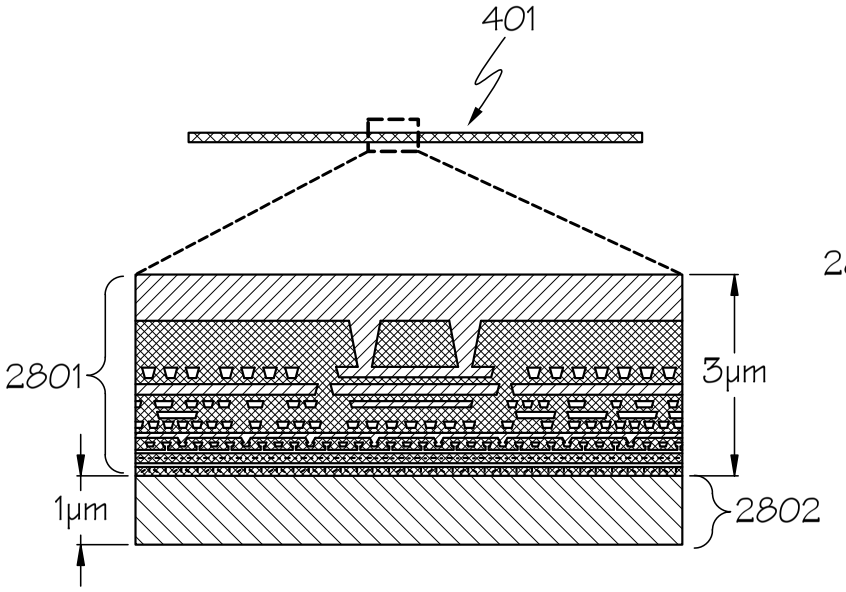


FIG. 28A

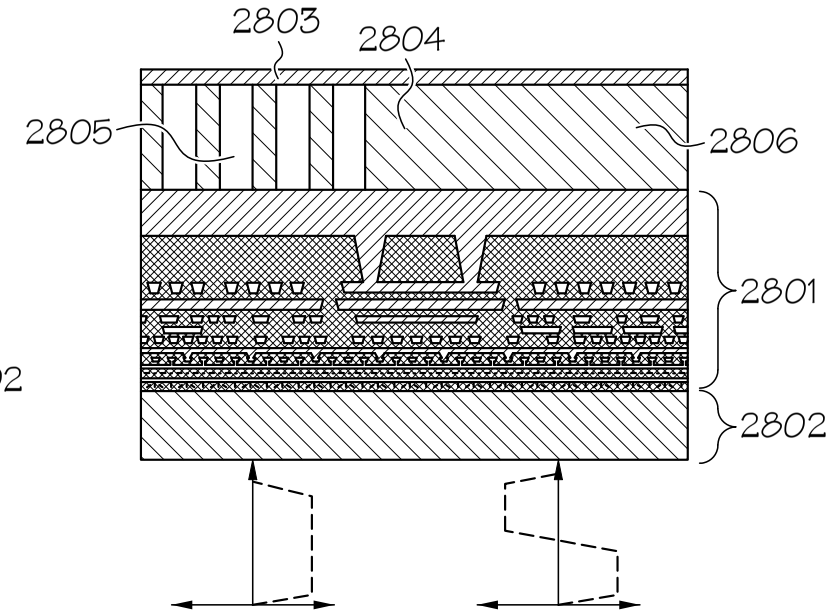


FIG. 28B

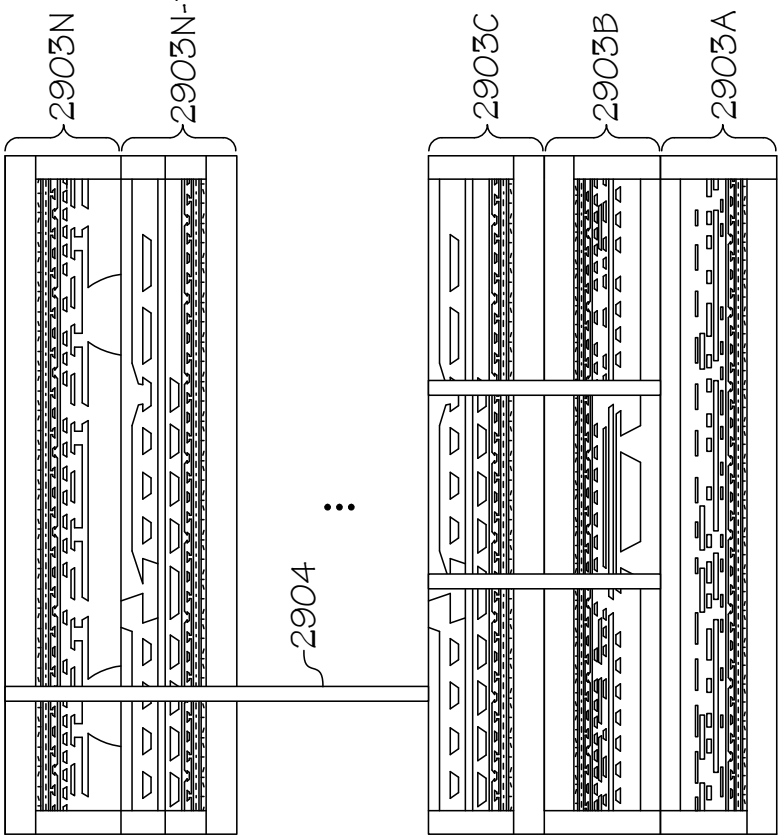


FIG. 29B

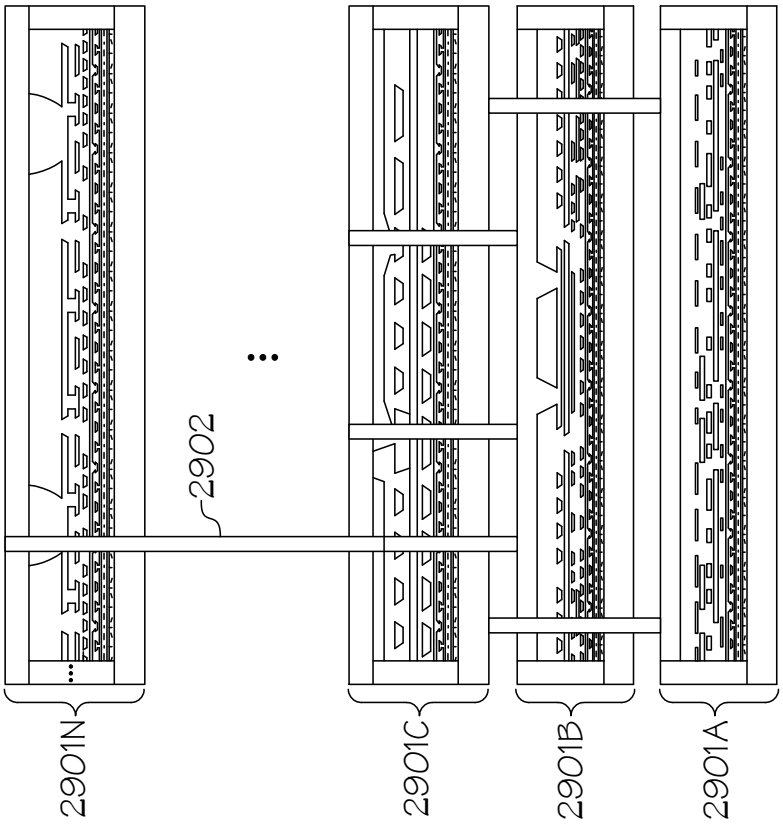


FIG. 29A

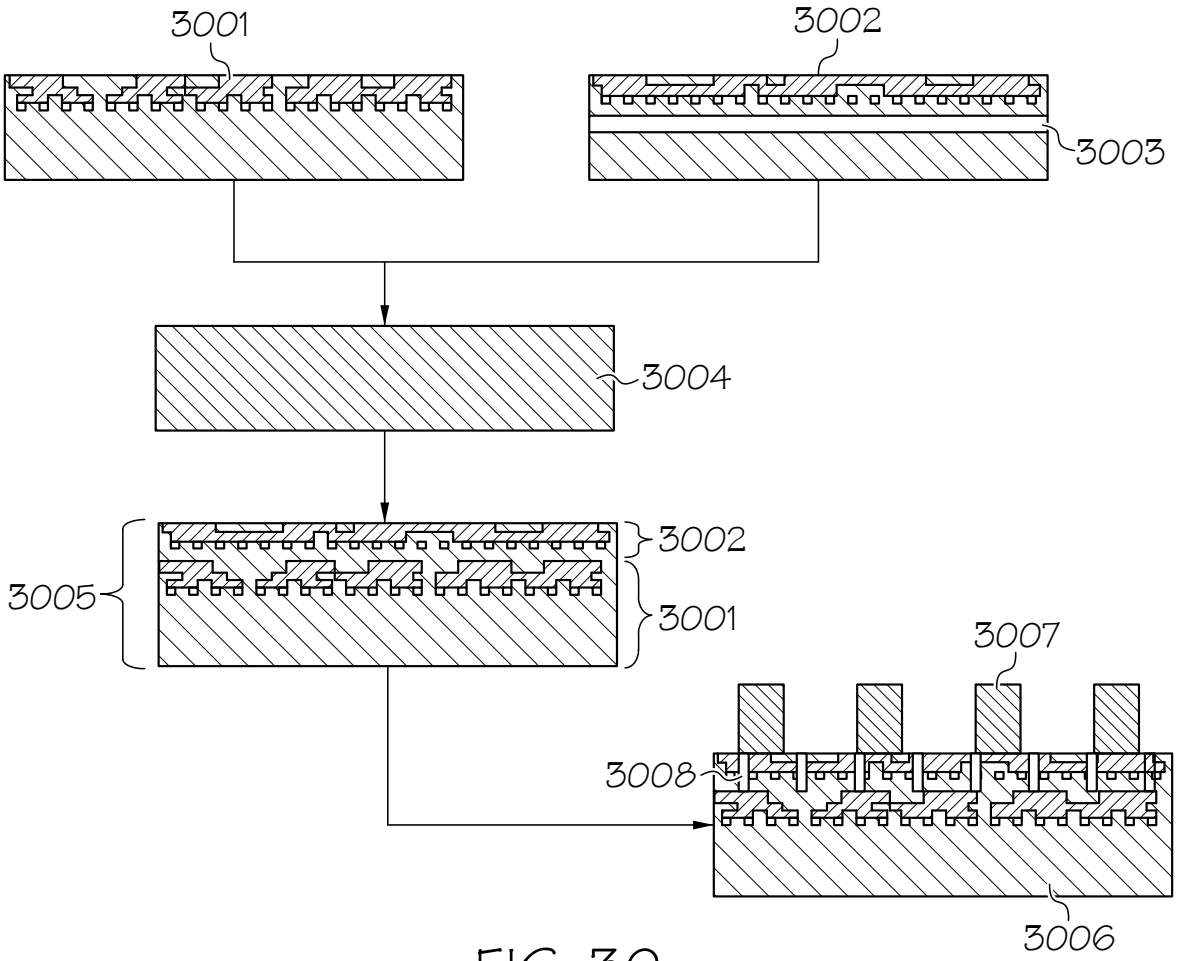


FIG. 30

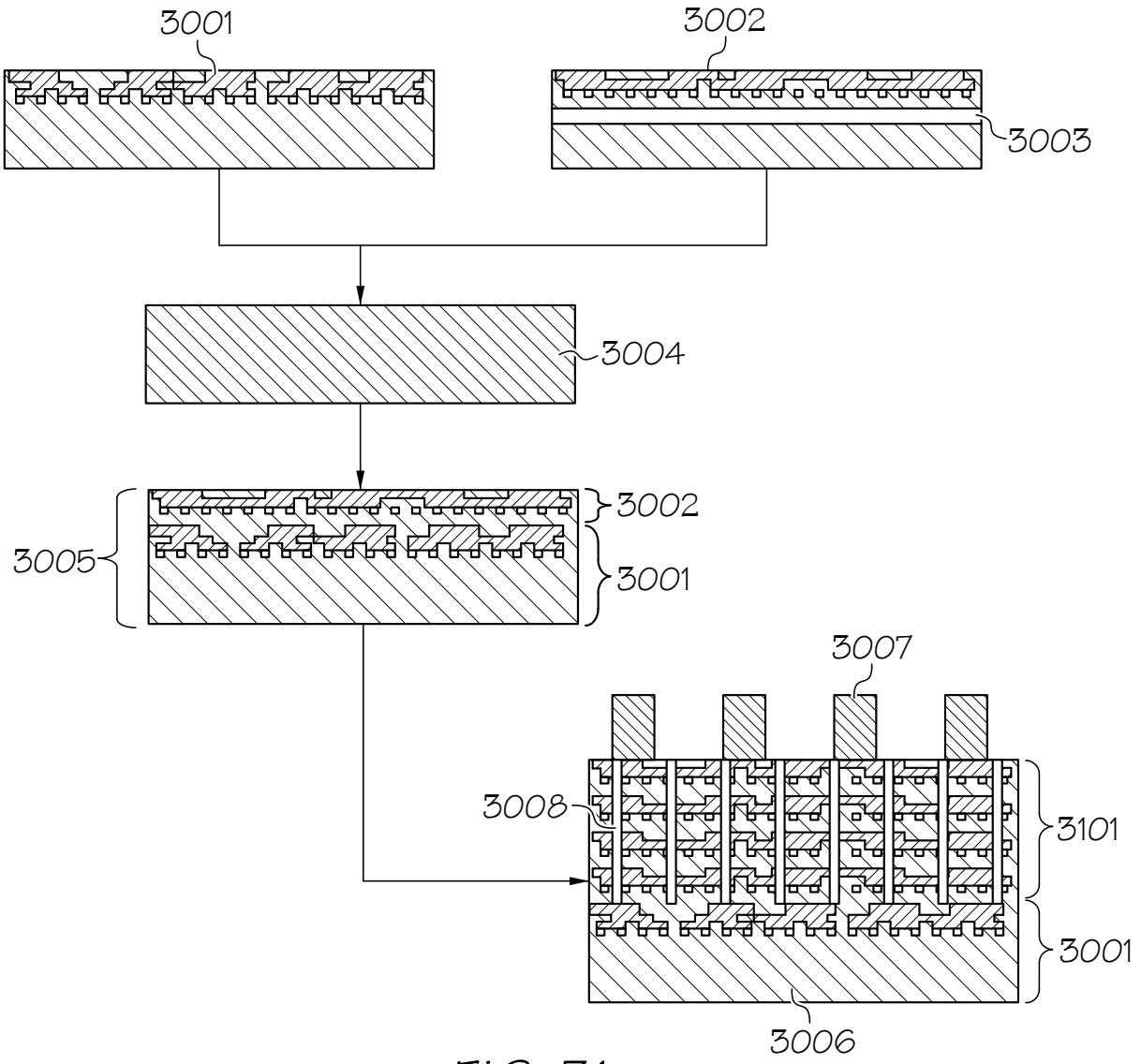


FIG. 31

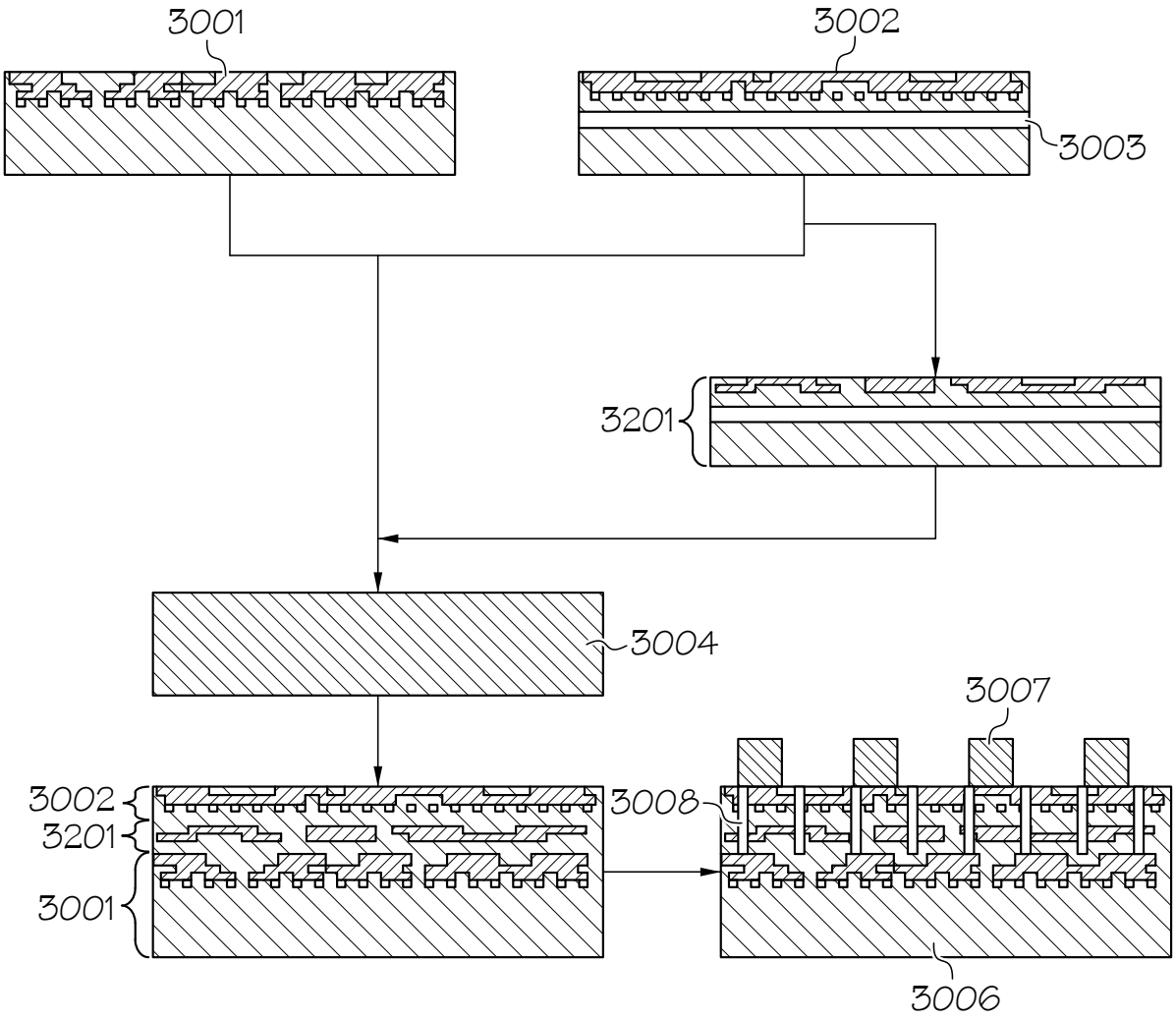
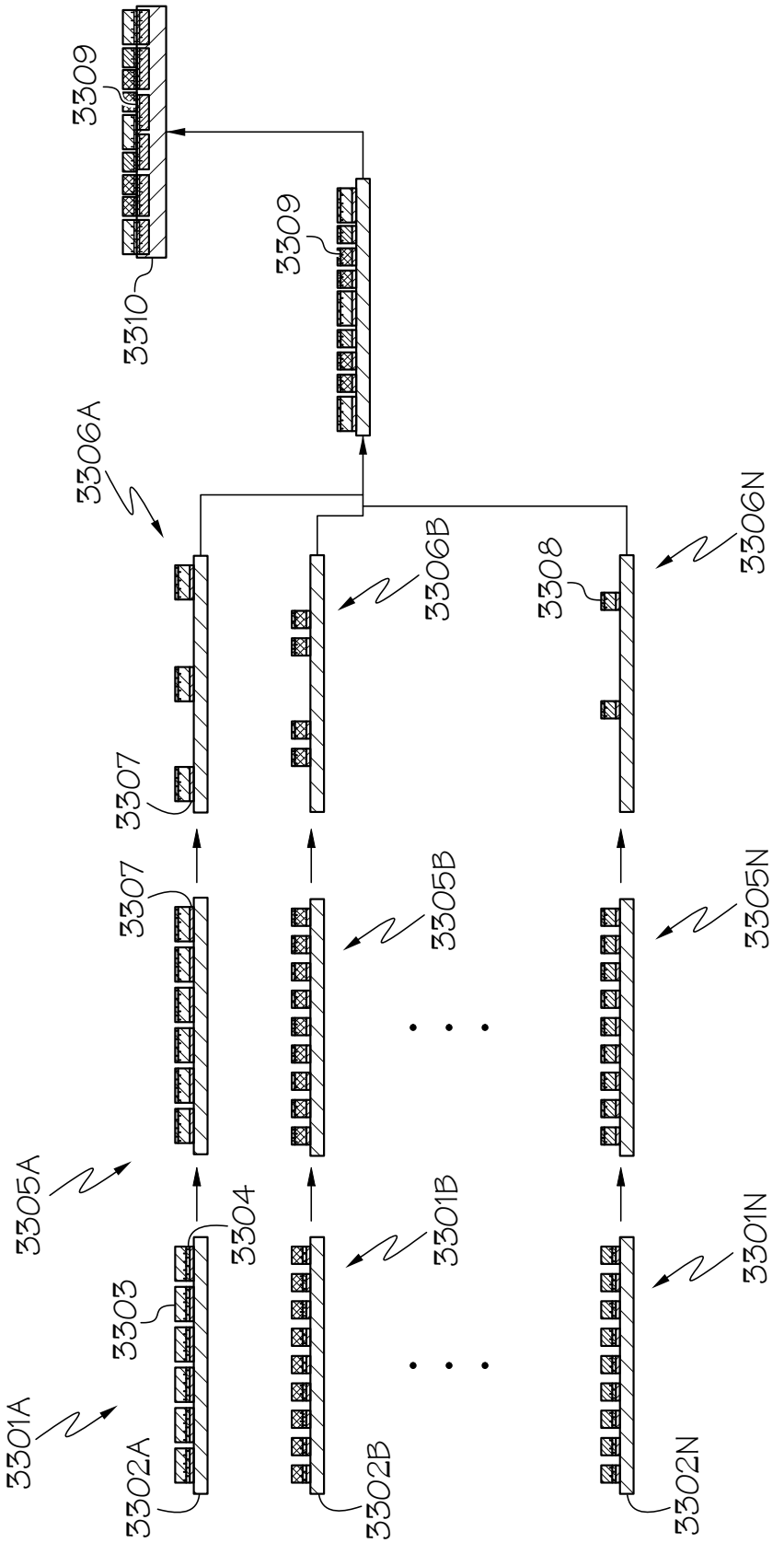


FIG. 32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3301N
3301A
3302A
3302B
3302N

FIG. 33

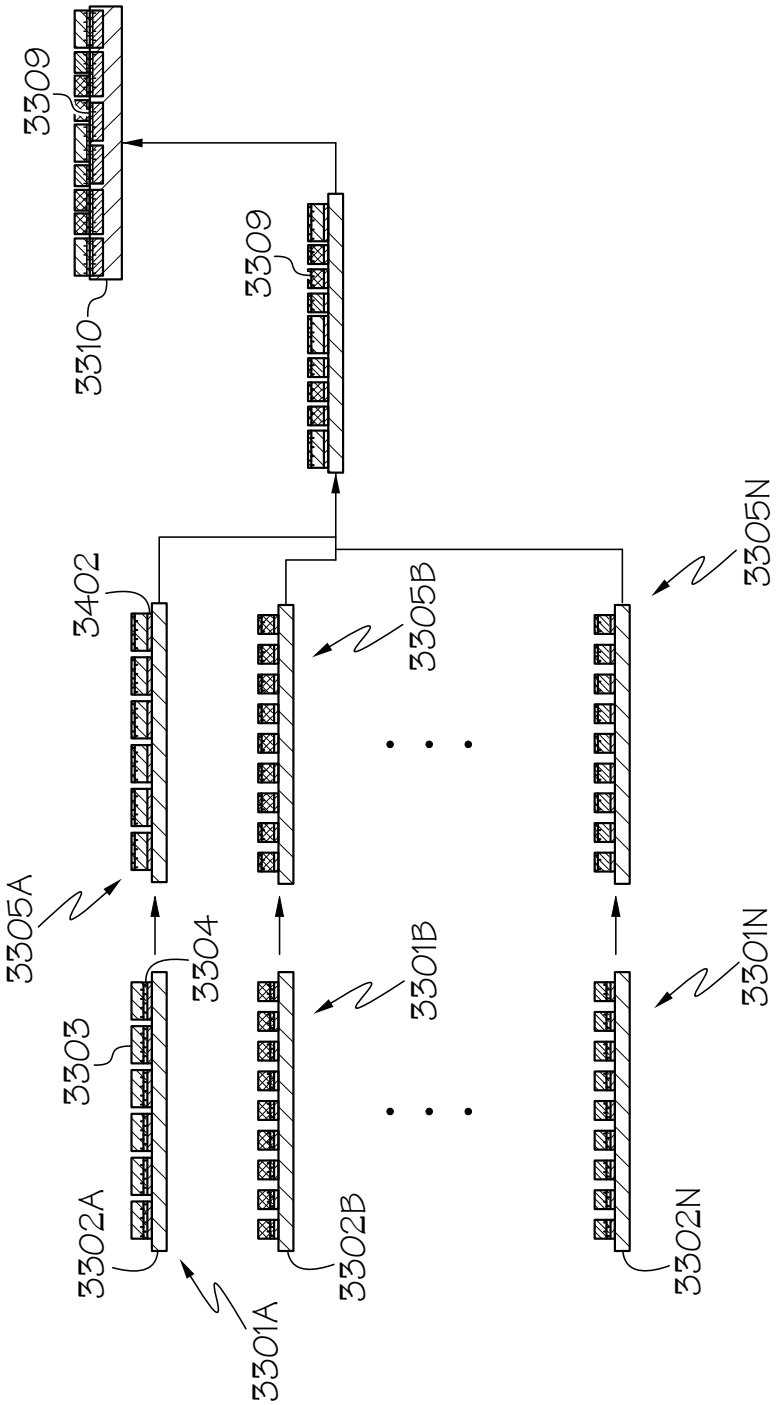
3309
3310
3309
3402
3305N
3305B
3305A
3304
3303
3301B
3301N
3302A
3302B
3302N
3301A

FIG. 34

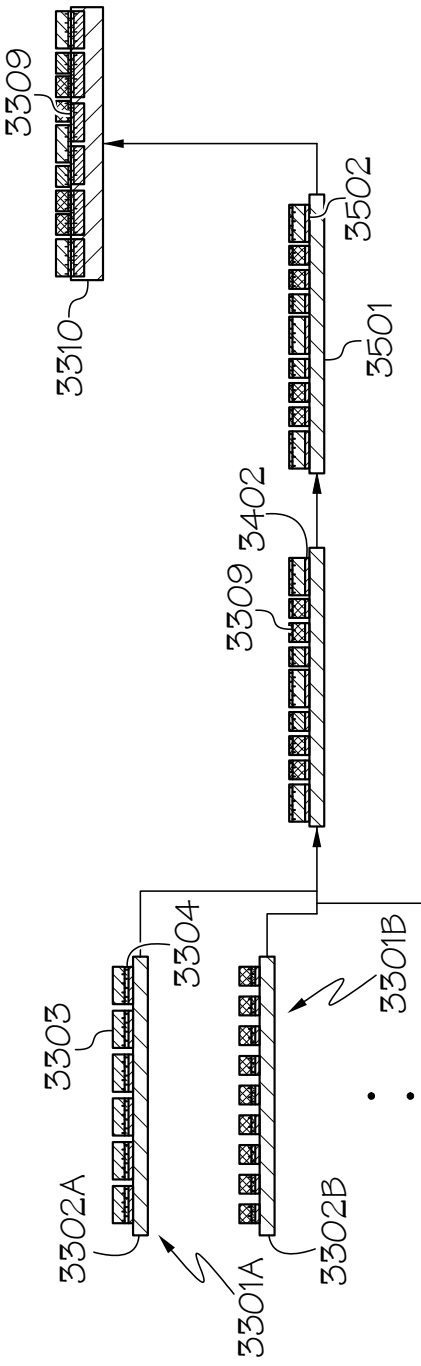
3309
3310
3502
3501
3402
3309
3303
3304
3301B
3301N
3302A
3301A
3302B
3302N

FIG. 35

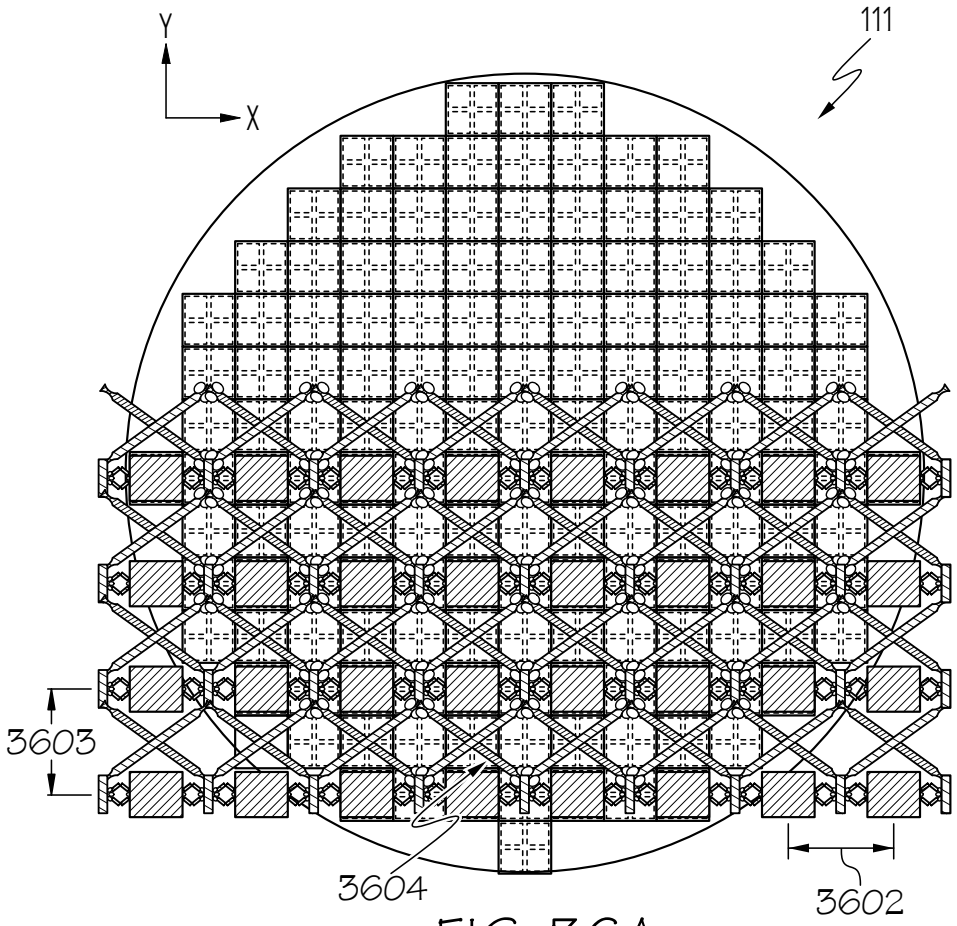

FIG. 36A

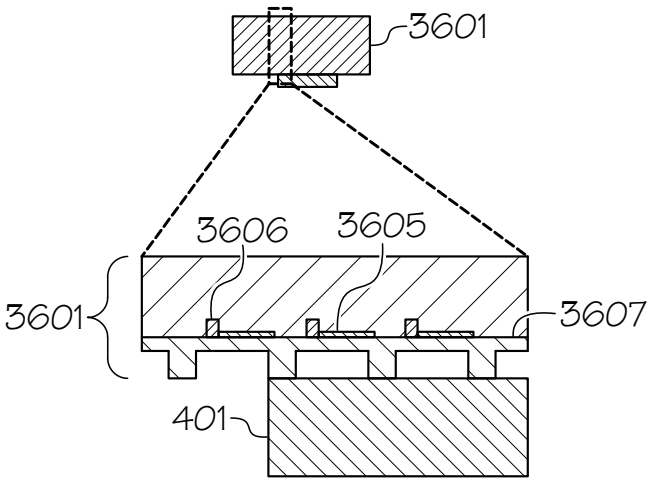

FIG. 36B

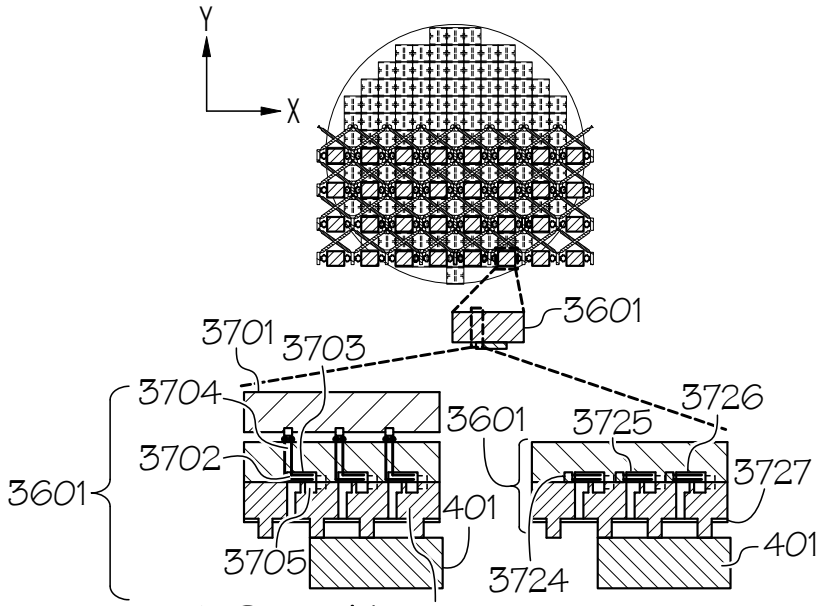

FIG. 37A FIG. 37I

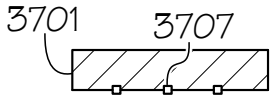

FIG. 37B

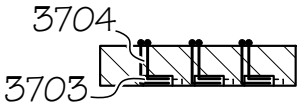

FIG. 37D

VACUUM CHANNEL PATTERNING	3708
METAL DEP AND PATTERNING (FOR FIXED ELECTRODE)	3709
OXIDE DEP	3710
METAL DEP AND PATERNING (FOR MOVABLE ELECTRODE)	3711
FLEXIBLE FILM DEPOSITION	3712
TSV PATTERN AND ETCH FROM BACKSIDE	3713
BUMP CREATION	3714

FIG. 37C

VACUUM CHANNEL PATTERNING	3715
OXIDE DEP	3716
TSV PATTERN AND ETCH FROM BACKSIDE	3717
PORUS FILM DEPOSITION	3718
OXIDE DEP	3719
PIN POLISHING	3720

FIG. 37E

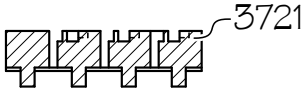

FIG. 37F

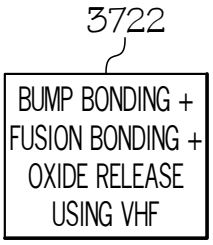

FIG. 37G

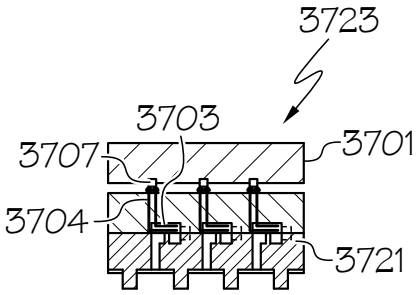

FIG. 37H

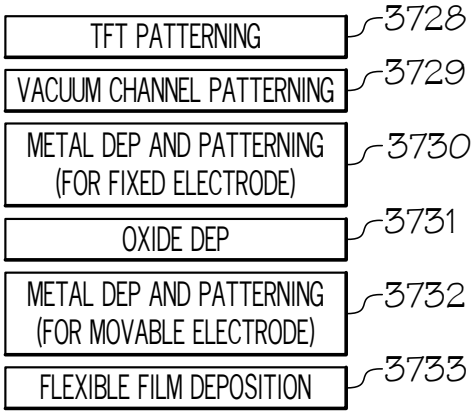

FIG. 37J

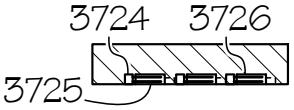

FIG. 37K

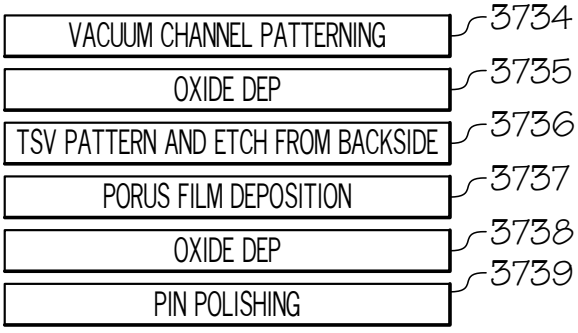

FIG. 37L

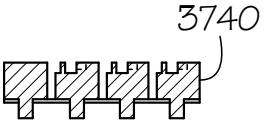

FIG. 37M

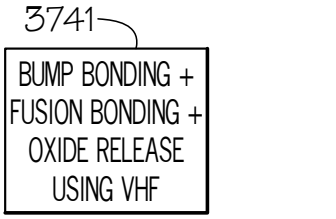

FIG. 37N

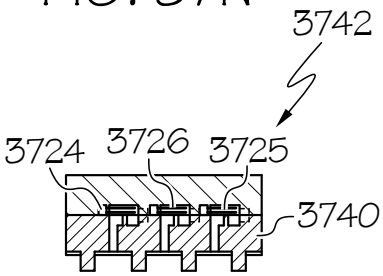

FIG. 37O

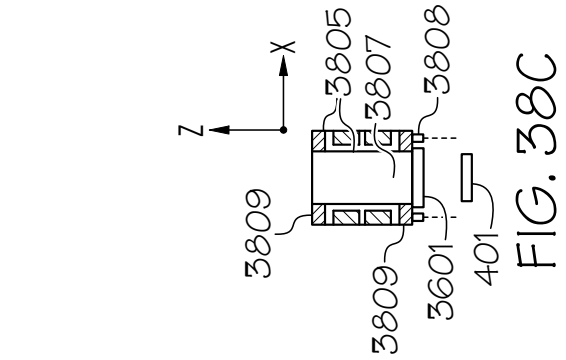

FIG. 38C

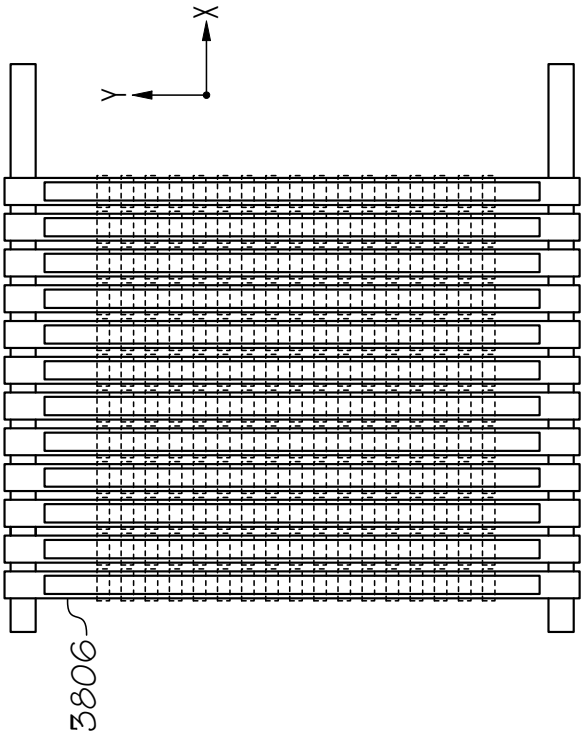

FIG. 38B

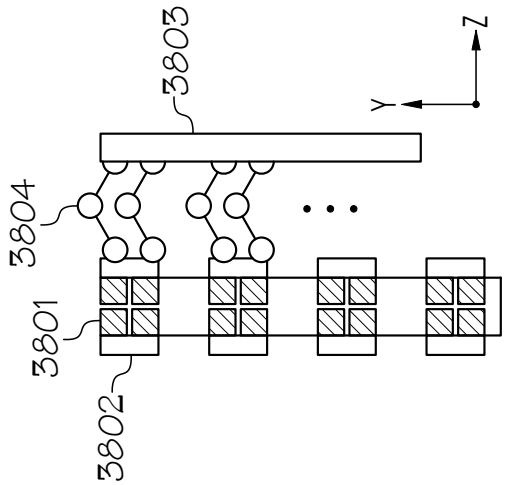

FIG. 38A

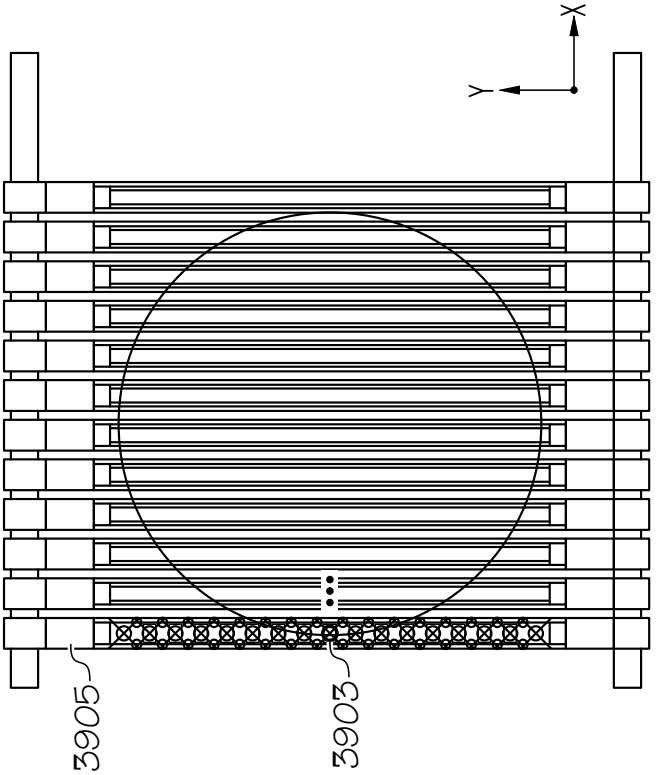

FIG. 39C

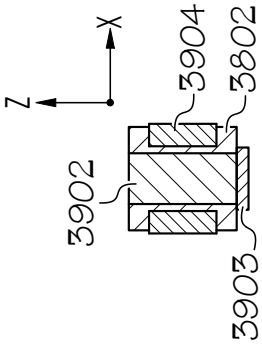

FIG. 39B

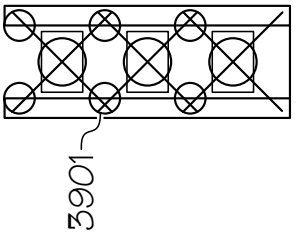

FIG. 39A

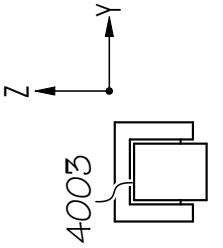

FIG. 40B

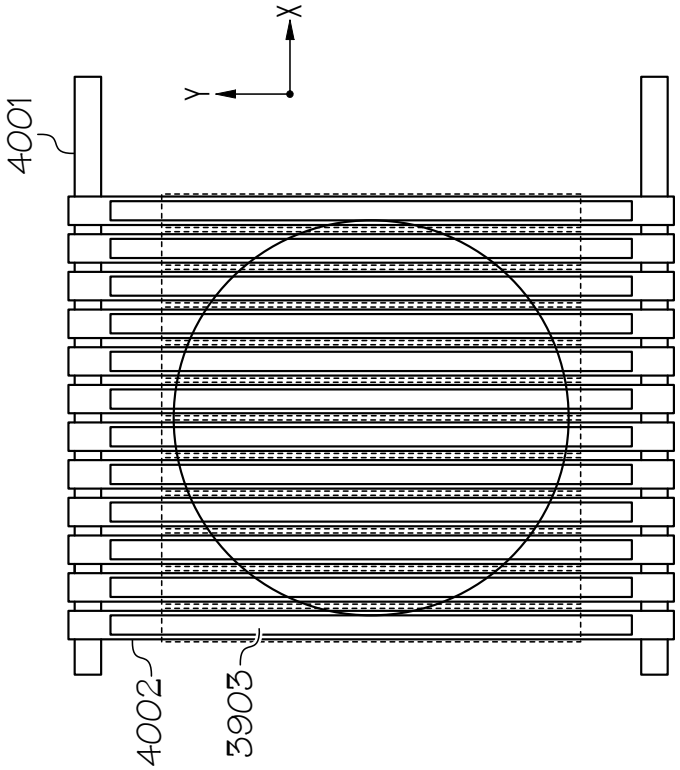

FIG. 40A

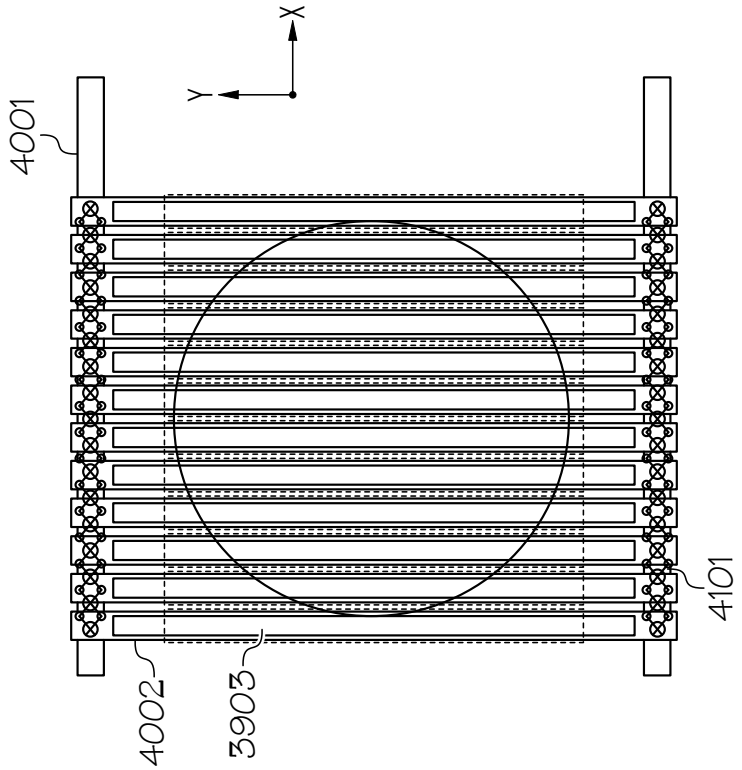

FIG. 41

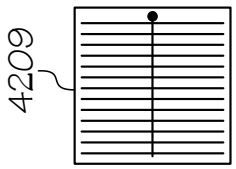

FIG. 42B

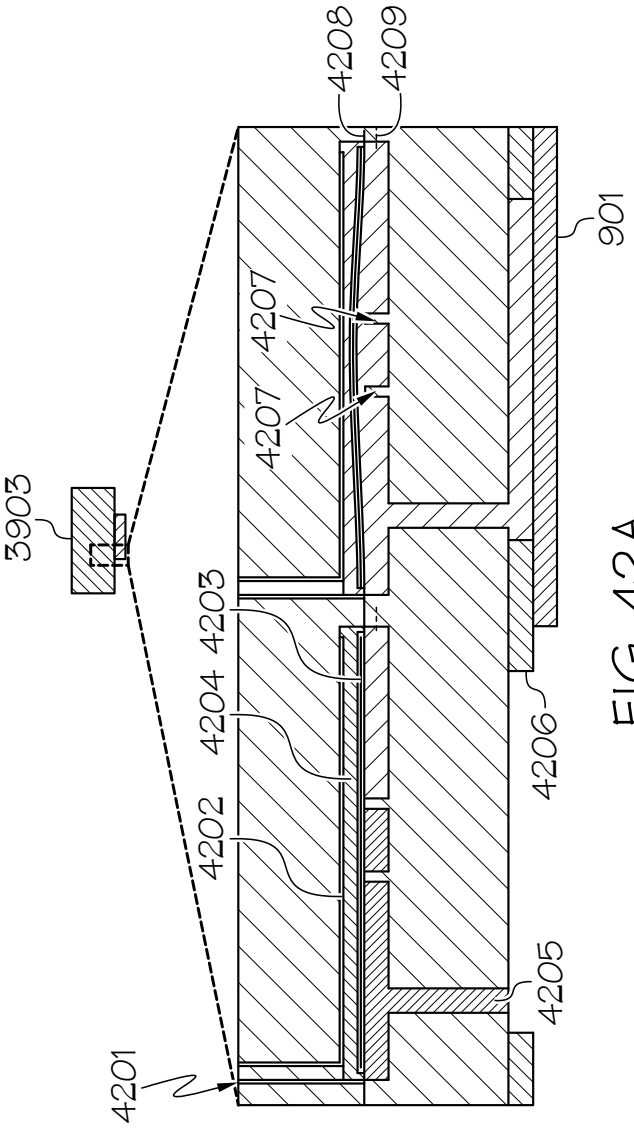

FIG. 42A

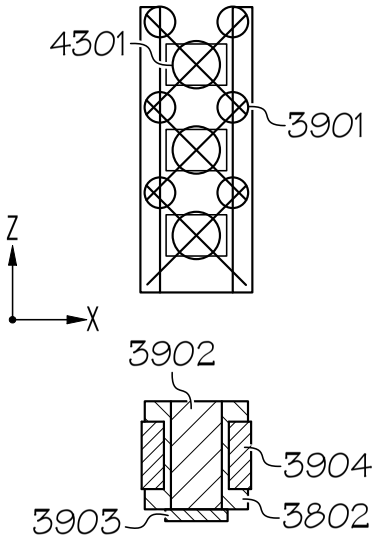

FIG. 43A

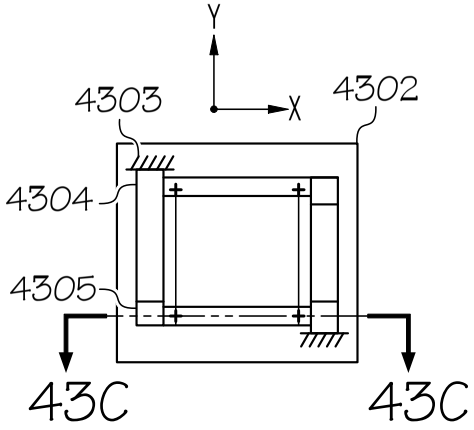

FIG. 43B

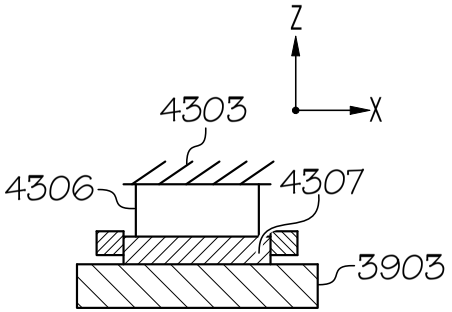

FIG. 43C

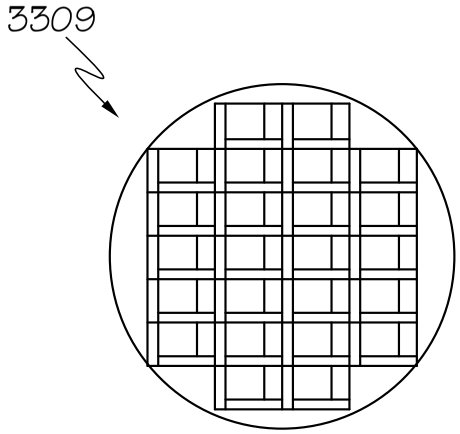

FIG. 44A

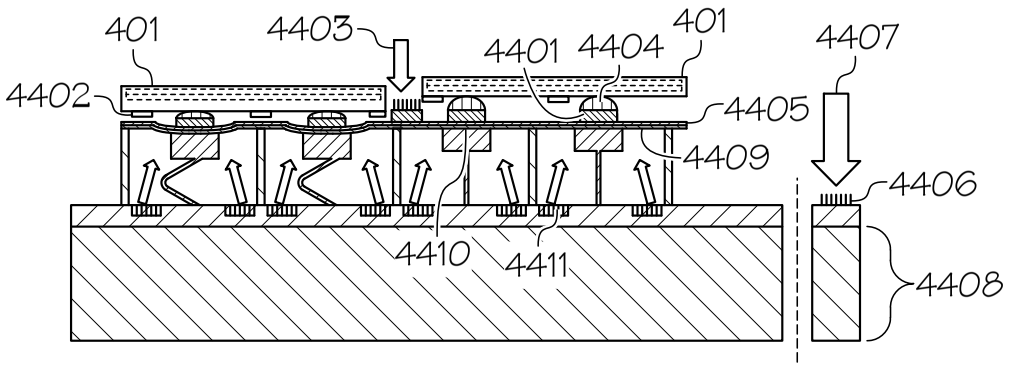

FIG. 44B

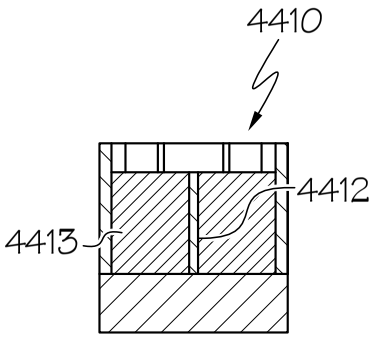

FIG. 44C

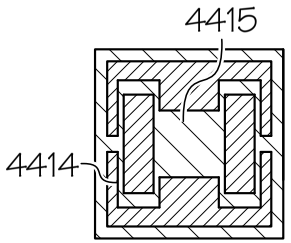

FIG. 44D

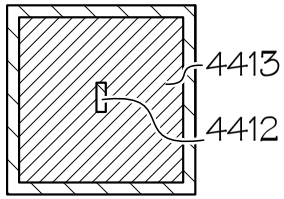

FIG. 44E

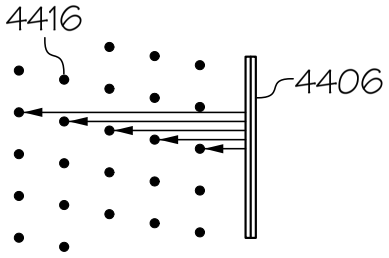

FIG. 44F

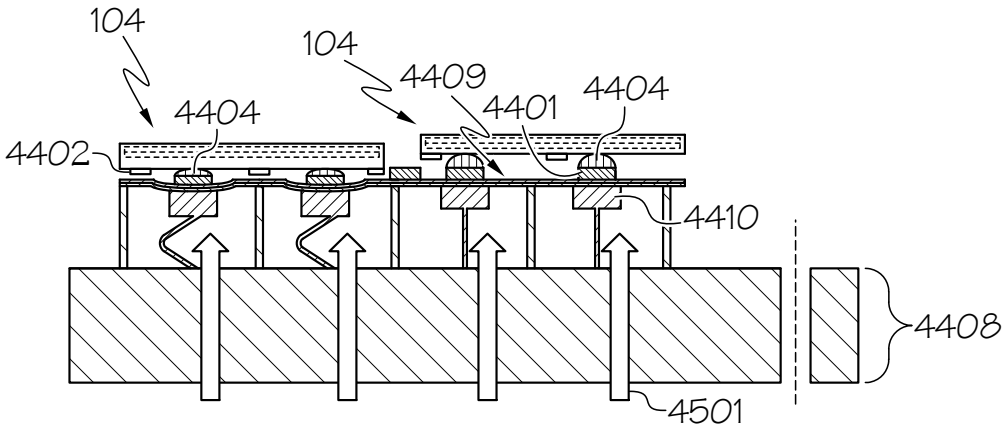

FIG. 45

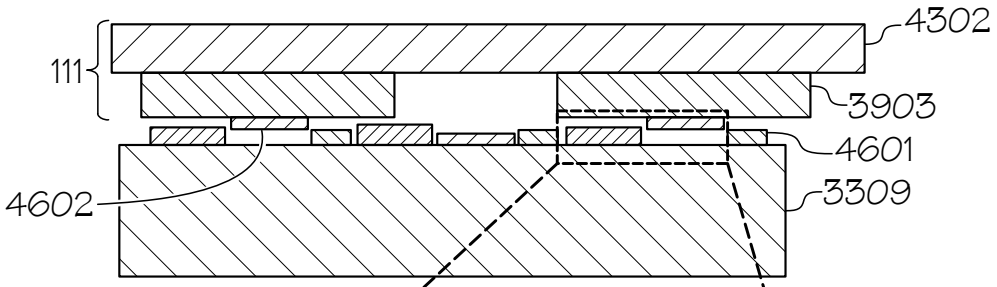

FIG. 46A

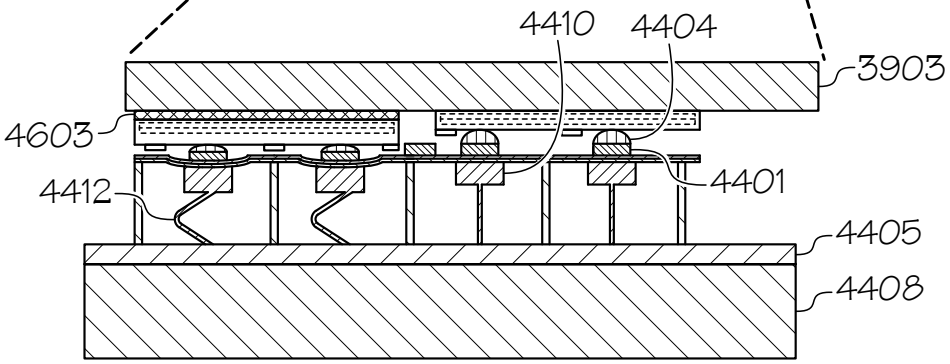

FIG. 46B

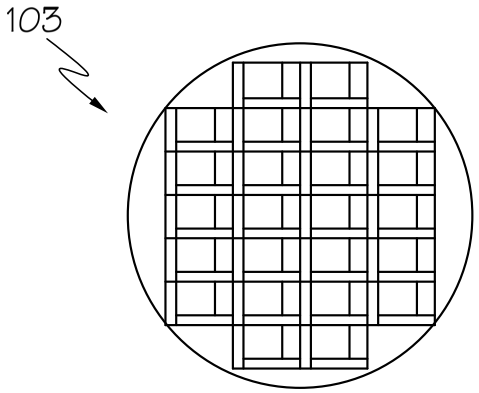

FIG. 47A

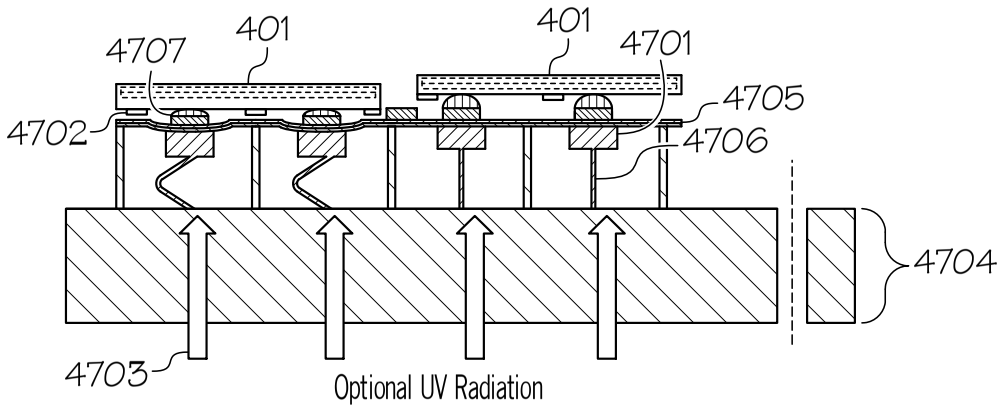

FIG. 47B

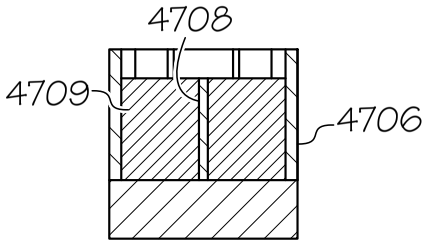

FIG. 47C

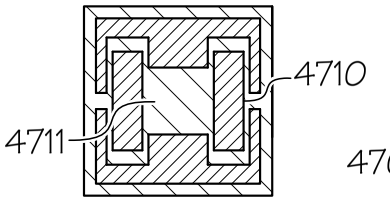

FIG. 47D

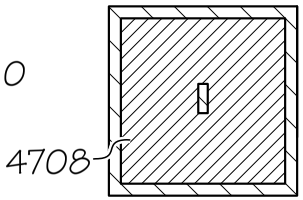

FIG. 47E

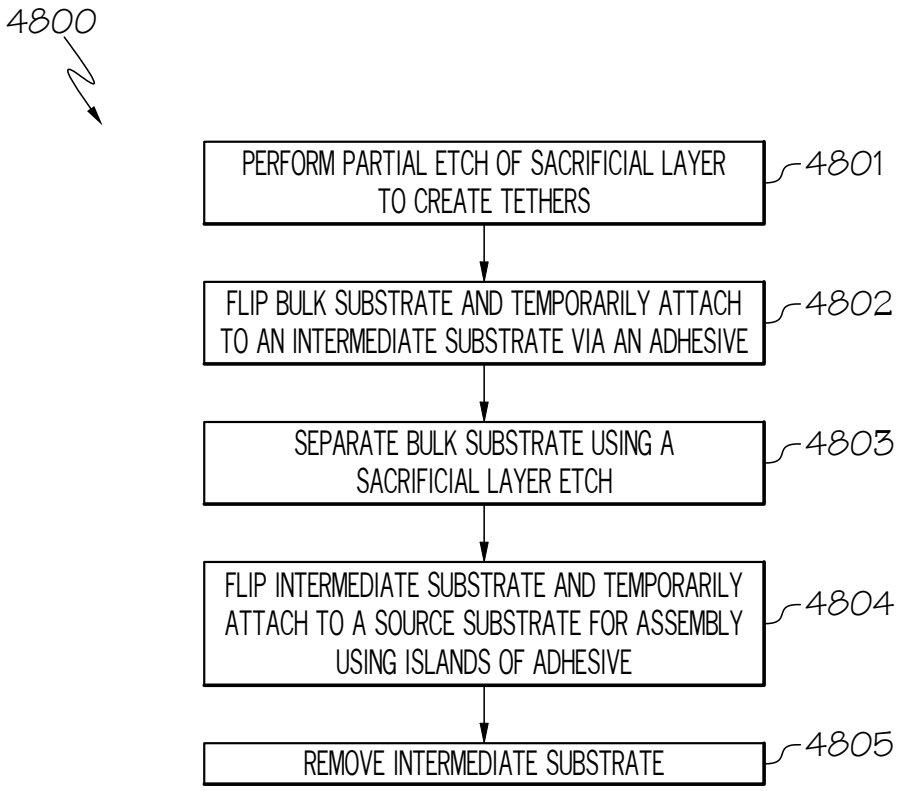
4800
PERFORM PARTIAL ETCH OF SACRIFICIAL LAYER TO CREATE TETHERS
4801
FLIP BULK SUBSTRATE AND TEMPORARILY ATTACH TO AN INTERMEDIATE SUBSTRATE VIA AN ADHESIVE
4802
SEPARATE BULK SUBSTRATE USING A SACRIFICIAL LAYER ETCH
4803
FLIP INTERMEDIATE SUBSTRATE AND TEMPORARILY ATTACH TO A SOURCE SUBSTRATE FOR ASSEMBLY USING ISLANDS OF ADHESIVE
4804
REMOVE INTERMEDIATE SUBSTRATE
4805

FIG. 48

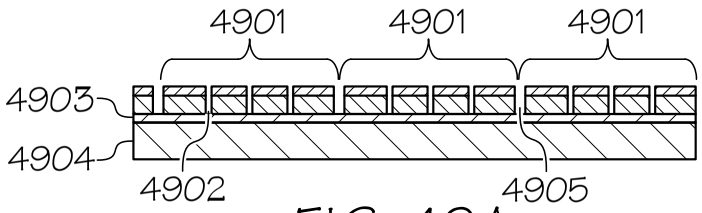

FIG. 49A

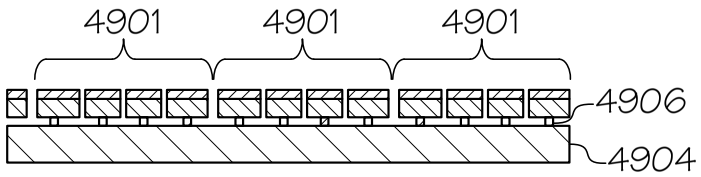

FIG. 49B

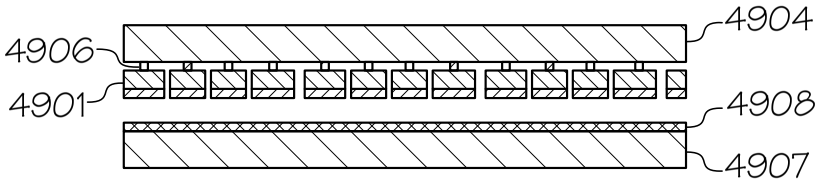

FIG. 49C

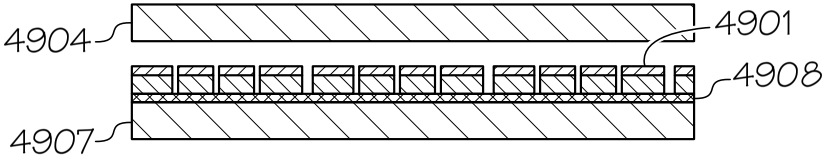

FIG. 49D

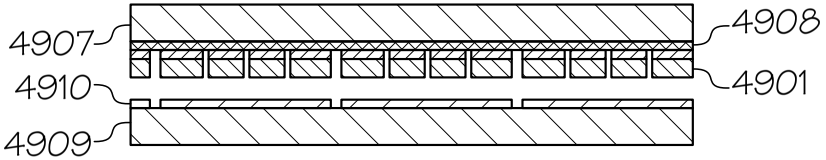

FIG. 49E

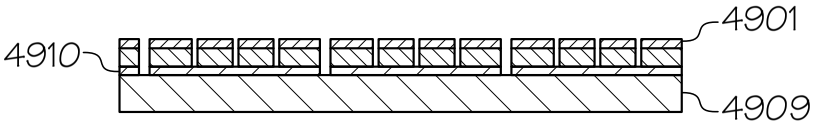

FIG. 49F

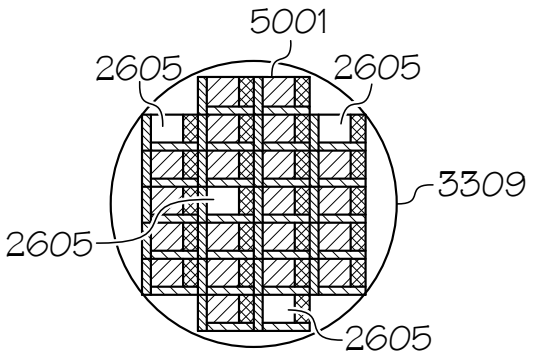

FIG. 50A

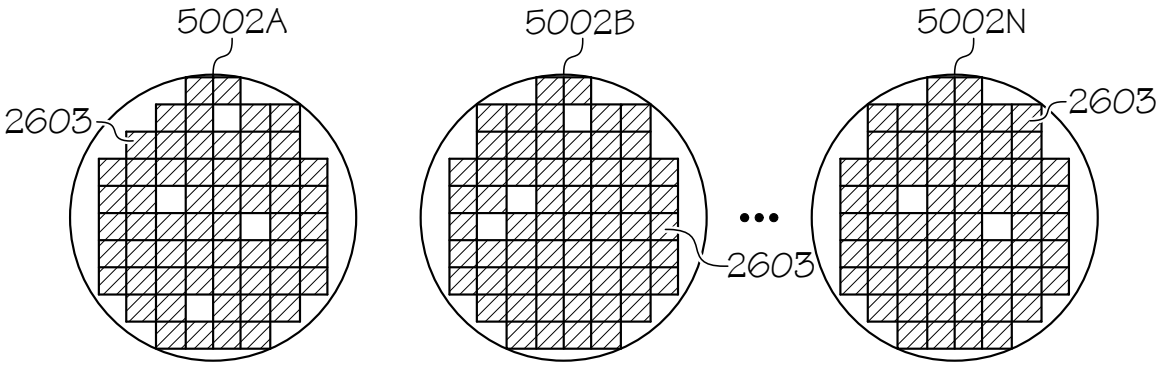

FIG. 50B

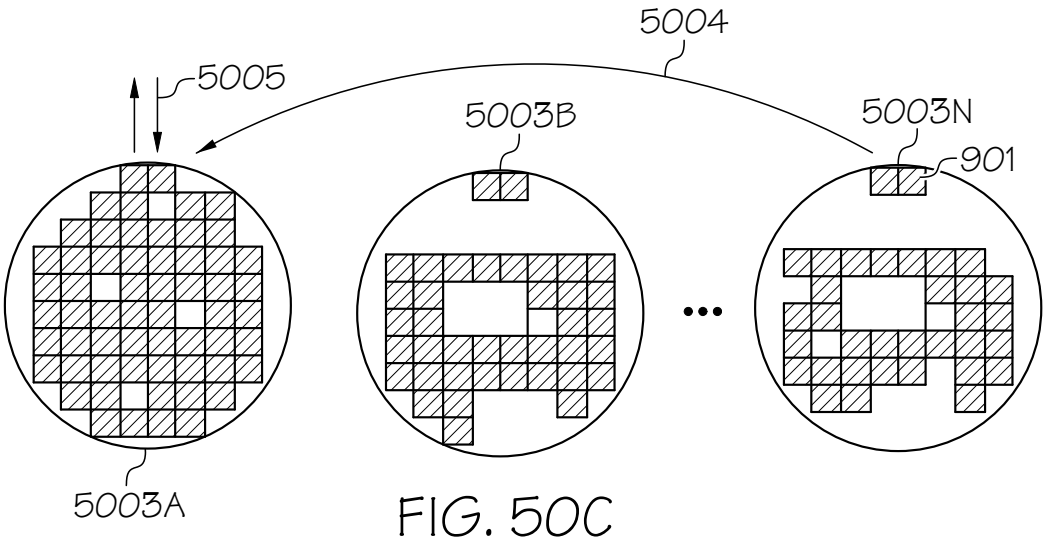

FIG. 50C

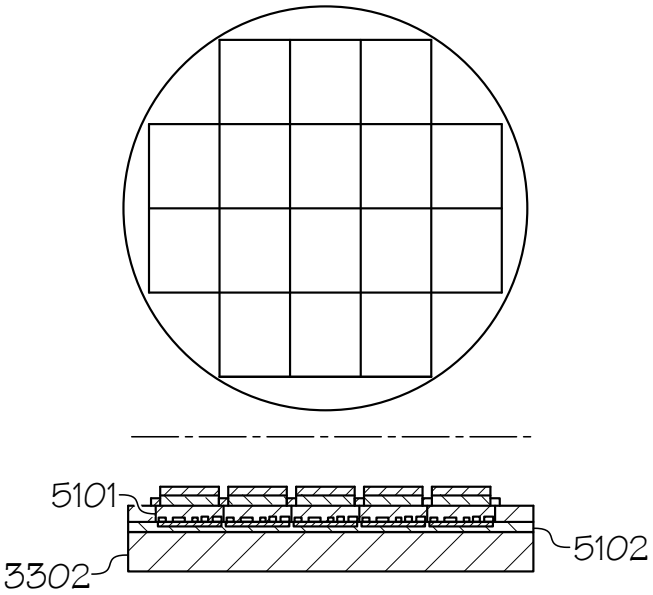

FIG. 51A

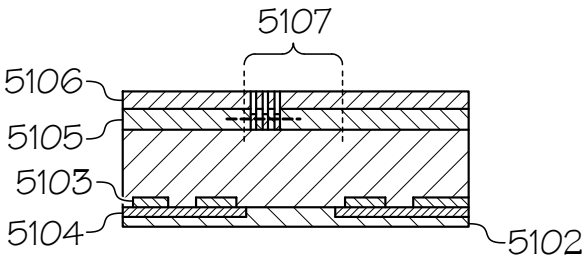

FIG. 51B

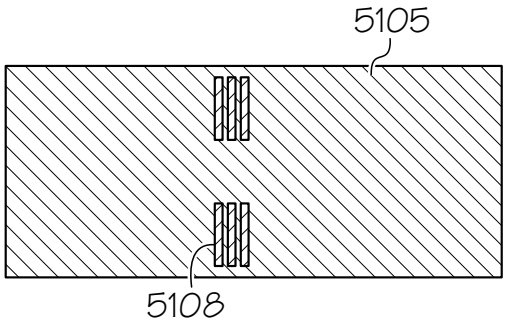

FIG. 51C

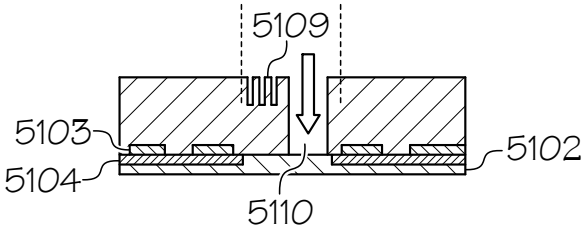

FIG. 51D

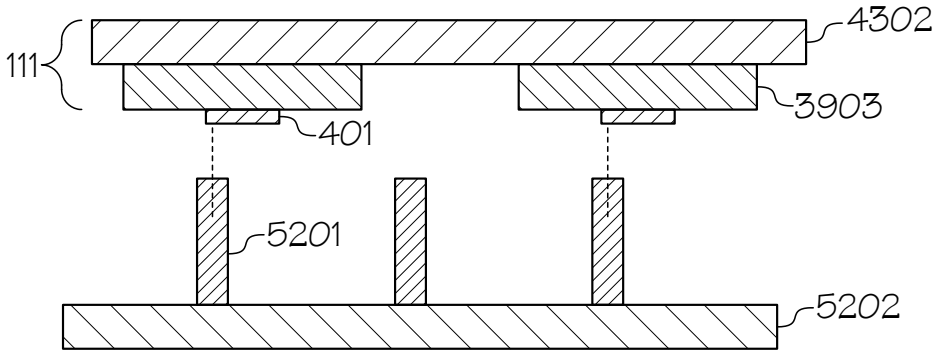

FIG. 52A

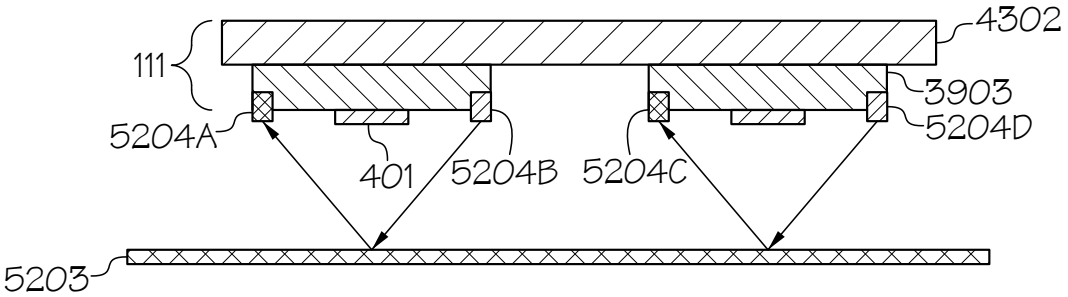

FIG. 52B

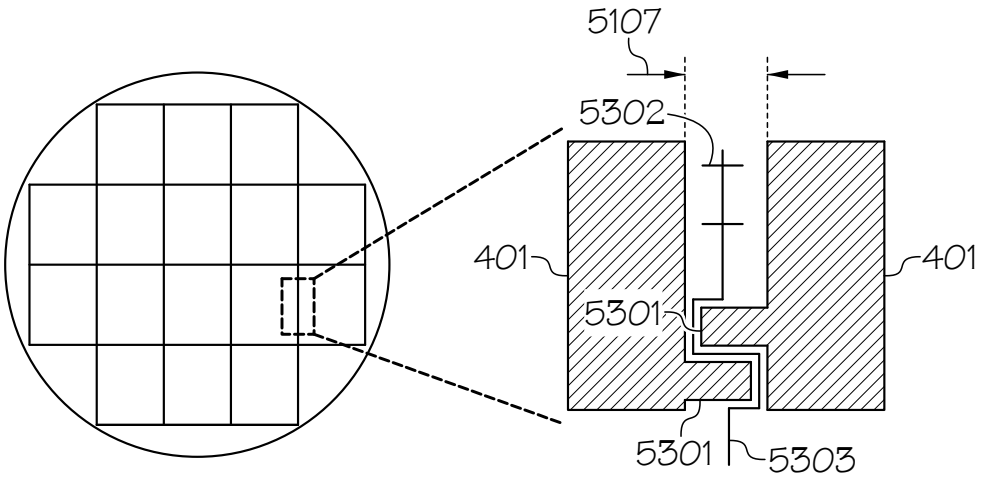

FIG. 53A

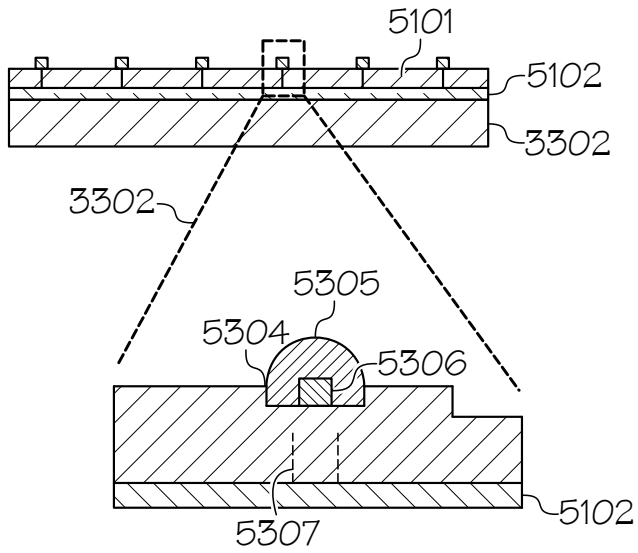

FIG. 53B

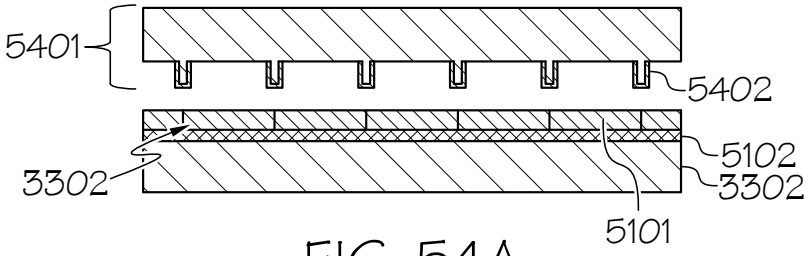

FIG. 54A

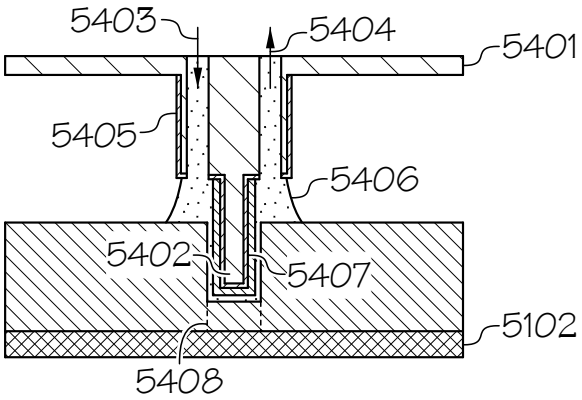

FIG. 54B

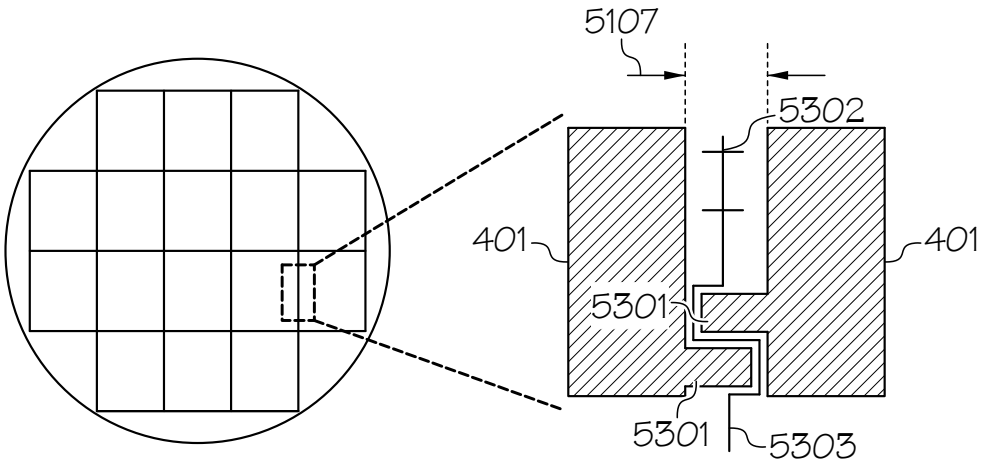

FIG. 55A

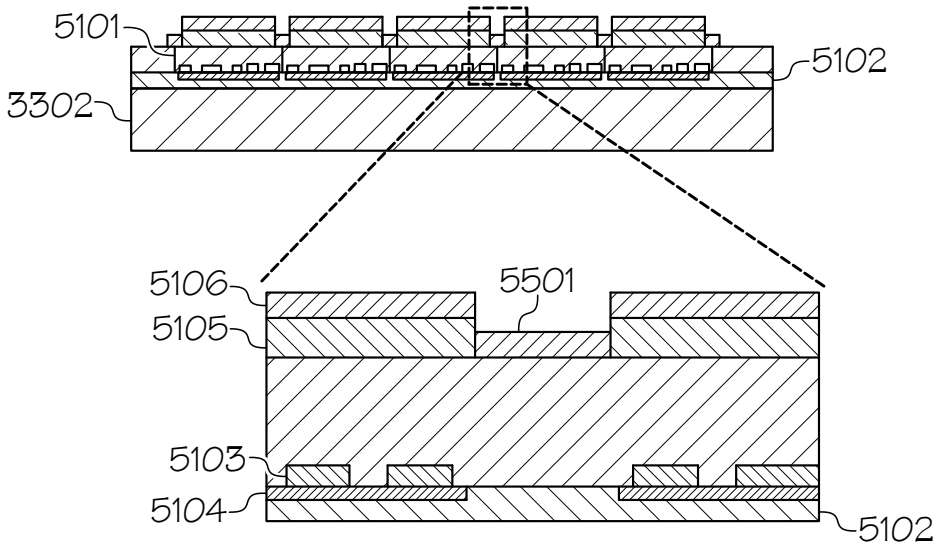

FIG. 55B

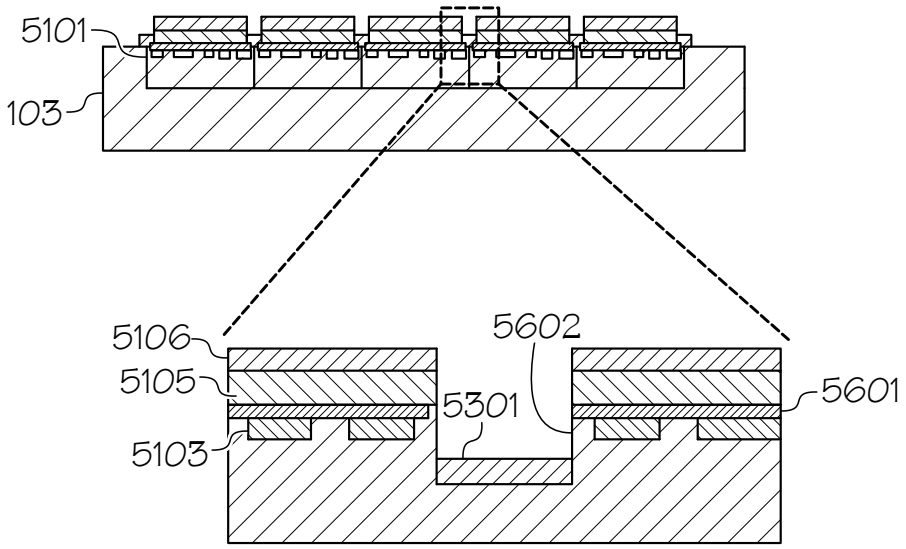

FIG. 56

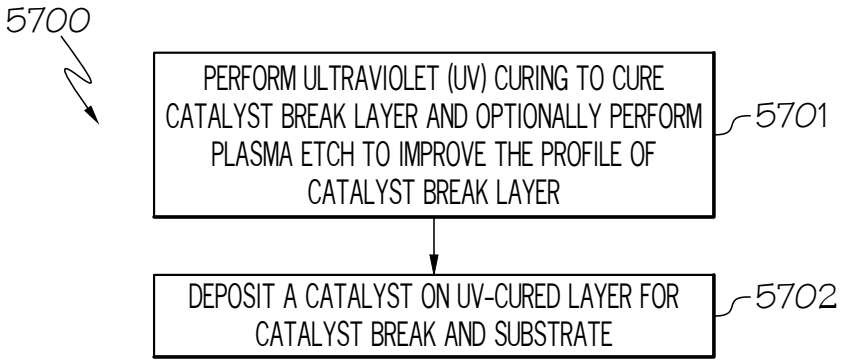

FIG. 57

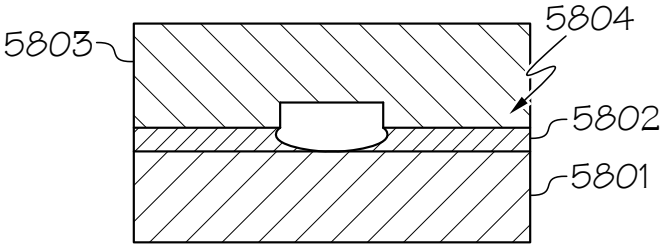

FIG. 58A

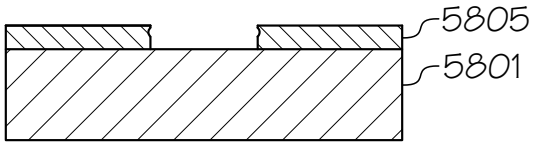

FIG. 58B

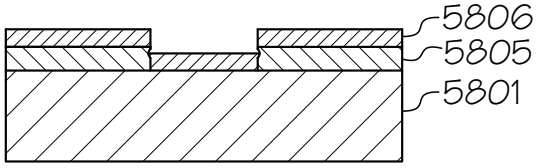

FIG. 58C

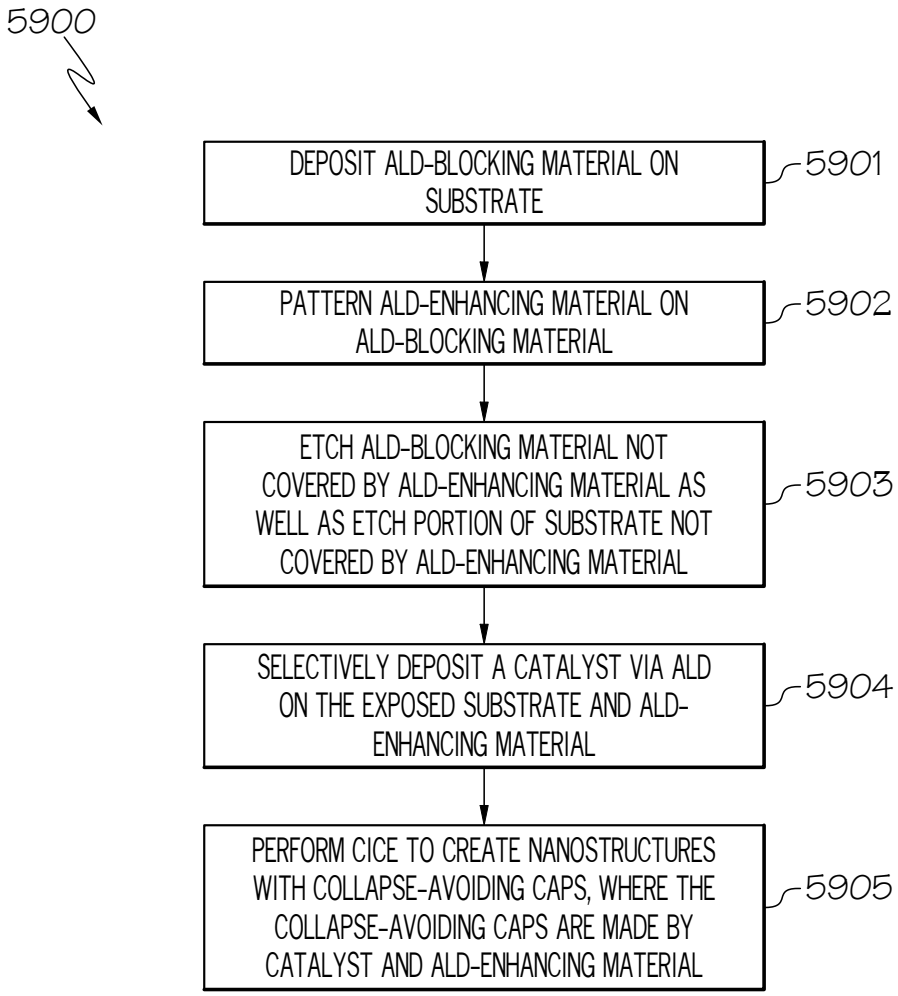
5900
DEPOSIT ALD-BLOCKING MATERIAL ON SUBSTRATE
5901
PATTERN ALD-ENHANCING MATERIAL ON ALD-BLOCKING MATERIAL
5902
ETCH ALD-BLOCKING MATERIAL NOT COVERED BY ALD-ENHANCING MATERIAL AS WELL AS ETCH PORTION OF SUBSTRATE NOT COVERED BY ALD-ENHANCING MATERIAL
5903
SELECTIVELY DEPOSIT A CATALYST VIA ALD ON THE EXPOSED SUBSTRATE AND ALD-ENHANCING MATERIAL
5904
PERFORM CICE TO CREATE NANOSTRUCTURES WITH COLLAPSE-AVOIDING CAPS, WHERE THE COLLAPSE-AVOIDING CAPS ARE MADE BY CATALYST AND ALD-ENHANCING MATERIAL
5905

FIG. 59

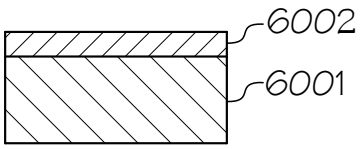

FIG. 60A

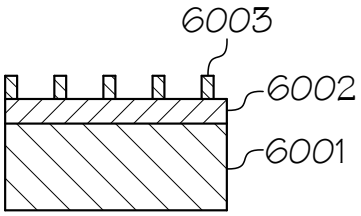

FIG. 60B

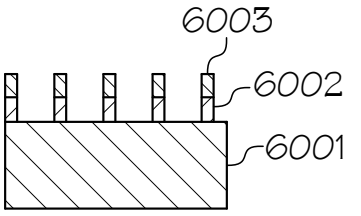

FIG. 60C

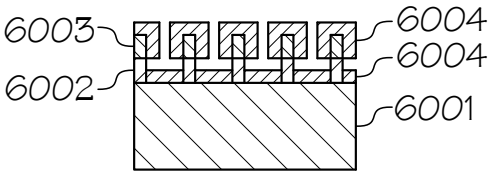

FIG. 60D

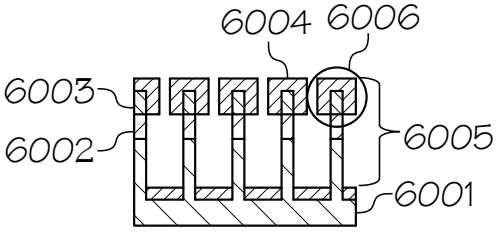

FIG. 60E

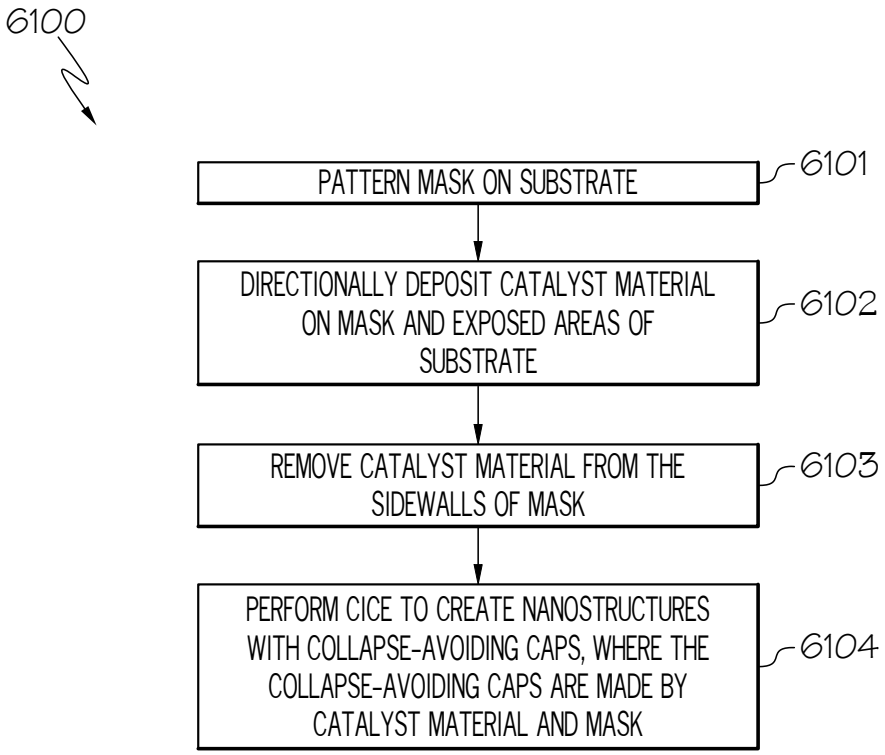
6100
PATTERN MASK ON SUBSTRATE
6101
DIRECTIONALLY DEPOSIT CATALYST MATERIAL ON MASK AND EXPOSED AREAS OF SUBSTRATE
6102
REMOVE CATALYST MATERIAL FROM THE SIDEWALLS OF MASK
6103
PERFORM CICE TO CREATE NANOSTRUCTURES WITH COLLAPSE-AVOIDING CAPS, WHERE THE COLLAPSE-AVOIDING CAPS ARE MADE BY CATALYST MATERIAL AND MASK
6104

FIG. 61

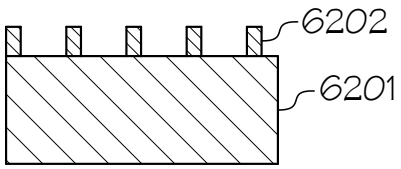

FIG. 62A

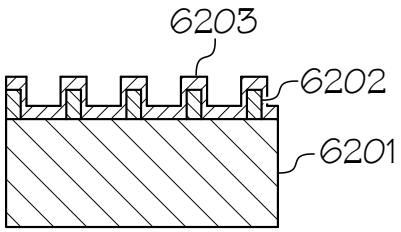

FIG. 62B

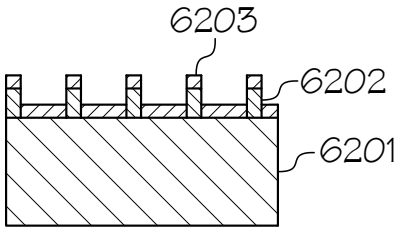

FIG. 62C

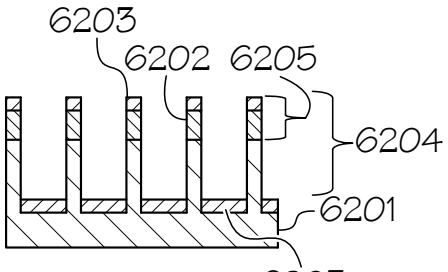

FIG. 62D

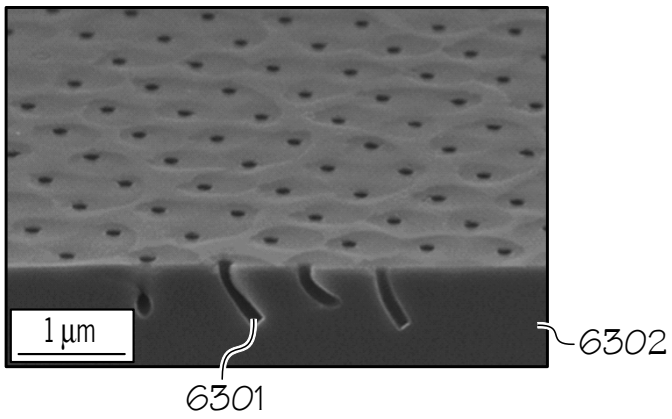

FIG. 63A



FIG. 63B

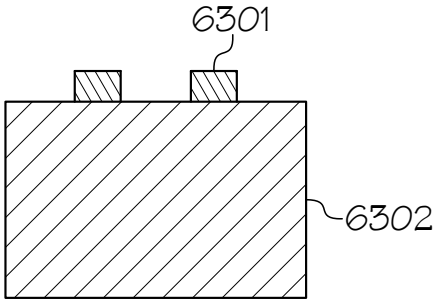

FIG. 63C

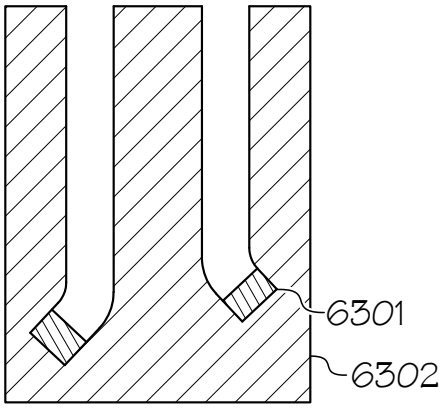

FIG. 63D

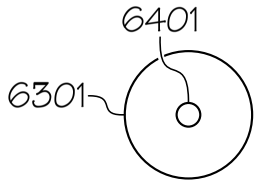

FIG. 64A

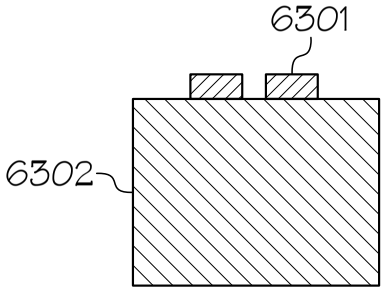

FIG. 64B

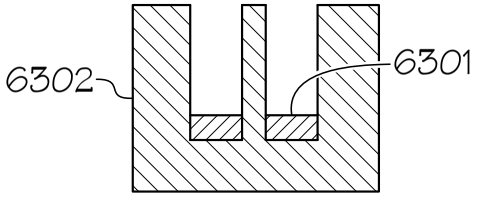

FIG. 64C

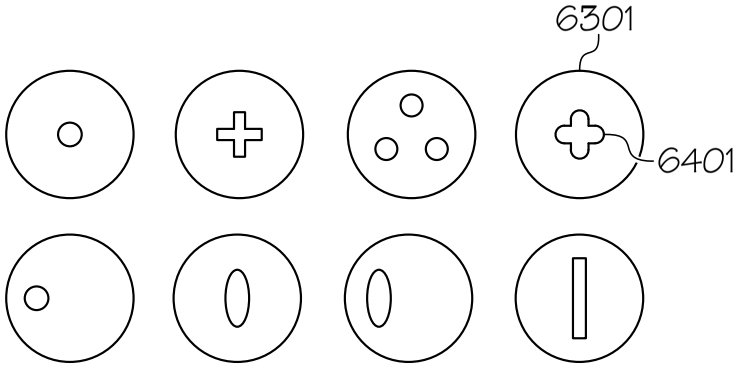

FIG. 64D

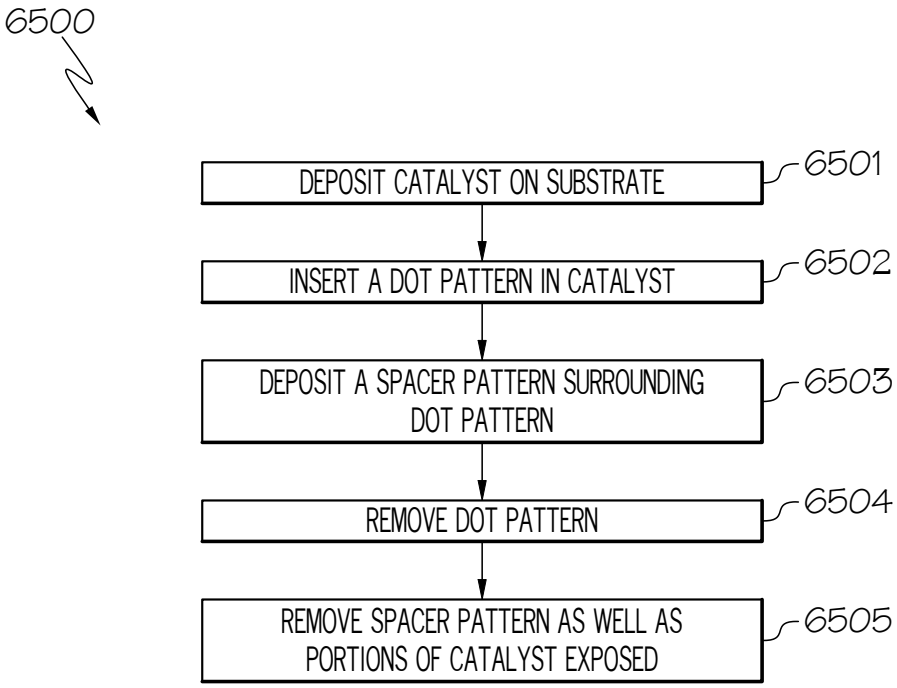
6500
DEPOSIT CATALYST ON SUBSTRATE
6501
INSERT A DOT PATTERN IN CATALYST
6502
DEPOSIT A SPACER PATTERN SURROUNDING DOT PATTERN
6503
REMOVE DOT PATTERN
6504
REMOVE SPACER PATTERN AS WELL AS PORTIONS OF CATALYST EXPOSED
6505

FIG. 65

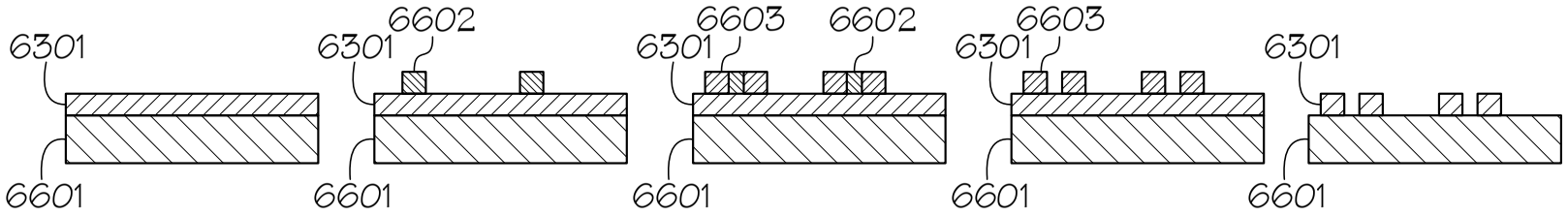

FIG. 66A FIG. 66B FIG. 66C FIG. 66D FIG. 66E

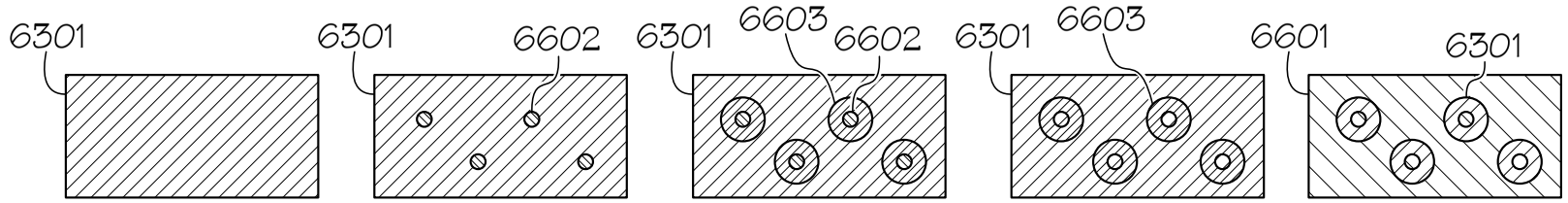

FIG. 67A FIG. 67B FIG. 67C FIG. 67D FIG. 67E

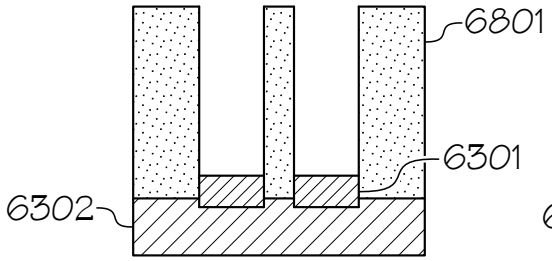

FIG. 68A

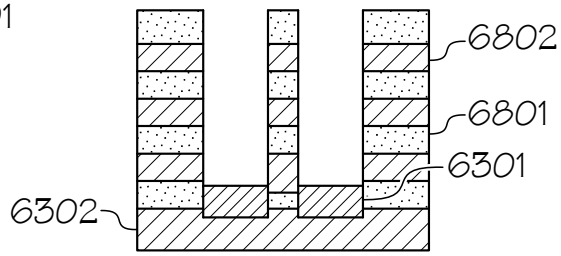

FIG. 68B

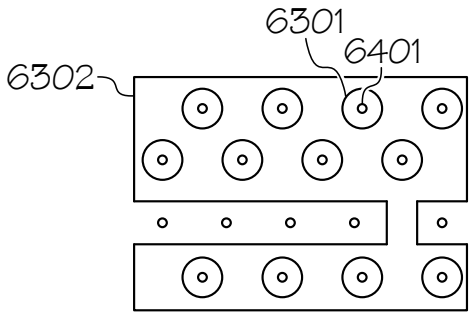

FIG. 69A

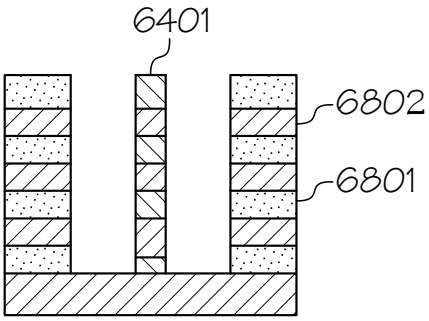

FIG. 69B

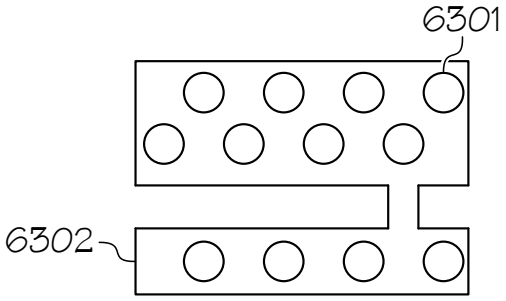

FIG. 69C

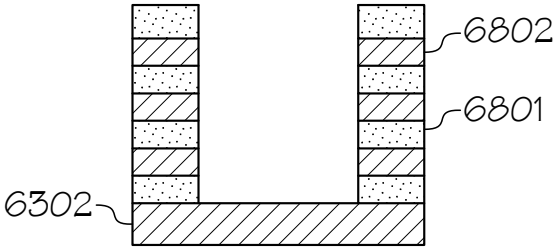

FIG. 69D

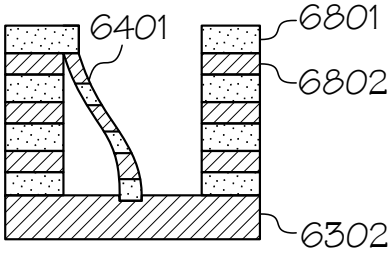

FIG. 70A

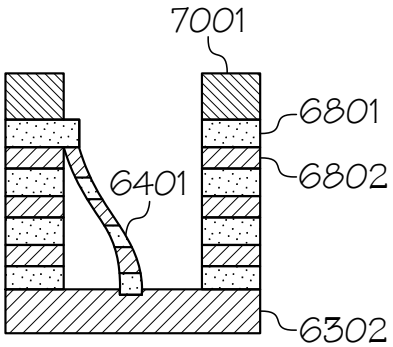

FIG. 70B

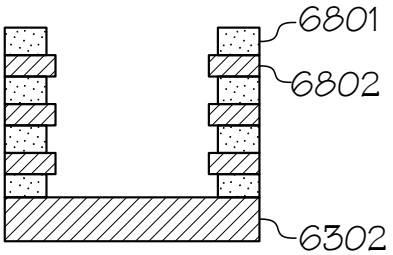

FIG. 70C

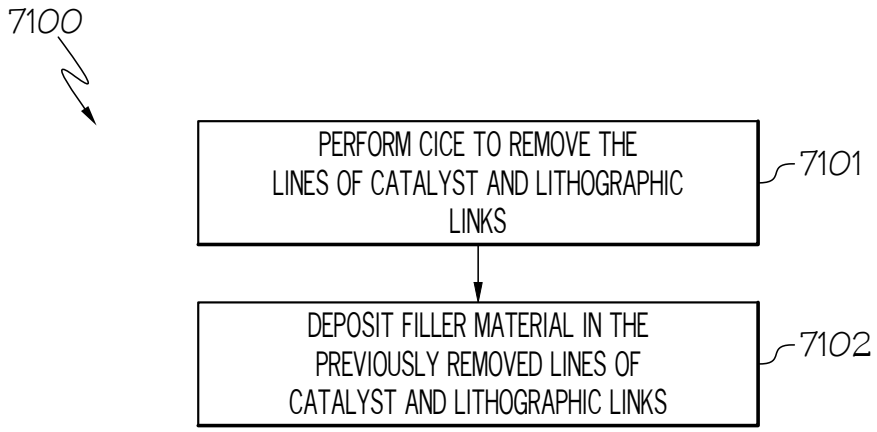
7100
PERFORM CICE TO REMOVE THE LINES OF CATALYST AND LITHOGRAPHIC LINKS
7101
DEPOSIT FILLER MATERIAL IN THE PREVIOUSLY REMOVED LINES OF CATALYST AND LITHOGRAPHIC LINKS
7102

FIG. 71

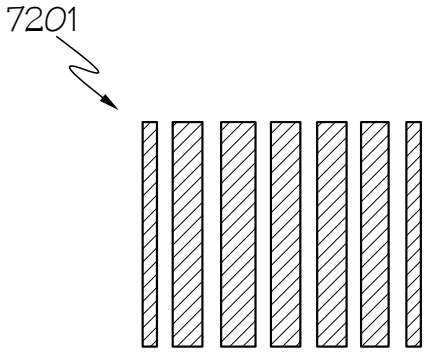

FIG. 72

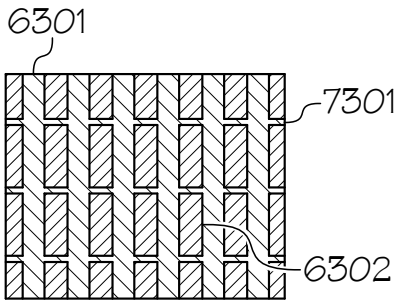

FIG. 73A

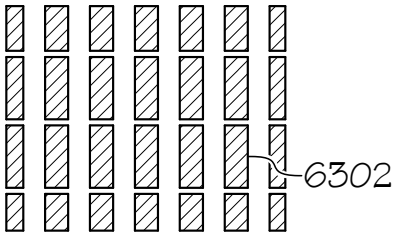

FIG. 73B

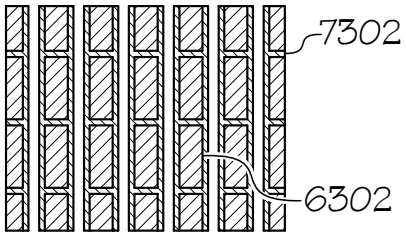

FIG. 73C

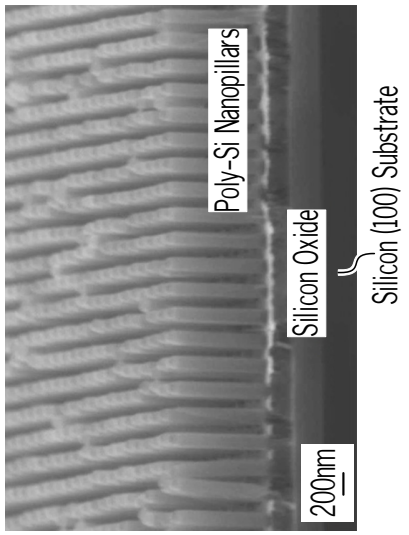

FIG. 74B

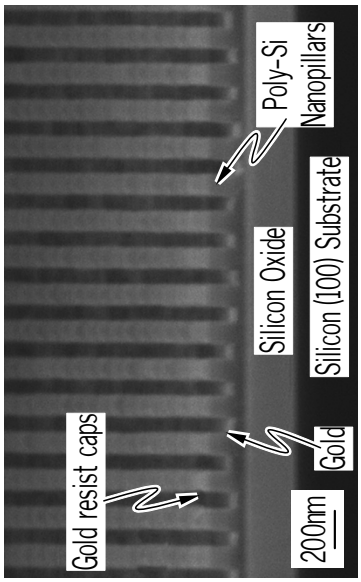

FIG. 74A

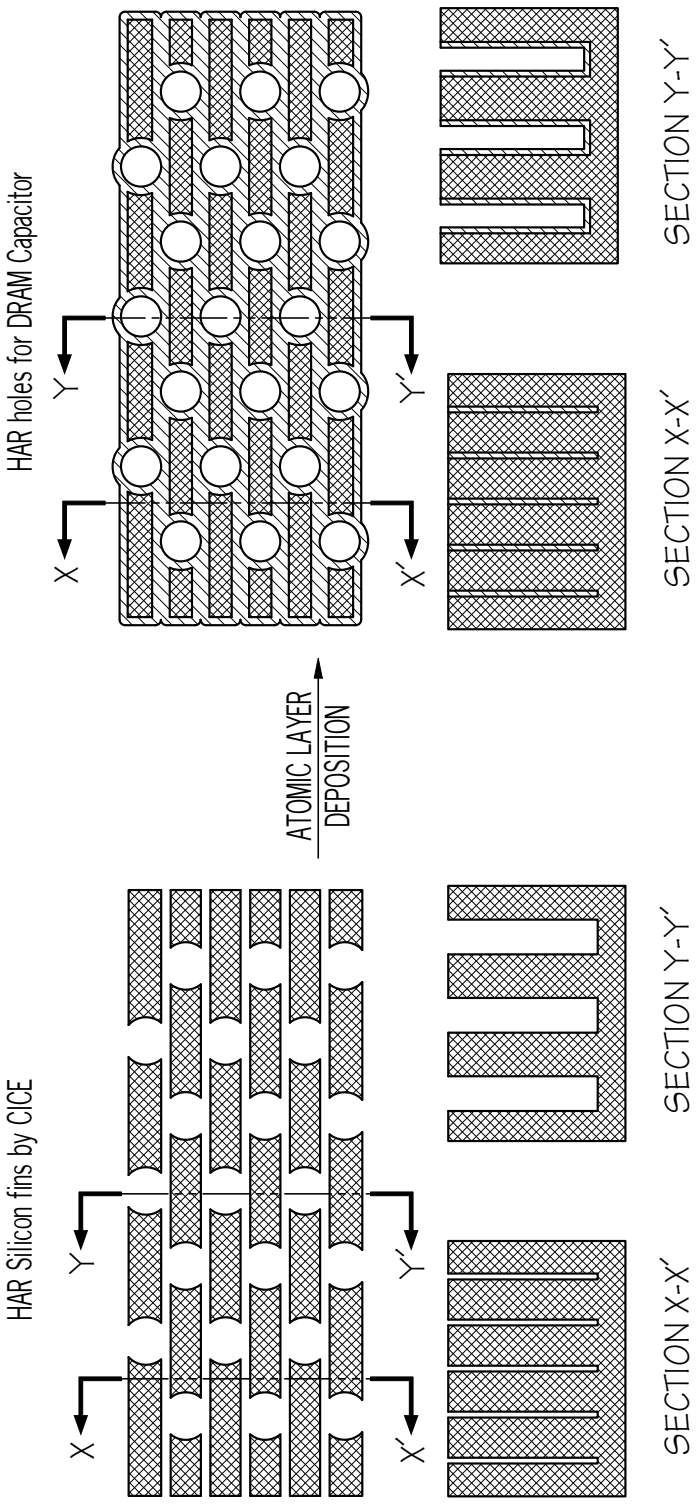
HAR Silicon fins by CICE
HAR holes for DRAM Capacitor
ATOMIC LAYER DEPOSITION
X
X'
Y
Y'
SECTION X-X'
SECTION Y-Y'
SECTION X-X'
SECTION Y-Y'

FIG. 75

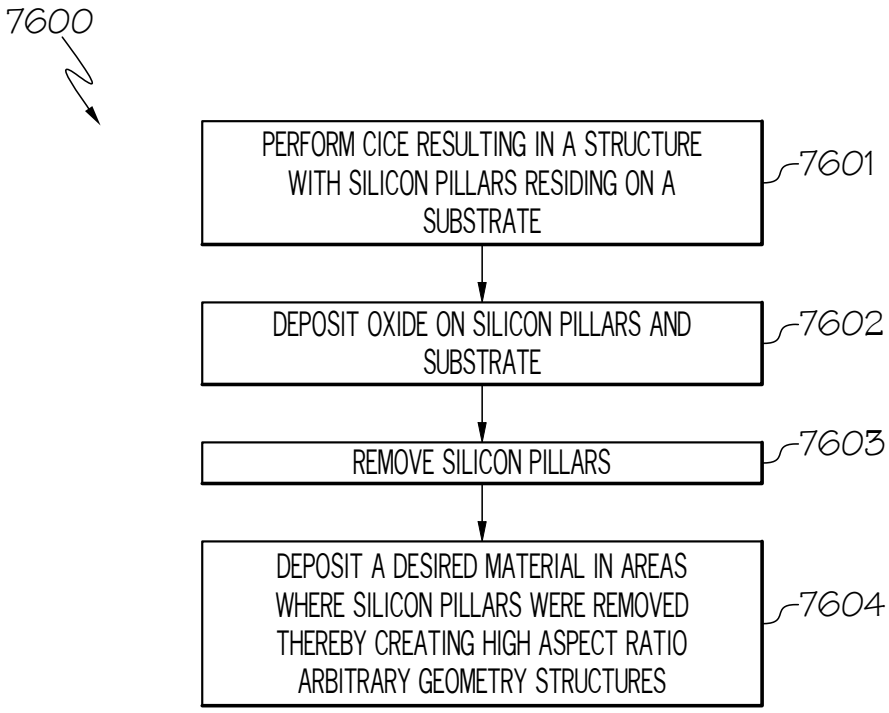
7600
PERFORM CICE RESULTING IN A STRUCTURE WITH SILICON PILLARS RESIDING ON A SUBSTRATE
7601
DEPOSIT OXIDE ON SILICON PILLARS AND SUBSTRATE
7602
REMOVE SILICON PILLARS
7603
DEPOSIT A DESIRED MATERIAL IN AREAS WHERE SILICON PILLARS WERE REMOVED THEREBY CREATING HIGH ASPECT RATIO ARBITRARY GEOMETRY STRUCTURES
7604

FIG. 76

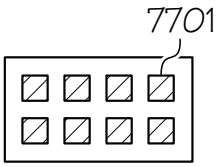

FIG. 77A

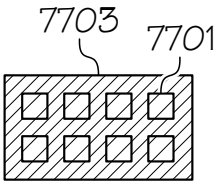

FIG. 77B

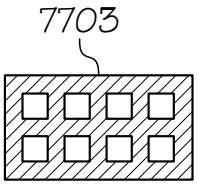

FIG. 77C

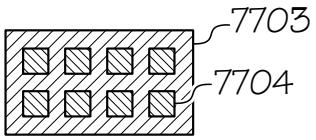

FIG. 77D

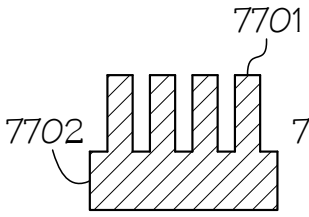

FIG. 78A

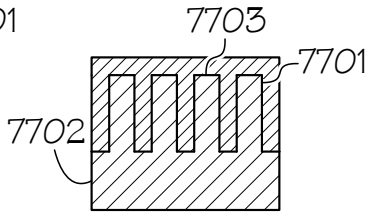

FIG. 78B

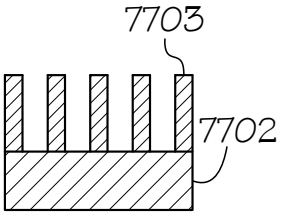

FIG. 78C

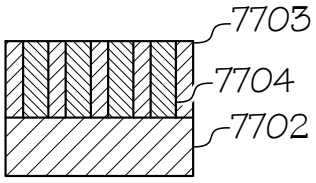

FIG. 78D

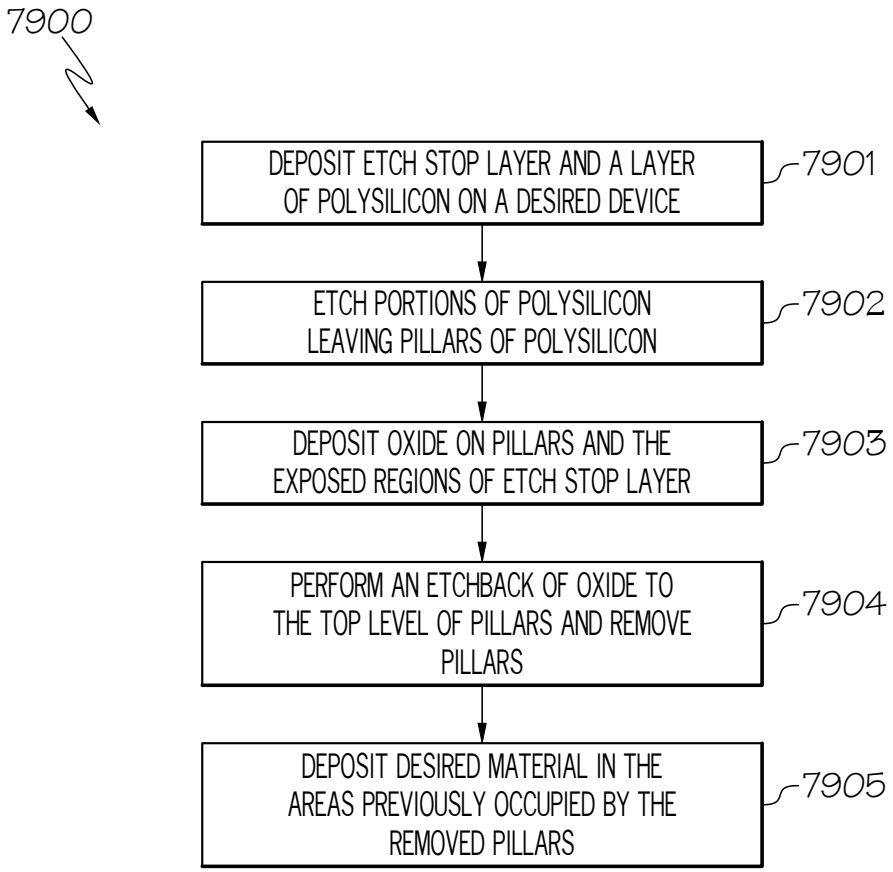
7900
DEPOSIT ETCH STOP LAYER AND A LAYER OF POLYSILICON ON A DESIRED DEVICE
7901
ETCH PORTIONS OF POLYSILICON LEAVING PILLARS OF POLYSILICON
7902
DEPOSIT OXIDE ON PILLARS AND THE EXPOSED REGIONS OF ETCH STOP LAYER
7903
PERFORM AN ETCHBACK OF OXIDE TO THE TOP LEVEL OF PILLARS AND REMOVE PILLARS
7904
DEPOSIT DESIRED MATERIAL IN THE AREAS PREVIOUSLY OCCUPIED BY THE REMOVED PILLARS
7905

FIG. 79

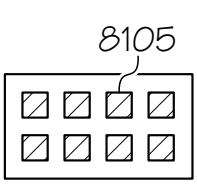

FIG. 80A

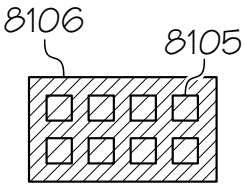

FIG. 80B

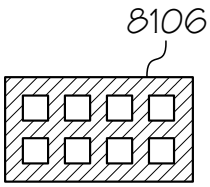

FIG. 80C

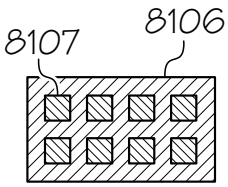

FIG. 80D

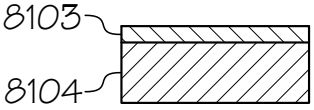

FIG. 81A

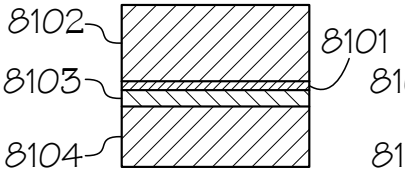

FIG. 81B

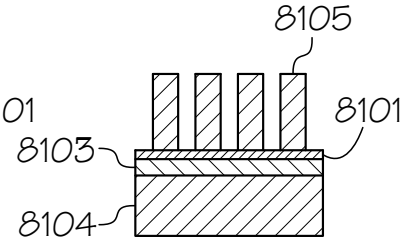

FIG. 81C

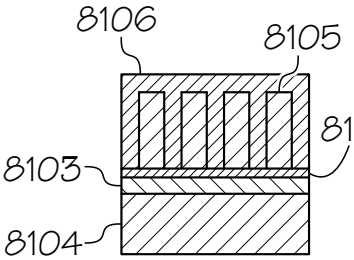

FIG. 81D

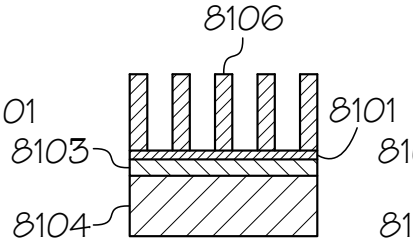

FIG. 81E

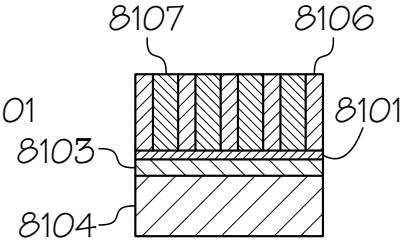

FIG. 81F

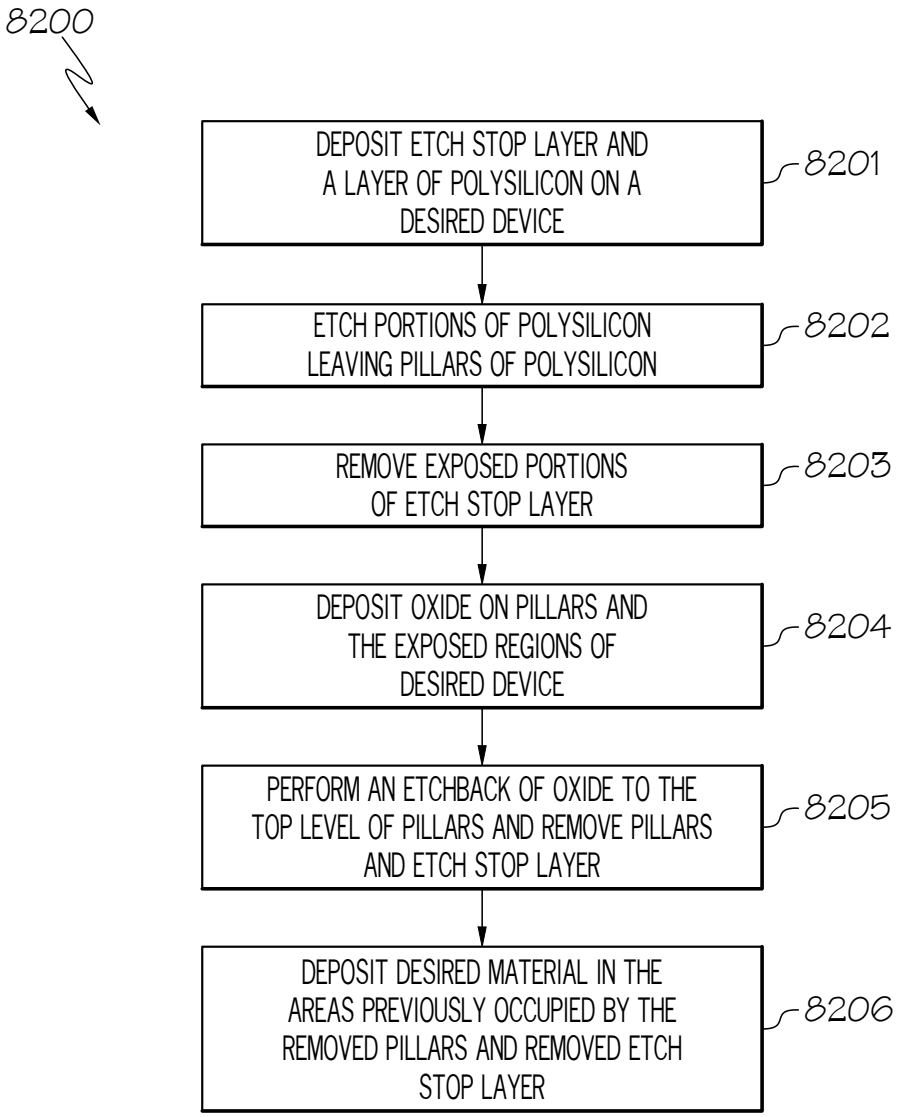
8200
DEPOSIT ETCH STOP LAYER AND A LAYER OF POLYSILICON ON A DESIRED DEVICE
8201
ETCH PORTIONS OF POLYSILICON LEAVING PILLARS OF POLYSILICON
8202
REMOVE EXPOSED PORTIONS OF ETCH STOP LAYER
8203
DEPOSIT OXIDE ON PILLARS AND THE EXPOSED REGIONS OF DESIRED DEVICE
8204
PERFORM AN ETCHBACK OF OXIDE TO THE TOP LEVEL OF PILLARS AND REMOVE PILLARS AND ETCH STOP LAYER
8205
DEPOSIT DESIRED MATERIAL IN THE AREAS PREVIOUSLY OCCUPIED BY THE REMOVED PILLARS AND REMOVED ETCH STOP LAYER
8206

FIG. 82

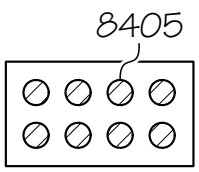

FIG. 83A

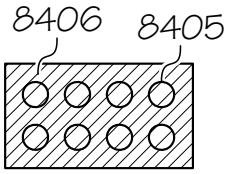

FIG. 83B

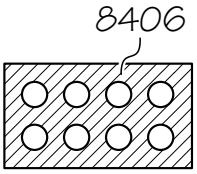

FIG. 83C

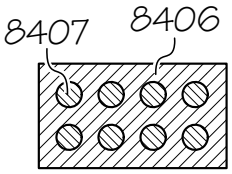

FIG. 83D

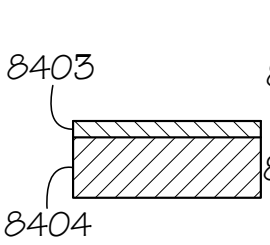

FIG. 84A

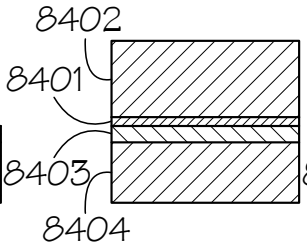

FIG. 84B

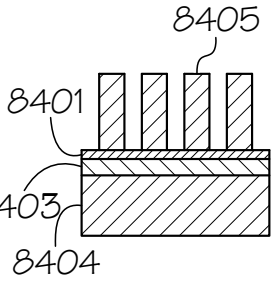

FIG. 84C

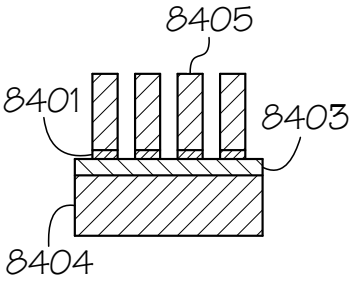

FIG. 84D

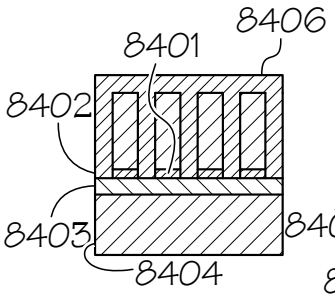

FIG. 84E

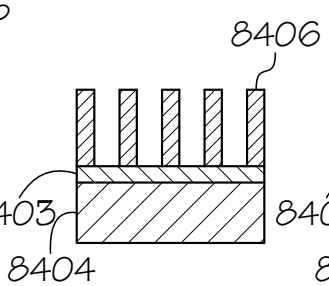

FIG. 84F

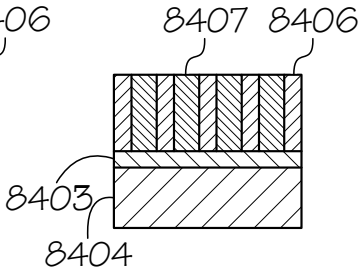

FIG. 84G

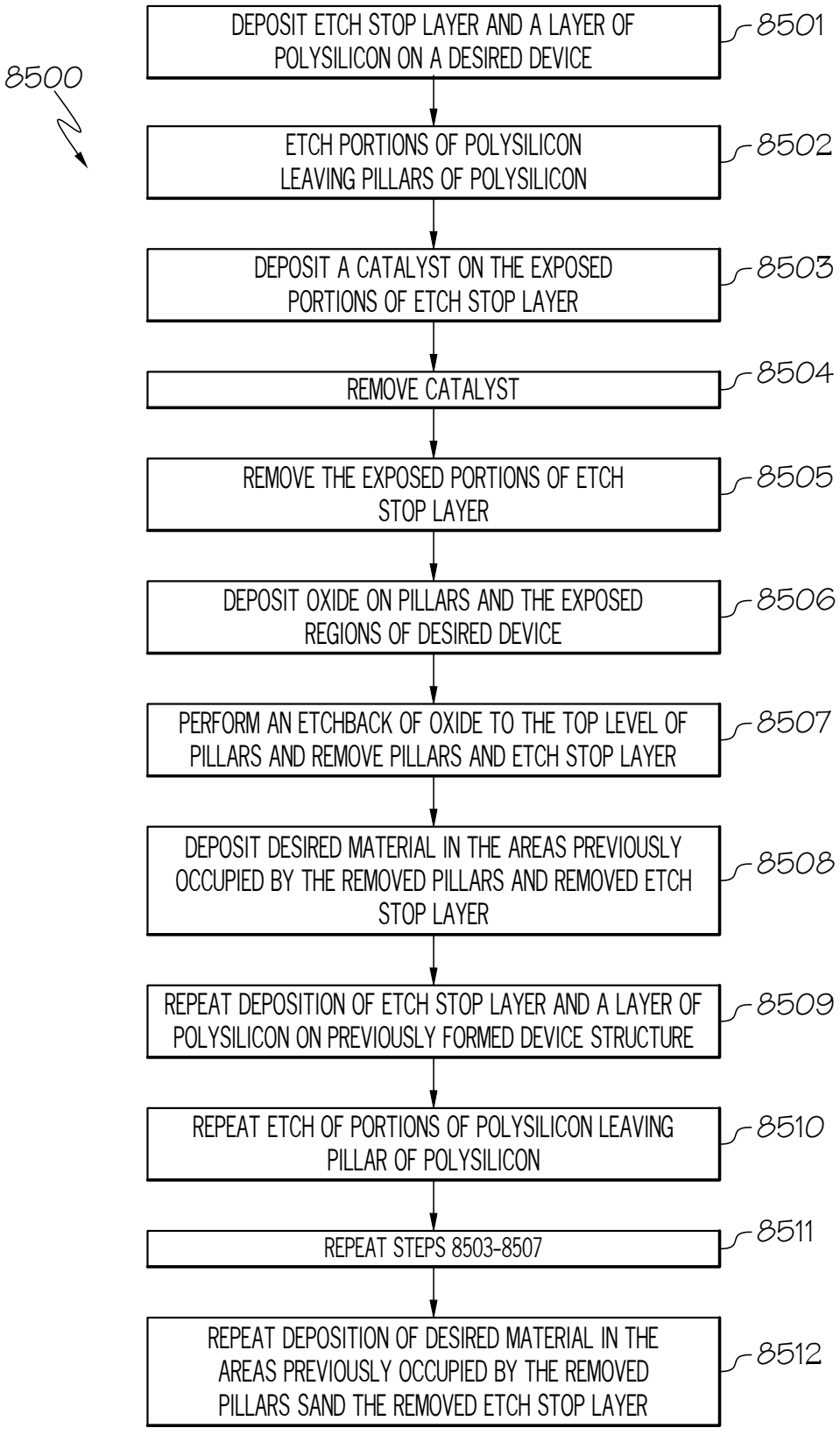
8500
DEPOSIT ETCH STOP LAYER AND A LAYER OF POLYSILICON ON A DESIRED DEVICE
8501
ETCH PORTIONS OF POLYSILICON LEAVING PILLARS OF POLYSILICON
8502
DEPOSIT A CATALYST ON THE EXPOSED PORTIONS OF ETCH STOP LAYER
8503
REMOVE CATALYST
8504
REMOVE THE EXPOSED PORTIONS OF ETCH STOP LAYER
8505
DEPOSIT OXIDE ON PILLARS AND THE EXPOSED REGIONS OF DESIRED DEVICE
8506
PERFORM AN ETCHBACK OF OXIDE TO THE TOP LEVEL OF PILLARS AND REMOVE PILLARS AND ETCH STOP LAYER
8507
DEPOSIT DESIRED MATERIAL IN THE AREAS PREVIOUSLY OCCUPIED BY THE REMOVED PILLARS AND REMOVED ETCH STOP LAYER
8508
REPEAT DEPOSITION OF ETCH STOP LAYER AND A LAYER OF POLYSILICON ON PREVIOUSLY FORMED DEVICE STRUCTURE
8509
REPEAT ETCH OF PORTIONS OF POLYSILICON LEAVING PILLAR OF POLYSILICON
8510
REPEAT STEPS 8503-8507
8511
REPEAT DEPOSITION OF DESIRED MATERIAL IN THE AREAS PREVIOUSLY OCCUPIED BY THE REMOVED PILLARS SAND THE REMOVED ETCH STOP LAYER
8512

FIG. 85

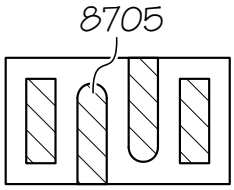

FIG. 86A

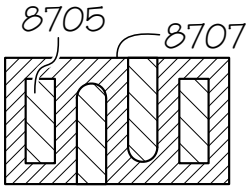

FIG. 86B

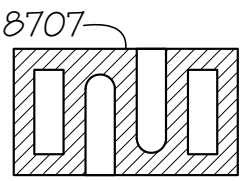

FIG. 86C

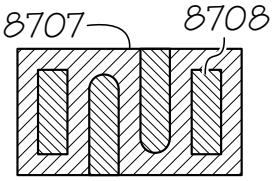

FIG. 86D

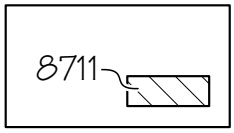

FIG. 86E

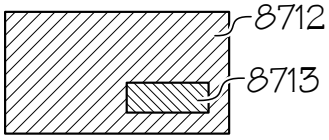

FIG. 86F

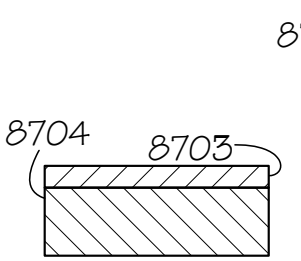

FIG. 87A

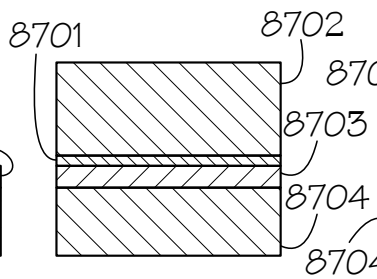

FIG. 87B

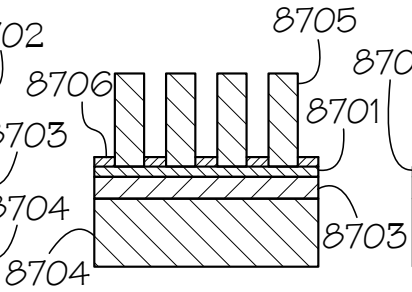

FIG. 87C

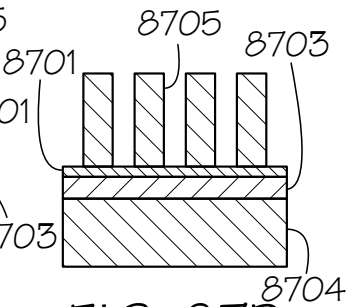

FIG. 87D

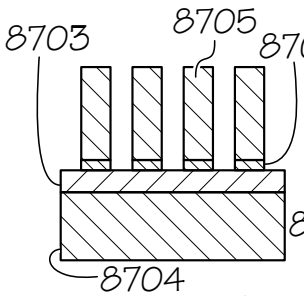

FIG. 87E

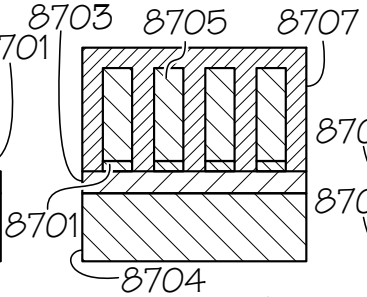

FIG. 87F

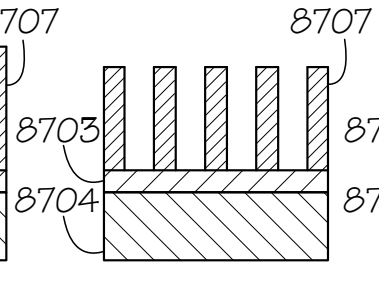

FIG. 87G

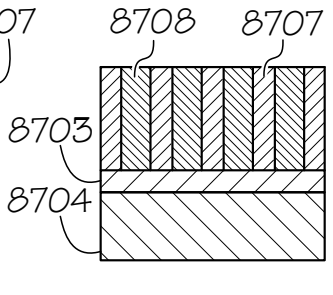

FIG. 87H

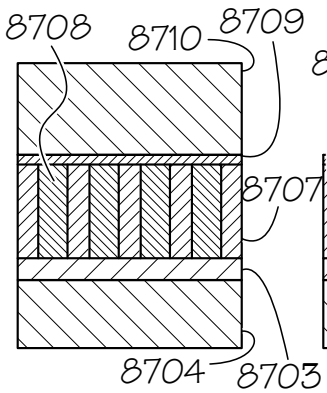

FIG. 87I

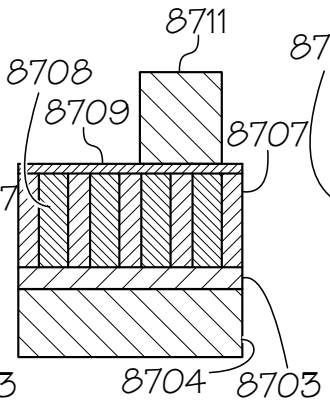

FIG. 87J

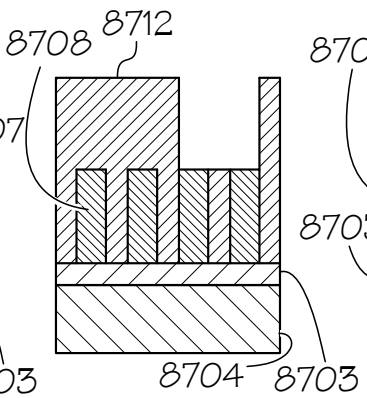

FIG. 87K

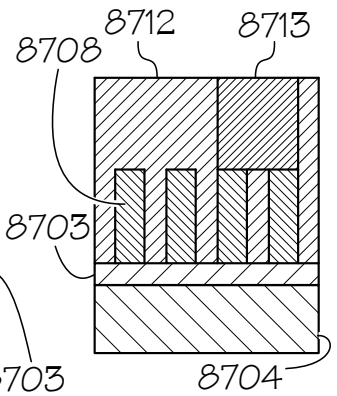

FIG. 87L

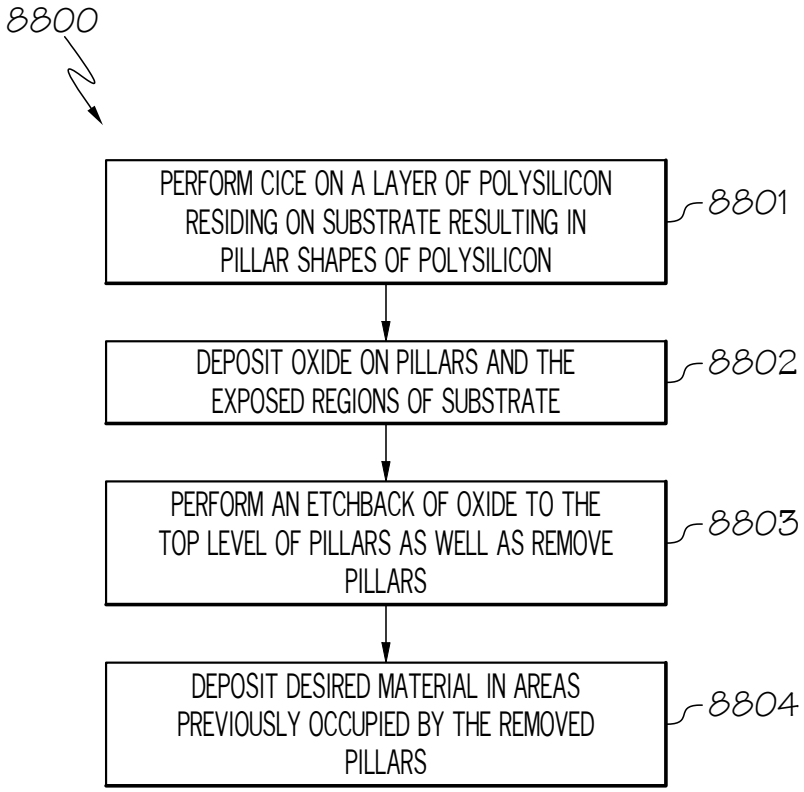
8800
PERFORM CICE ON A LAYER OF POLYSILICON RESIDING ON SUBSTRATE RESULTING IN PILLAR SHAPES OF POLYSILICON
8801
DEPOSIT OXIDE ON PILLARS AND THE EXPOSED REGIONS OF SUBSTRATE
8802
PERFORM AN ETCHBACK OF OXIDE TO THE TOP LEVEL OF PILLARS AS WELL AS REMOVE PILLARS
8803
DEPOSIT DESIRED MATERIAL IN AREAS PREVIOUSLY OCCUPIED BY THE REMOVED PILLARS
8804

FIG. 88

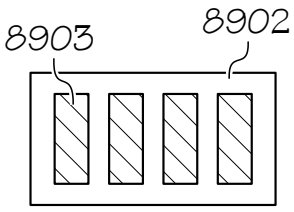

FIG. 89A

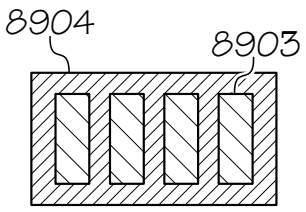

FIG. 89B

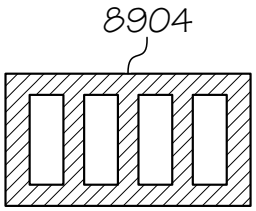

FIG. 89C

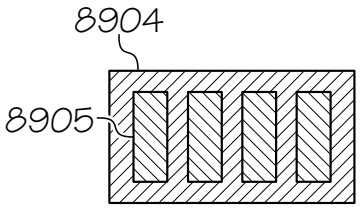

FIG. 89D

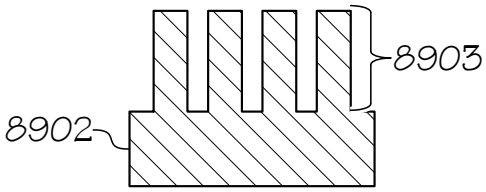

FIG. 90A

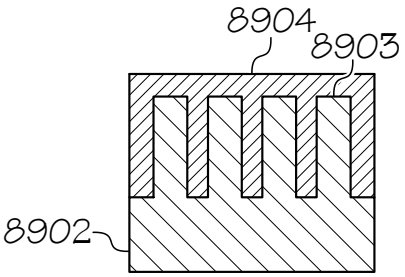

FIG. 90B

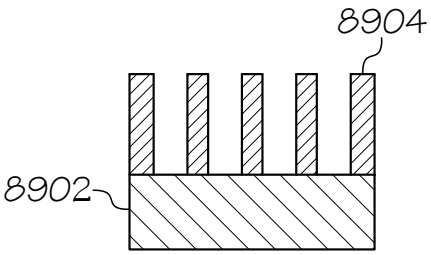

FIG. 90C

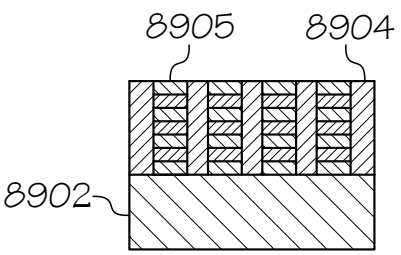

FIG. 90D

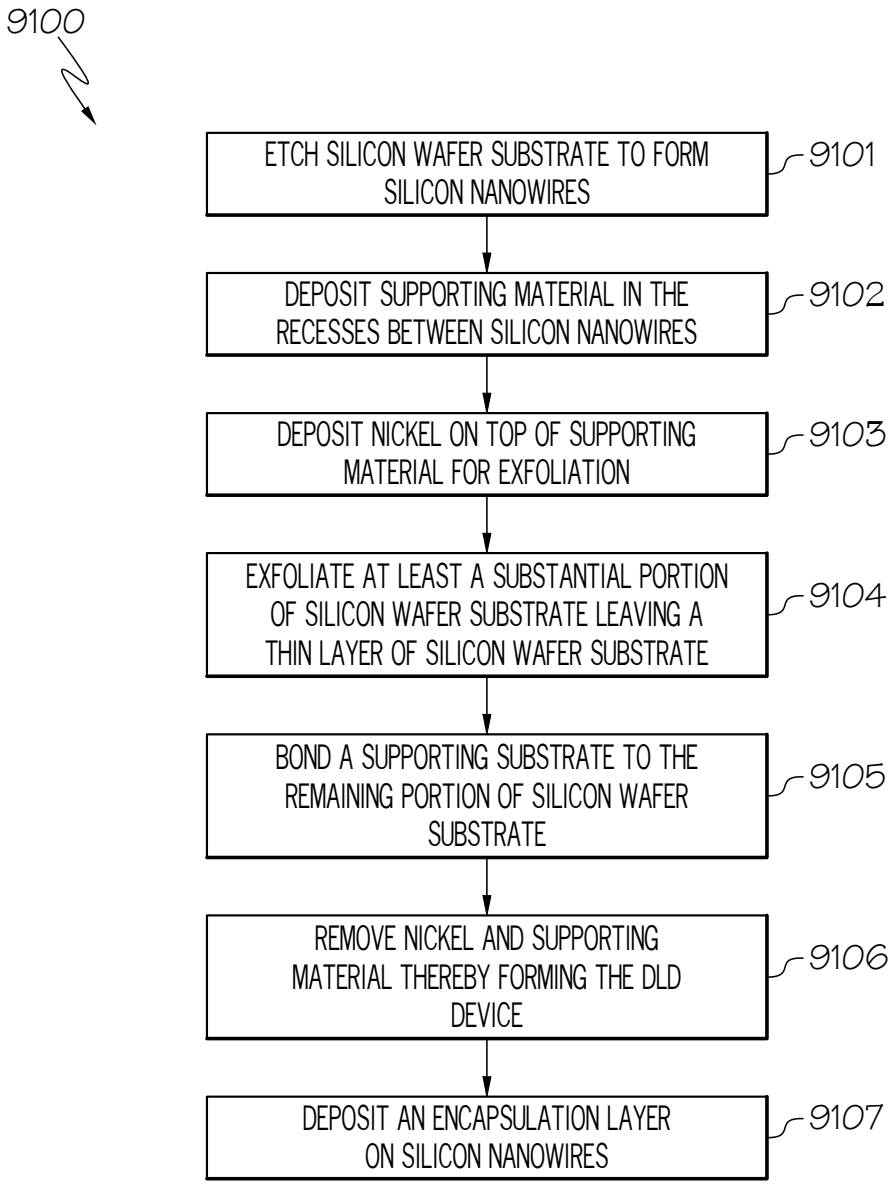
9100
ETCH SILICON WAFER SUBSTRATE TO FORM SILICON NANOWIRES
9101
DEPOSIT SUPPORTING MATERIAL IN THE RECESSES BETWEEN SILICON NANOWIRES
9102
DEPOSIT NICKEL ON TOP OF SUPPORTING MATERIAL FOR EXFOLIATION
9103
EXFOLIATE AT LEAST A SUBSTANTIAL PORTION OF SILICON WAFER SUBSTRATE LEAVING A THIN LAYER OF SILICON WAFER SUBSTRATE
9104
BOND A SUPPORTING SUBSTRATE TO THE REMAINING PORTION OF SILICON WAFER SUBSTRATE
9105
REMOVE NICKEL AND SUPPORTING MATERIAL THEREBY FORMING THE DLD DEVICE
9106
DEPOSIT AN ENCAPSULATION LAYER ON SILICON NANOWIRES
9107

FIG. 91

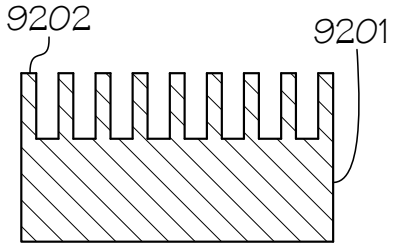

FIG. 92A

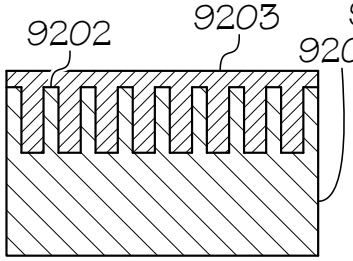

FIG. 92B

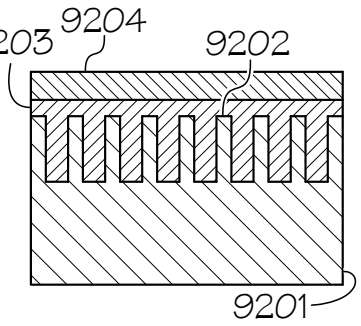

FIG. 92C

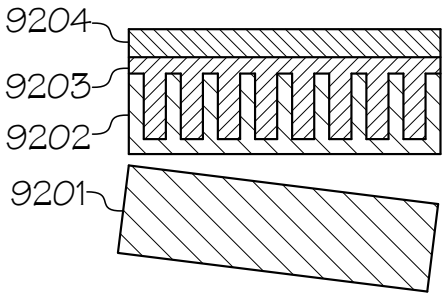

FIG. 92D

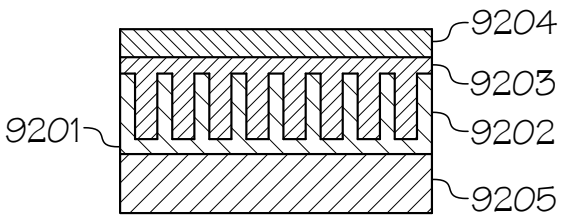

FIG. 92E

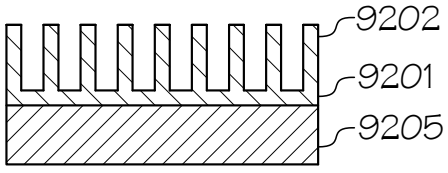

FIG. 92F

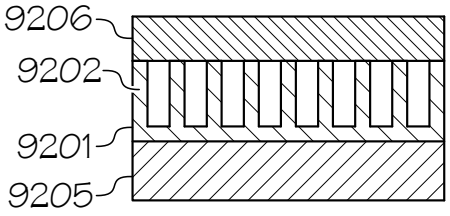

FIG. 92G

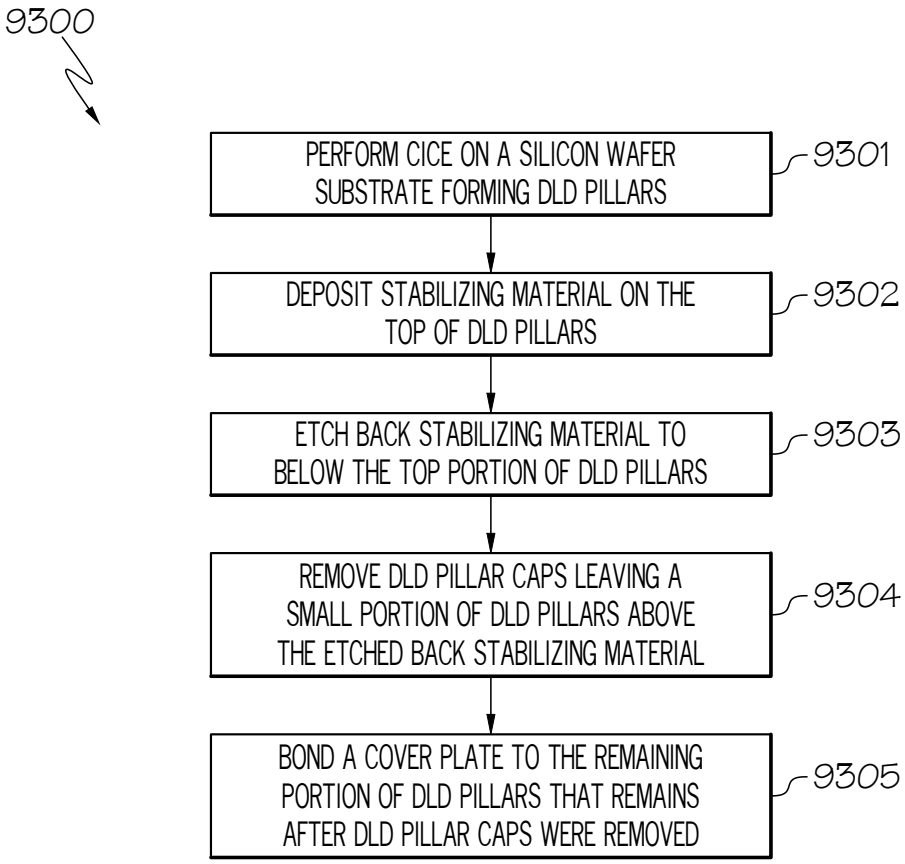
9300
PERFORM CICE ON A SILICON WAFER SUBSTRATE FORMING DLD PILLARS
9301
DEPOSIT STABILIZING MATERIAL ON THE TOP OF DLD PILLARS
9302
ETCH BACK STABILIZING MATERIAL TO BELOW THE TOP PORTION OF DLD PILLARS
9303
REMOVE DLD PILLAR CAPS LEAVING A SMALL PORTION OF DLD PILLARS ABOVE THE ETCHED BACK STABILIZING MATERIAL
9304
BOND A COVER PLATE TO THE REMAINING PORTION OF DLD PILLARS THAT REMAINS AFTER DLD PILLAR CAPS WERE REMOVED
9305

FIG. 93

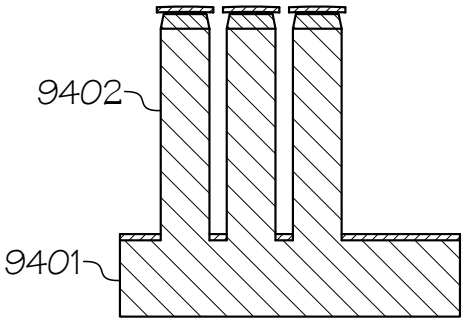

FIG. 94A

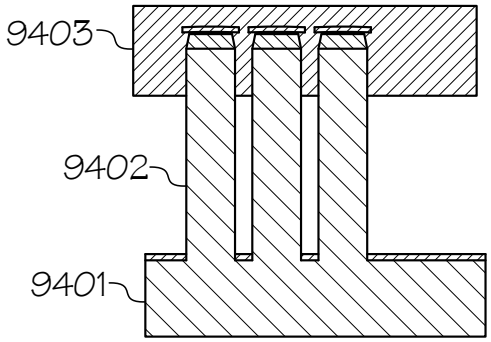

FIG. 94B

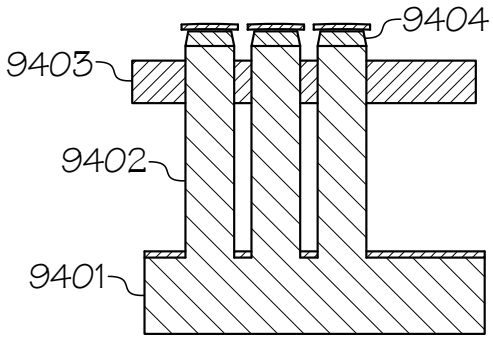

FIG. 94C

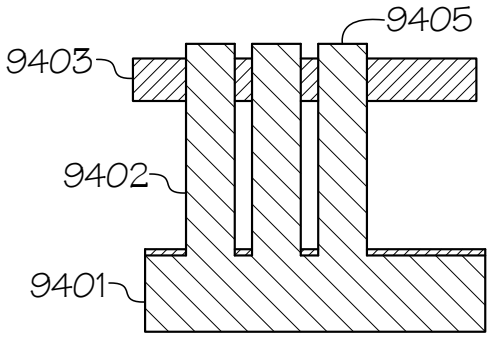

FIG. 94D

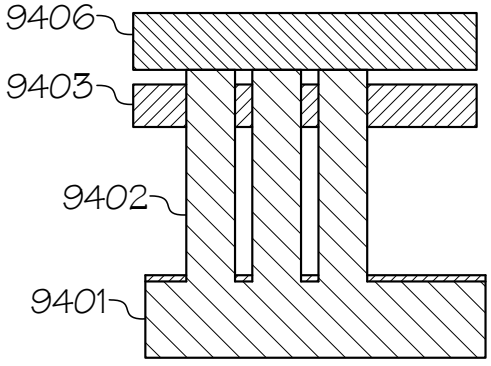

FIG. 94E

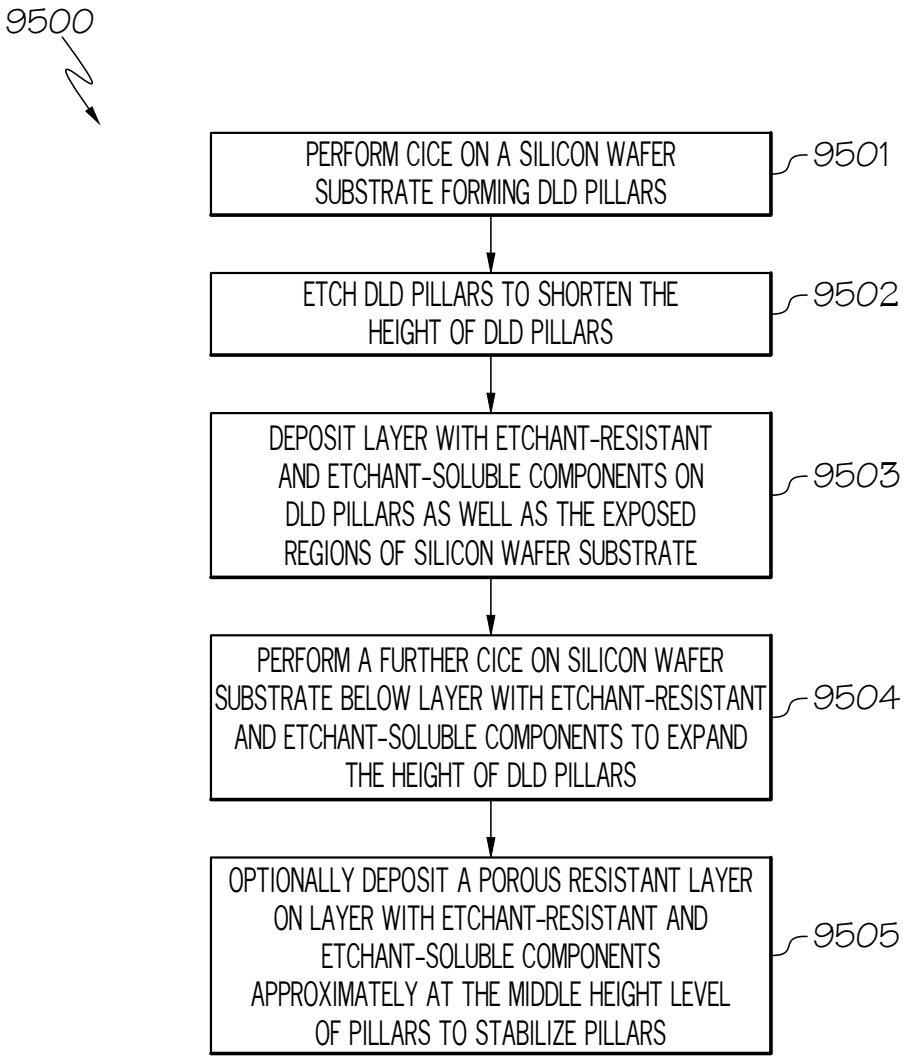
9500
PERFORM CICE ON A SILICON WAFER SUBSTRATE FORMING DLD PILLARS
9501
ETCH DLD PILLARS TO SHORTEN THE HEIGHT OF DLD PILLARS
9502
DEPOSIT LAYER WITH ETCHANT-RESISTANT AND ETCHANT-SOLUBLE COMPONENTS ON DLD PILLARS AS WELL AS THE EXPOSED REGIONS OF SILICON WAFER SUBSTRATE
9503
PERFORM A FURTHER CICE ON SILICON WAFER SUBSTRATE BELOW LAYER WITH ETCHANT-RESISTANT AND ETCHANT-SOLUBLE COMPONENTS TO EXPAND THE HEIGHT OF DLD PILLARS
9504
OPTIONALLY DEPOSIT A POROUS RESISTANT LAYER ON LAYER WITH ETCHANT-RESISTANT AND ETCHANT-SOLUBLE COMPONENTS APPROXIMATELY AT THE MIDDLE HEIGHT LEVEL OF PILLARS TO STABILIZE PILLARS
9505

FIG. 95

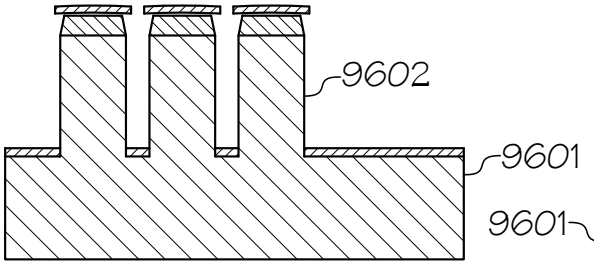

FIG. 96A

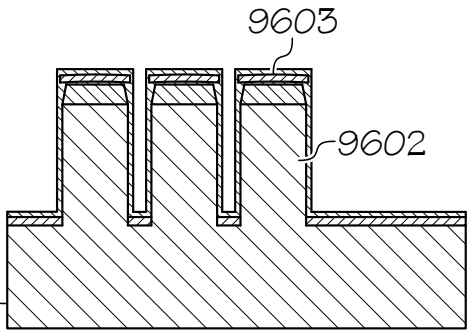

FIG. 96B

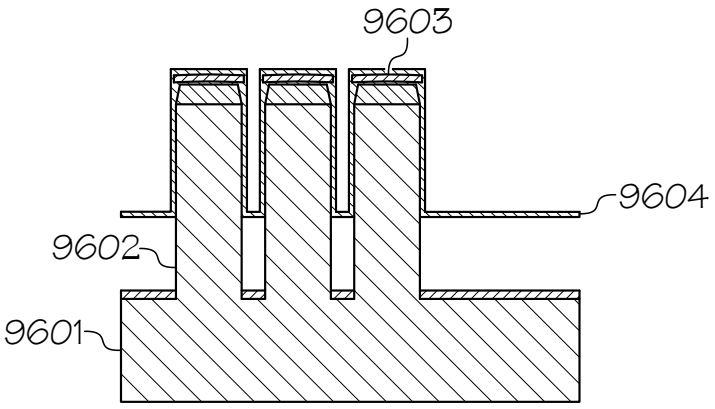

FIG. 96C

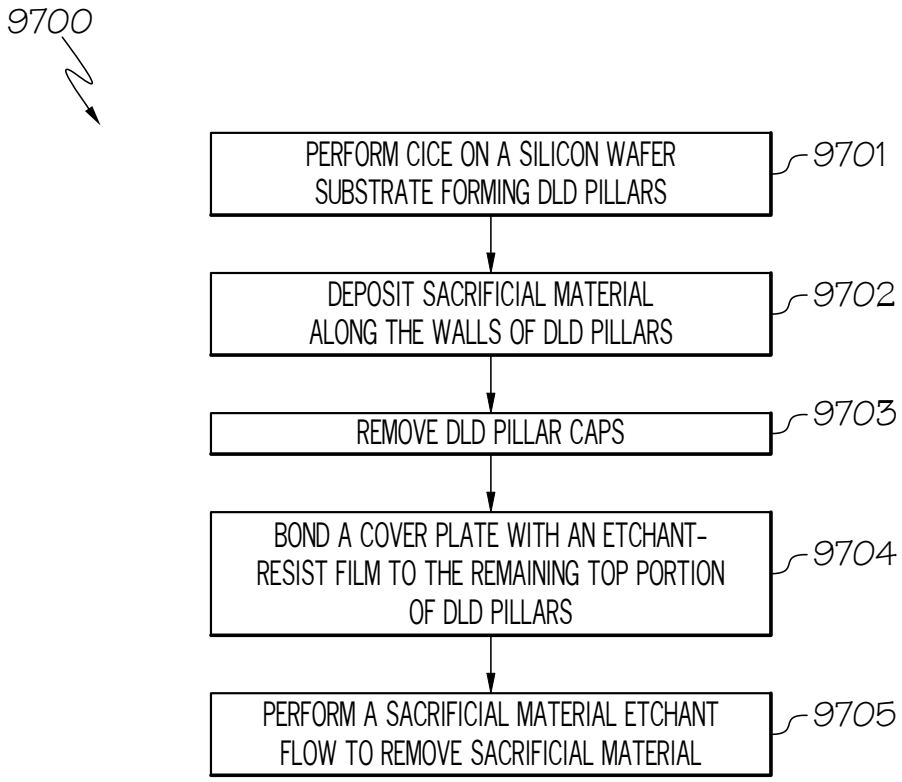
9700
PERFORM CICE ON A SILICON WAFER SUBSTRATE FORMING DLD PILLARS
9701
DEPOSIT SACRIFICIAL MATERIAL ALONG THE WALLS OF DLD PILLARS
9702
REMOVE DLD PILLAR CAPS
9703
BOND A COVER PLATE WITH AN ETCHANT-RESIST FILM TO THE REMAINING TOP PORTION OF DLD PILLARS
9704
PERFORM A SACRIFICIAL MATERIAL ETCHANT FLOW TO REMOVE SACRIFICIAL MATERIAL
9705

FIG. 97

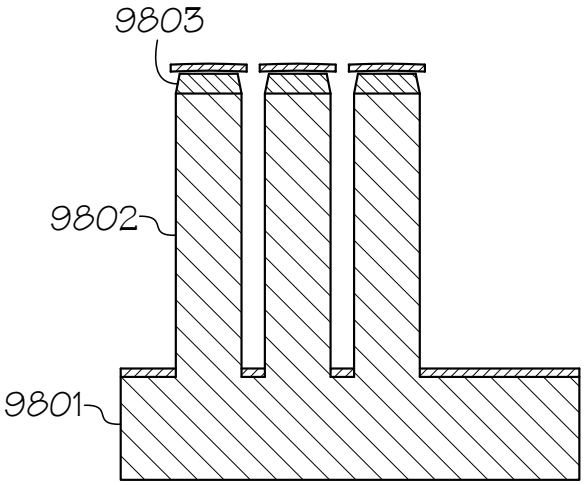

FIG. 98A

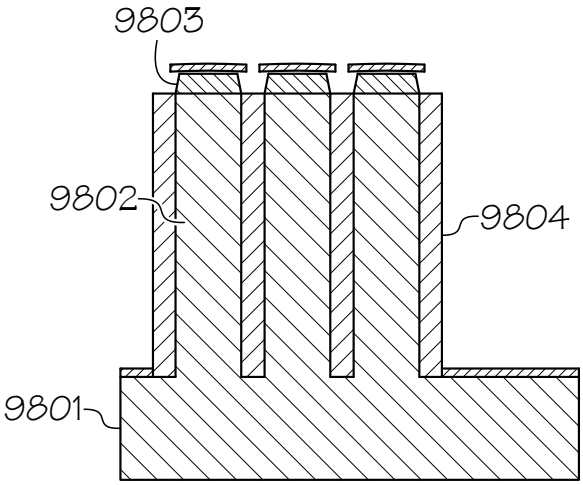

FIG. 98B

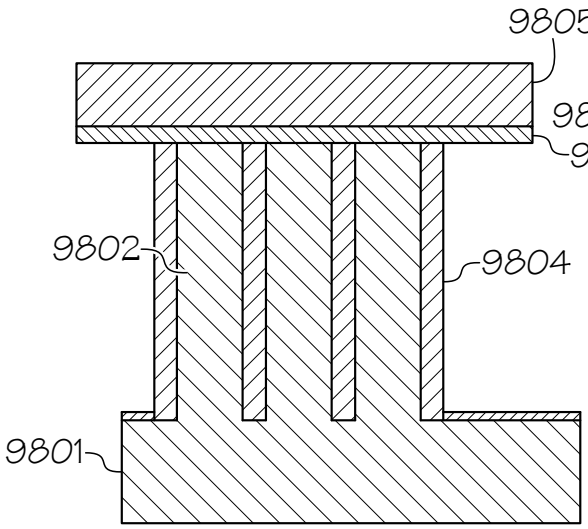

FIG. 98C

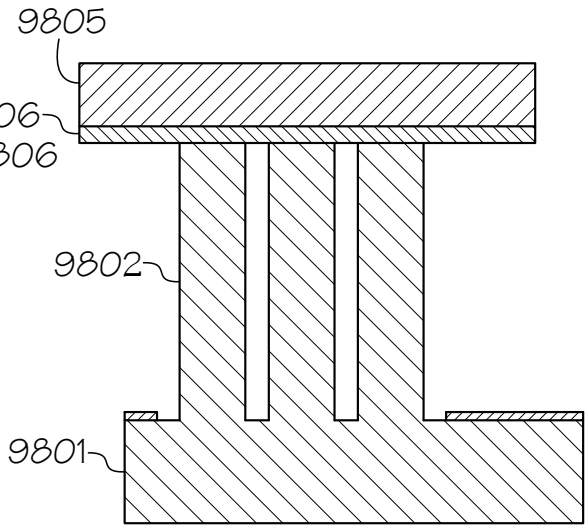

FIG. 98D

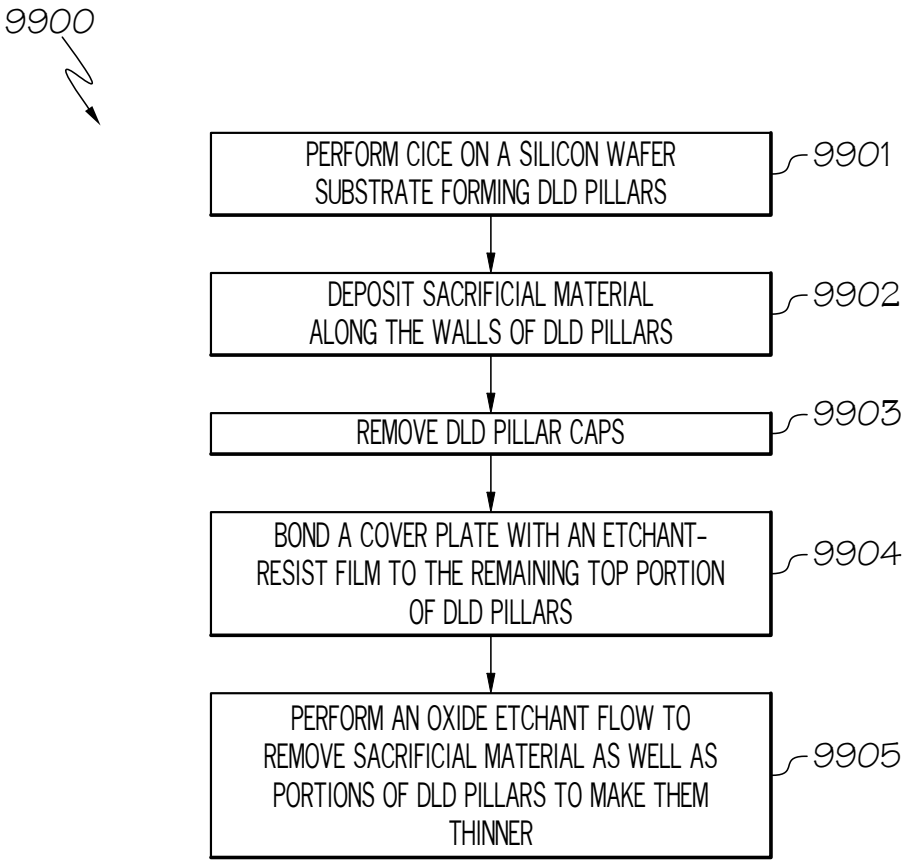
9900
PERFORM CICE ON A SILICON WAFER SUBSTRATE FORMING DLD PILLARS
9901
DEPOSIT SACRIFICIAL MATERIAL ALONG THE WALLS OF DLD PILLARS
9902
REMOVE DLD PILLAR CAPS
9903
BOND A COVER PLATE WITH AN ETCHANT-RESIST FILM TO THE REMAINING TOP PORTION OF DLD PILLARS
9904
PERFORM AN OXIDE ETCHANT FLOW TO REMOVE SACRIFICIAL MATERIAL AS WELL AS PORTIONS OF DLD PILLARS TO MAKE THEM THINNER
9905

FIG. 99

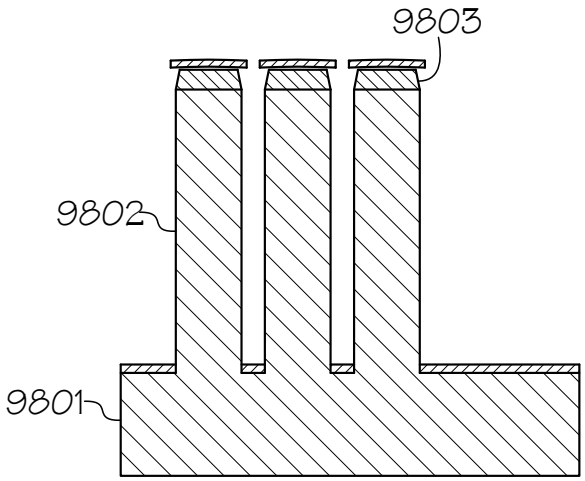

FIG. 100A

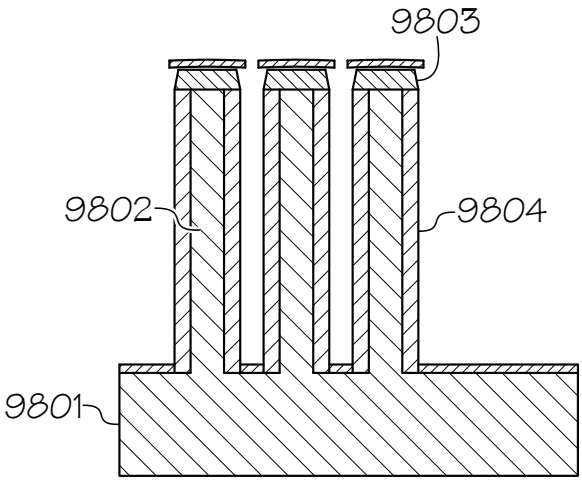

FIG. 100B

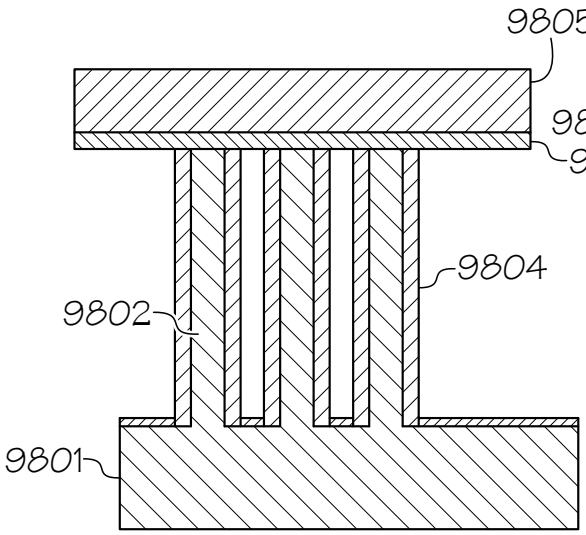

FIG. 100C

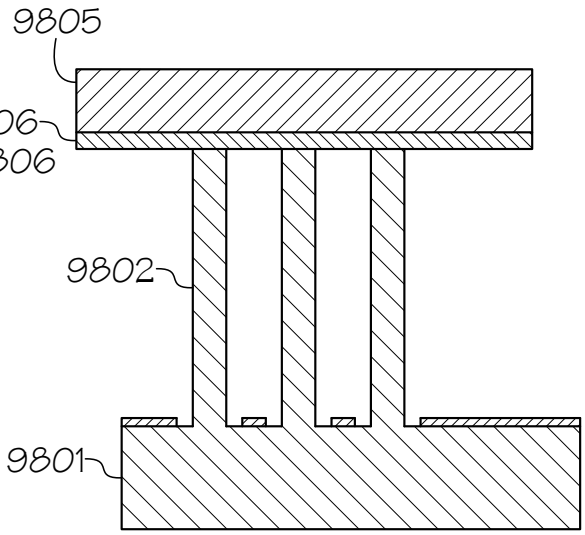

FIG. 100D

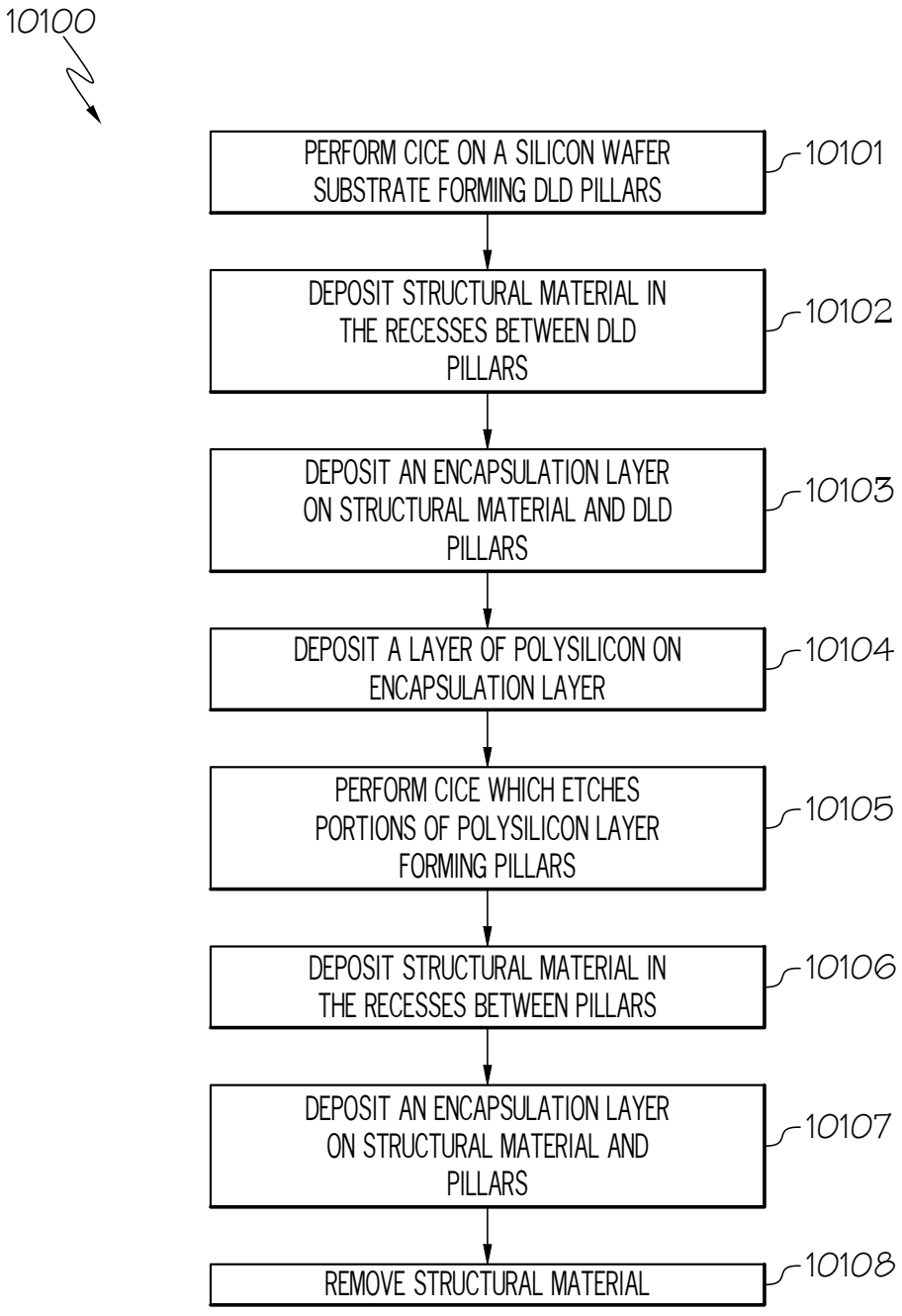
10100
PERFORM CICE ON A SILICON WAFER SUBSTRATE FORMING DLD PILLARS
10101
DEPOSIT STRUCTURAL MATERIAL IN THE RECESSES BETWEEN DLD PILLARS
10102
DEPOSIT AN ENCAPSULATION LAYER ON STRUCTURAL MATERIAL AND DLD PILLARS
10103
DEPOSIT A LAYER OF POLYSILICON ON ENCAPSULATION LAYER
10104
PERFORM CICE WHICH ETCHES PORTIONS OF POLYSILICON LAYER FORMING PILLARS
10105
DEPOSIT STRUCTURAL MATERIAL IN THE RECESSES BETWEEN PILLARS
10106
DEPOSIT AN ENCAPSULATION LAYER ON STRUCTURAL MATERIAL AND PILLARS
10107
REMOVE STRUCTURAL MATERIAL
10108

FIG. 101

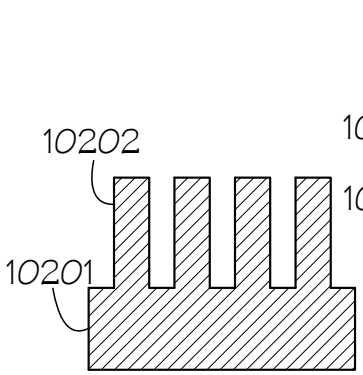

FIG. 102A

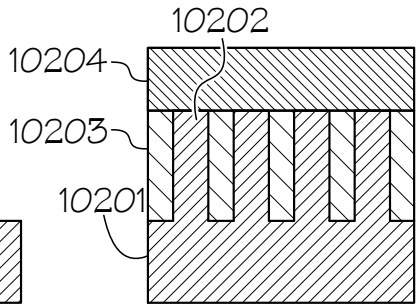

FIG. 102B

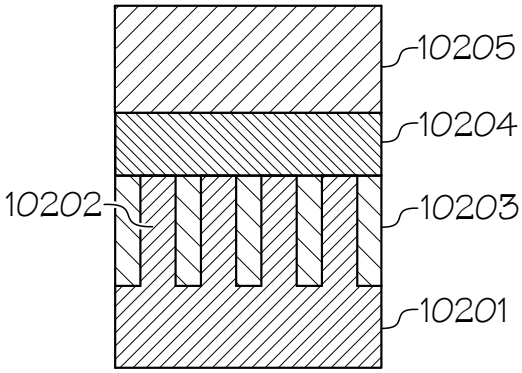

FIG. 102C

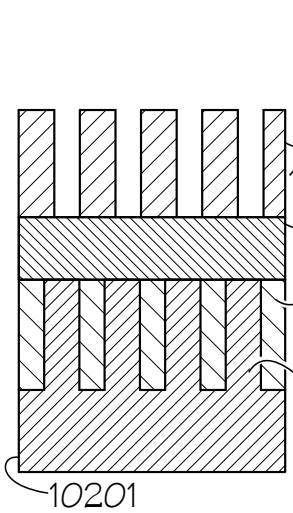

FIG. 102D

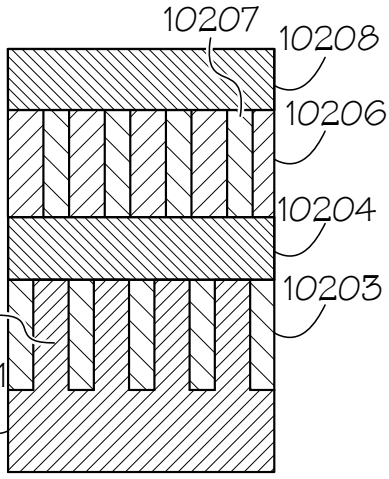

FIG. 102E

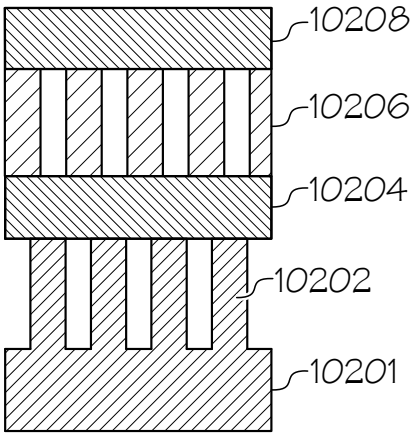

FIG. 102F

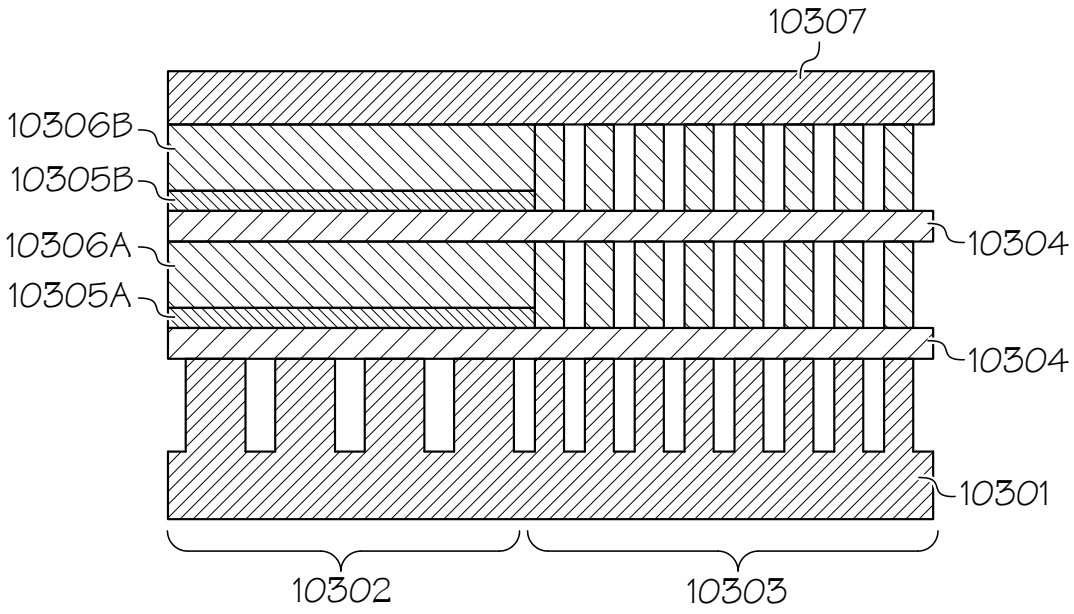
10307
10306B
10305B
10306A
10305A
10304
10304
10301
10302
10303

FIG. 103

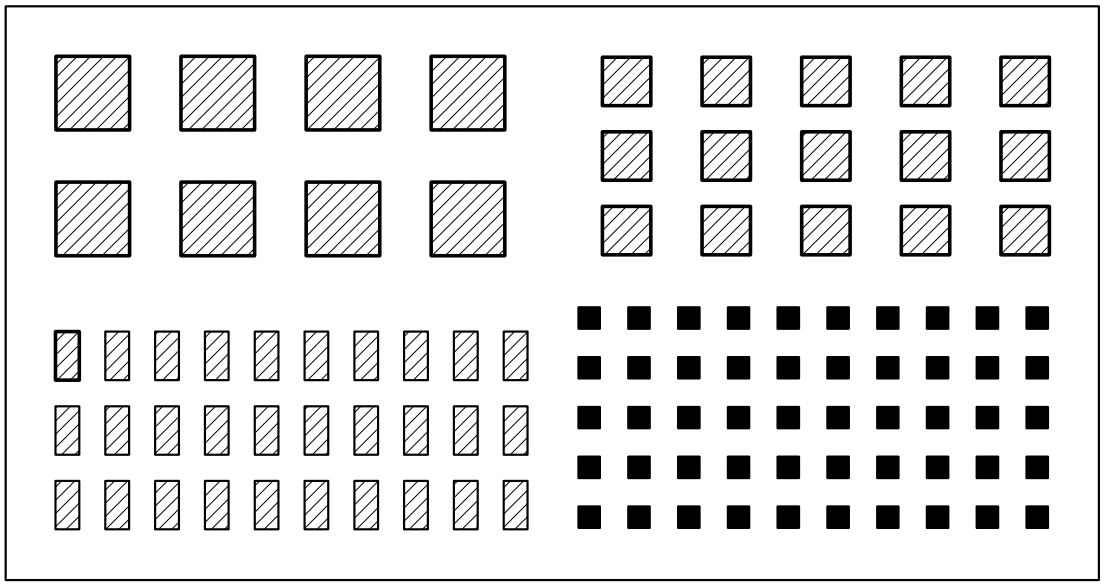

FIG. 104

DIGITAL OUTPUT
ANALOG OUTPUT
BIAS GENERATION & DACS (OPT)
A/D CONVERSION (OPT)
ANALOG AMPLIFICATION
PIXEL ARRAY
HORIZONTAL SCANNER / COLUMN BUFFERS
VERTICAL SCANNER FOR ROW SELECTION
CONTROL & TIMING LOGIC (OPT)
BSI SENSOR
MEMORY
LOGIC

FIG. 105

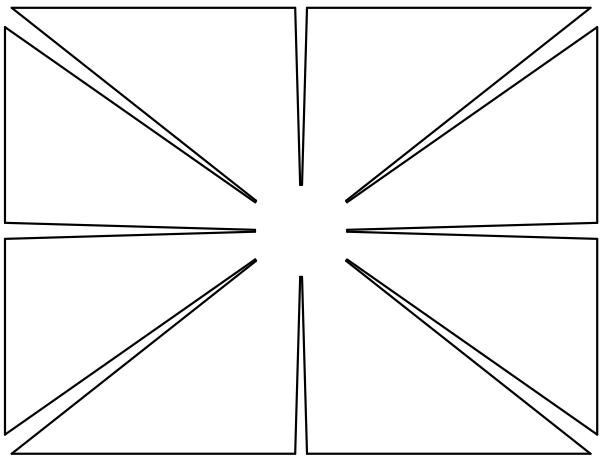

FIG. 106