

PHASE LOCKED LOOP USING
DELAY COMPENSATION TECHNIQUES

ABSTRACT

A phase locked loop circuit for eliminating loop latency includes an input circuit for inputting a phase signal corresponding to phase changes and an actual phase
5 signal corresponding to actual phase sampling of a sampling clock, a filter circuit for connecting the phase signal and the actual phase signal to a phase update signal, and a feedback circuit to eliminate the loop latency by feeding back to the filter circuit a portion of the phase update signal.

Figure 4.

This Sheet Has Been Replaced

