FIG. 1

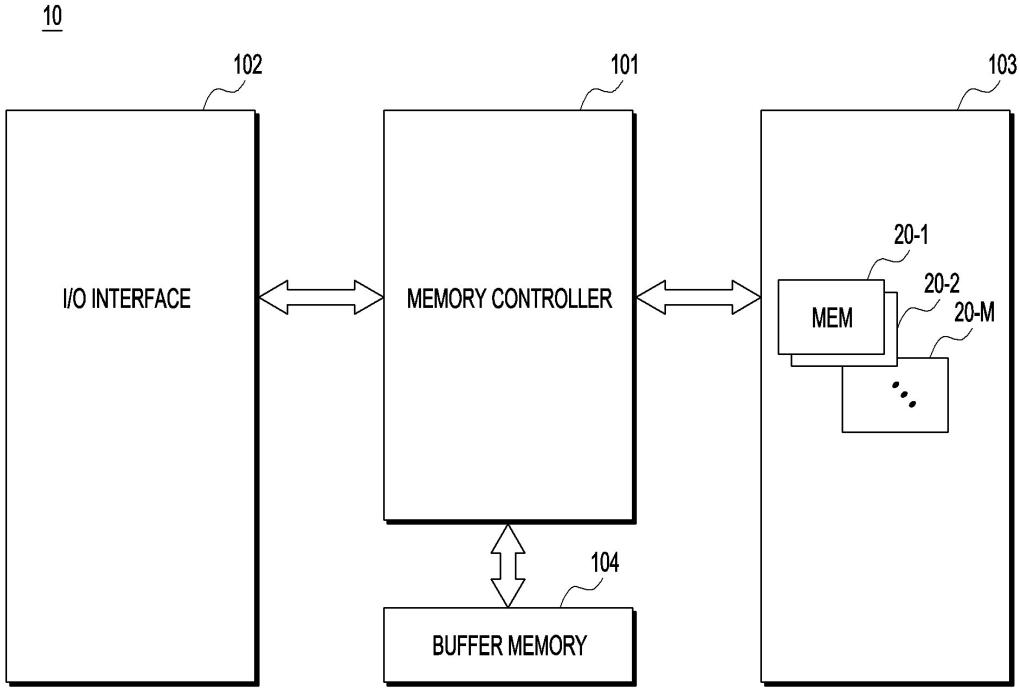

10
102
101
103
I/O INTERFACE
MEMORY CONTROLLER
20-1
20-2
20-M
MEM
104
BUFFER MEMORY

FIG. 2

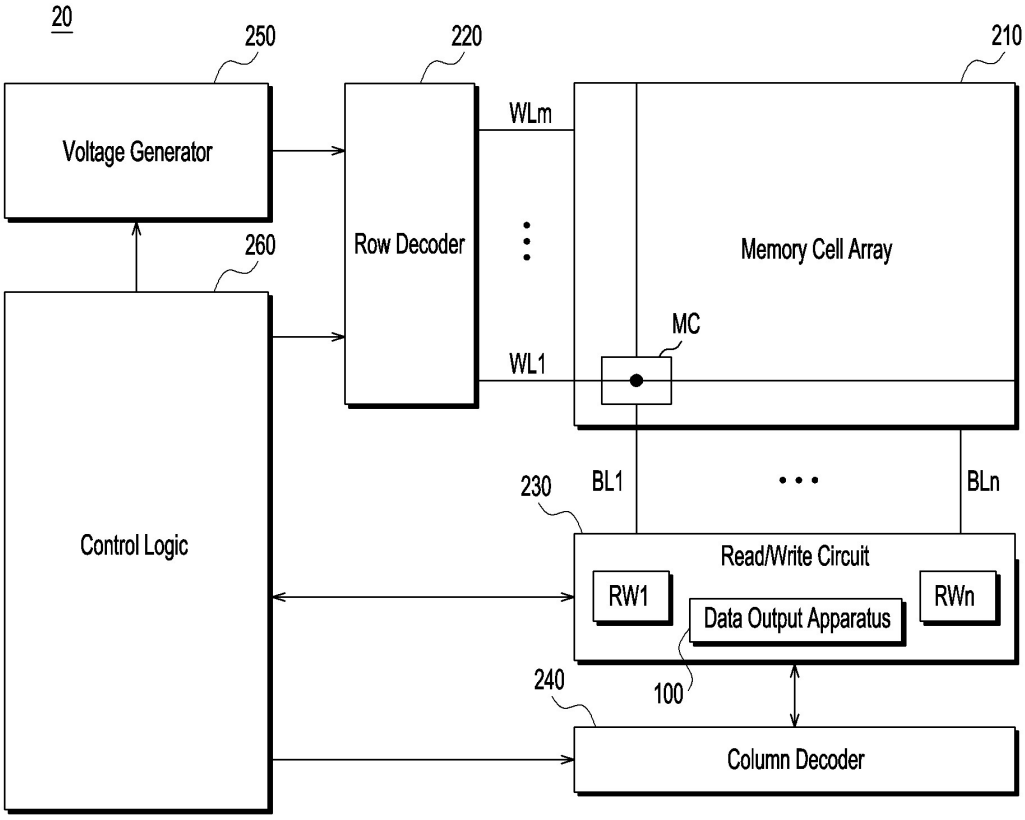

20
250
220
210
Voltage Generator
WLm
Row Decoder
Memory Cell Array
260
MC
WL1
230
BL1
BLn
Control Logic
Read/Write Circuit
RW1
RWn
Data Output Apparatus
100
240
Column Decoder

FIG. 3

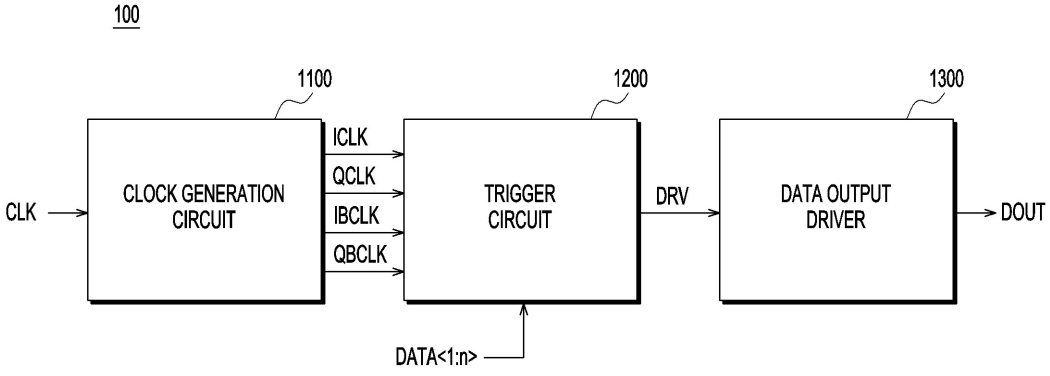

100
1100
1200
1300
CLK
CLOCK GENERATION CIRCUIT
ICLK
QCLK
IBCLK
QBCLK
TRIGGER CIRCUIT
DRV
DATA OUTPUT DRIVER
DOUT
DATA<1:n>

FIG. 4

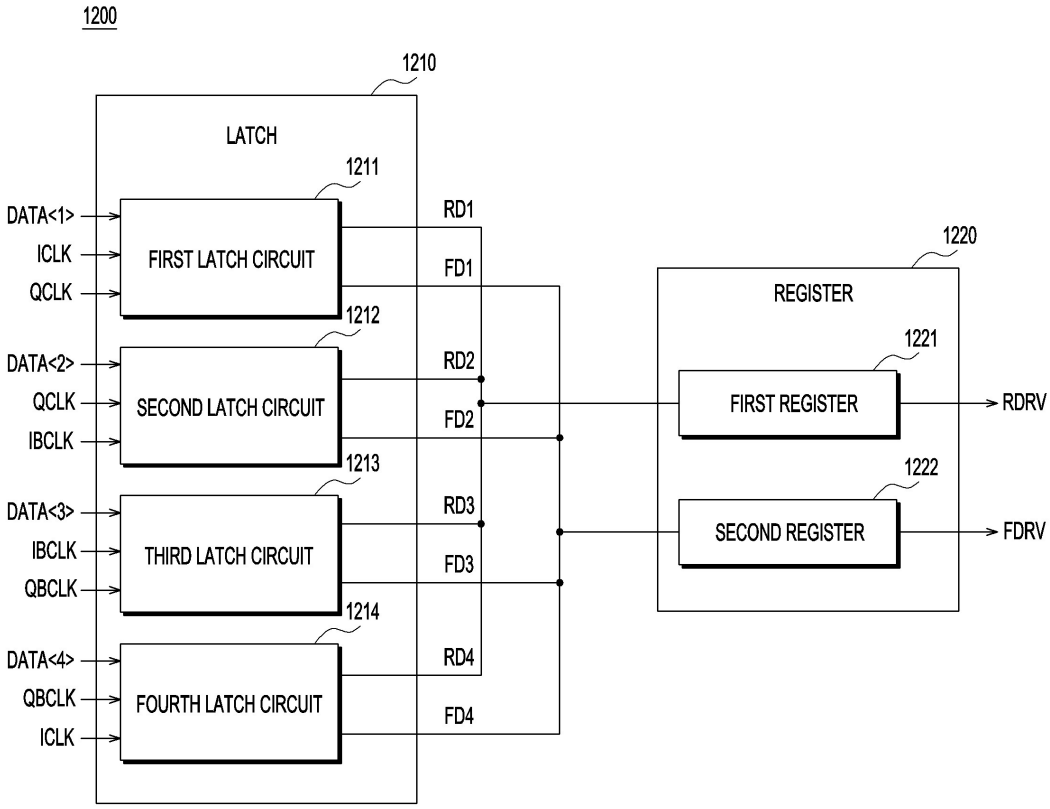

1200
1210
LATCH
1211
FIRST LATCH CIRCUIT
1212
SECOND LATCH CIRCUIT
1213
THIRD LATCH CIRCUIT
1214
FOURTH LATCH CIRCUIT
DATA<1>
ICLK
QCLK
DATA<2>
QCLK
IBCLK
DATA<3>
IBCLK
QBCLK
DATA<4>
QBCLK
ICLK
RD1
FD1
RD2
FD2
RD3
FD3
RD4
FD4
1220
REGISTER
1221
FIRST REGISTER
1222
SECOND REGISTER
RDRV
FDRV

FIG. 5

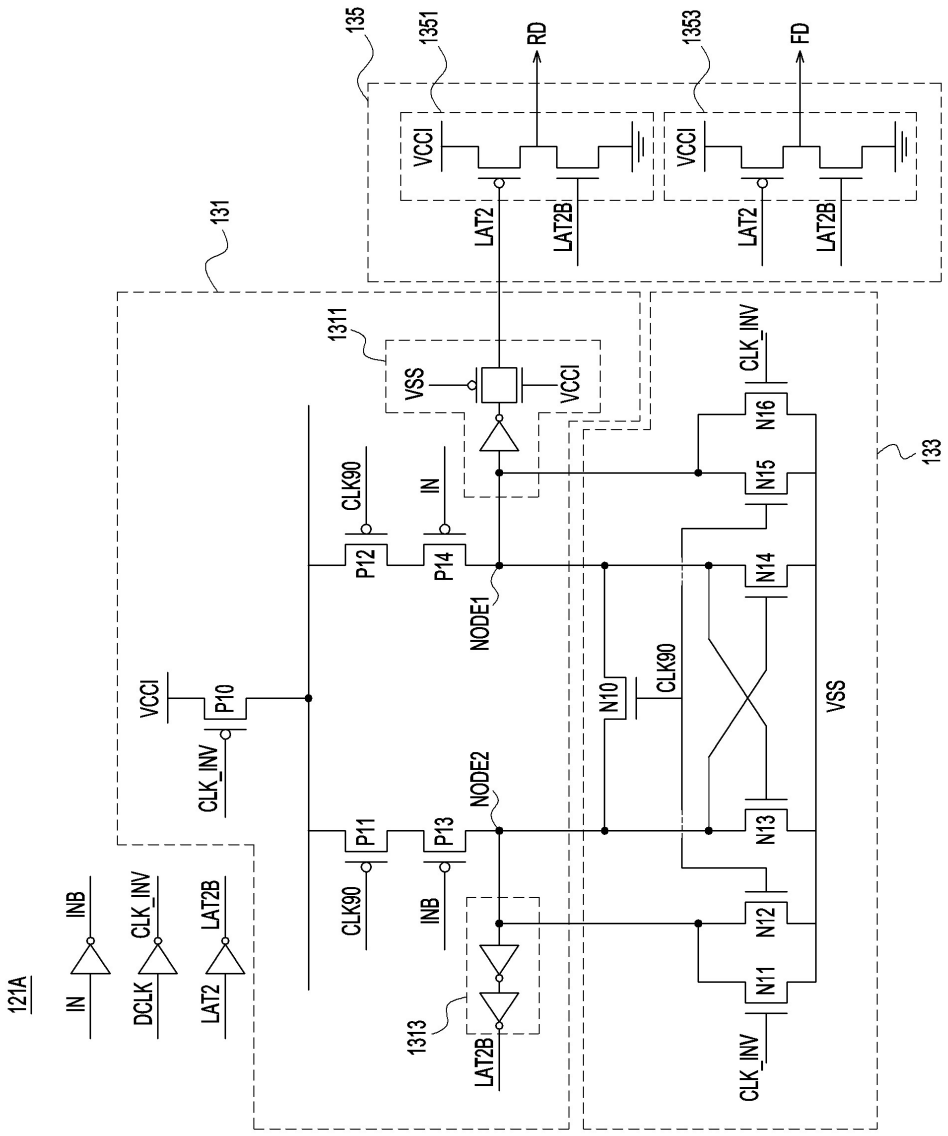

121A
IN
INB
DCLK
CLK_INV
LAT2
LAT2B
131
135
1351
1353
RD
FD
VCCI
LAT2
LAT2B
1311
VSS
VCCI
CLK90
IN
P12
P14
NODE1
P10
CLK_INV
P11
P13
NODE2
CLK90
INB
1313
LAT2B
N10
CLK90
CLK_INV
N16
N15
N14
N13
N12
N11
CLK_INV
VSS
133

FIG. 6

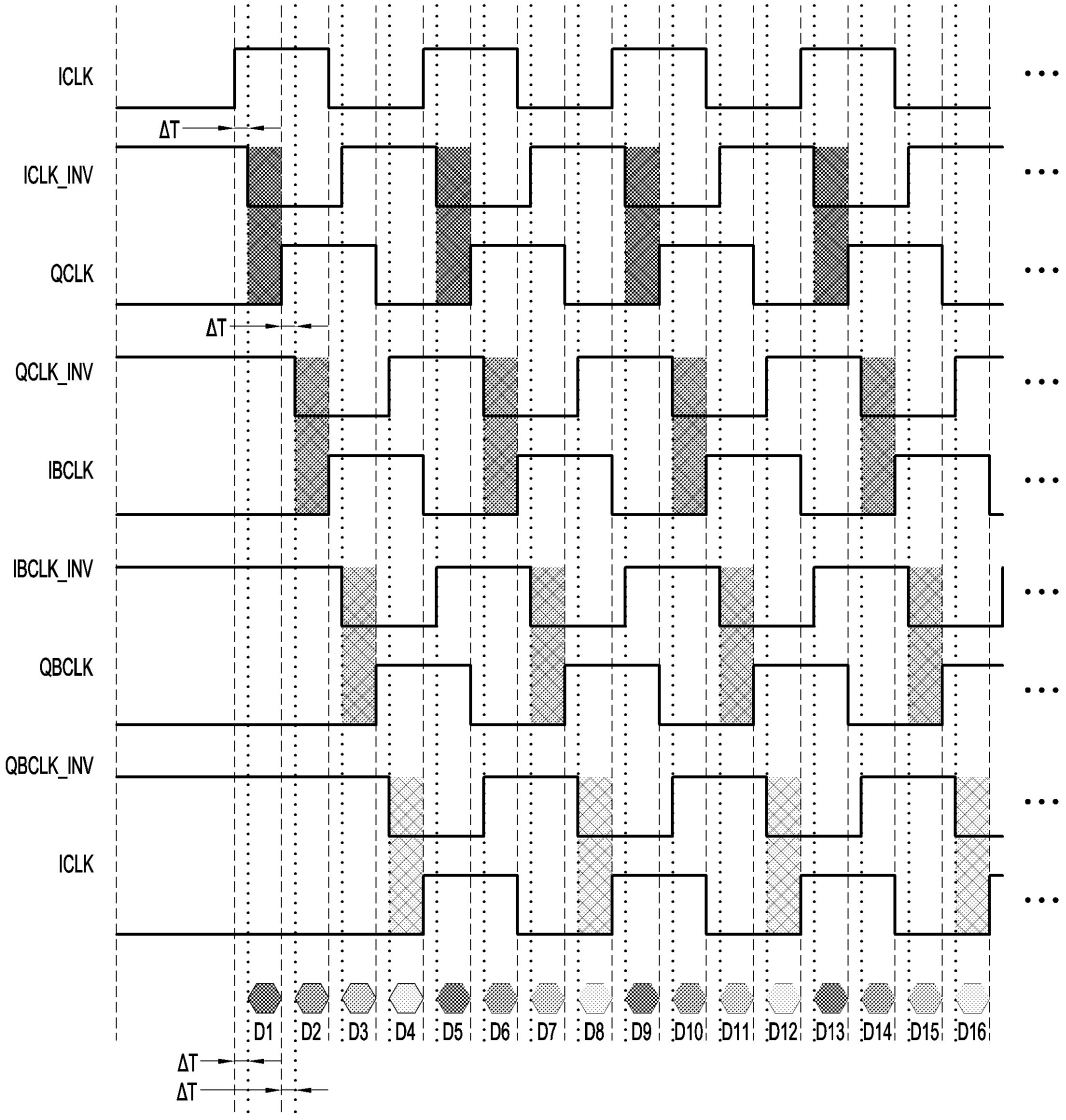

ICLK
ΔT
ICLK_INV
QCLK
ΔT
QCLK_INV
IBCLK
IBCLK_INV
QBCLK
QBCLK_INV
ICLK
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
ΔT
ΔT

FIG. 7

