TITLE OF THE INVENTION

SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device, and particularly, to a semiconductor device including a sealing resin for sealing a semiconductor chip.

2. Description of the Related Art

There are many kinds of semiconductor devices. For example, in one kind of semiconductor device, a semiconductor chip is electrically connected to connection pads arranged on a substrate (including a tape-like substrate), and a sealing resin is applied to seal the semiconductor chip. In another kind of semiconductor device, a portion of a lead frame is used as a connection pad, a semiconductor chip is electrically connected to the connection pad portion of the lead frame, and a sealing resin is applied to seal the semiconductor chip.

FIG. 1 is a cross-sectional view of a semiconductor device of the related art.

FIG. 2 is a top view of the semiconductor device shown in FIG. 1.

Referring to FIG. 1 and FIG. 2, a semiconductor device 100 includes a lead frame 101, a semiconductor chip 102, and sealing resin 103.

The lead frame 101 includes a chip supporter 105 on which the semiconductor chip 102 is disposed, and plural terminal portions 106 for connecting with wires 107 which are electrically connected to the semiconductor chip 102. The terminal portions 106 are external connection terminals for connecting the semiconductor device 100 to a

mounting board, such as a mother board. It should be noted that in FIG. 2, for description purpose, the sealing resin 103 disposed on the chip supporter 105 and the terminal portions 106 is not illustrated.

Between the chip supporter 105 and the terminal portions 106 there are formed penetration portions 109 to separate the chip supporter 105 from the terminal portions 106.

The semiconductor chip 102 includes a chip main body 111 and plural electrode pads 112. The chip main body 111 is attached to the chip supporter 105 by an adhesive agent 114. The electrode pads 112 are electrically connected to the terminal portions 106 through the wires 107. In other words, the semiconductor chip 102 is bonded to the terminal portions 106 by wire-bonding.

The sealing resin 103 seals the wires 107 and the semiconductor chip 102, and fills up the penetration portions 109.

FIG. 3 is a cross-sectional view of another semiconductor device of the related art.

In FIG. 3, the same reference numbers are assigned to the same elements as those shown in FIG. 1.

The semiconductor device shown in FIG. 3 also has a lead frame, but does not have a chip supporter 105.

Referring to FIG. 3, a semiconductor device 120 is different from the semiconductor device 100 in that the chip supporter 105 is removed and the side of the chip main body 111 opposite to the electrode pads 112 is exposed from the sealing resin 103.

For example, Japanese Laid Open Patent Application No. 2004-319577 discloses such kind of structure.

However, in the semiconductor device 100 of the

related art, since the lead frame 101, the semiconductor chip 102, and the sealing resin 103 have different thermal expansion coefficients in the thickness direction, warpage occurs in the semiconductor device 100.

In addition, in the semiconductor device 120 of the related art, since the semiconductor chip 102 and the sealing resin 103 have different thermal expansion coefficients in the thickness direction, warpage occurs in the semiconductor device 120.

SUMMARY OF THE INVENTION

The present invention solves one or more problems of the related art.

An embodiment of the present invention is to provide a semiconductor device able to prevent warpage.

According to a first aspect of the present invention, there is provided a semiconductor device, comprising:

a semiconductor chip;

a lead frame including

a chip supporter with the semiconductor chip disposed thereon, and

a terminal portion that is electrically connected to the semiconductor chip; and

a sealing resin that seals the semiconductor chip,

wherein

a first thermal expansion control member having a thermal expansion coefficient approximately equal to a thermal expansion coefficient of the lead frame is arranged on the semiconductor chip, and

an upper surface of the first thermal expansion control member is nearly in the same plane as an upper

surface of the sealing resin.

According to the present invention, since the first thermal expansion control member having nearly the same thermal expansion coefficient with the lead frame is arranged on the semiconductor chip, and the upper surface of the first thermal expansion control member and the upper surface of the sealing resin are nearly in the same plane, the chip supporter and the first thermal expansion control member, which have nearly the same thermal expansion coefficient, are arranged above and below the semiconductor chip, and this prevents warpage in the semiconductor device.

According to a second aspect of the present invention, there is provided a semiconductor device, comprising:

a semiconductor chip including

a semiconductor substrate, and

a semiconductor element formed on the semiconductor substrate;

a sealing resin that seals the semiconductor chip; and

an external connection terminal that is electrically connected to the semiconductor element, and is exposed from the sealing resin,

wherein

a first thermal expansion control member having a thermal expansion coefficient approximately equal to a thermal expansion coefficient of the semiconductor substrate is arranged on the semiconductor chip, and

an upper surface of the first thermal expansion control member is nearly in the same plane as an upper surface of the sealing resin.

According to the present invention, since the

first thermal expansion control member having nearly the same thermal expansion coefficient with the semiconductor substrate is arranged on the semiconductor chip, and the upper surface of the first thermal expansion control member and the upper surface of the sealing resin are nearly in the same plane, the semiconductor substrate and the first thermal expansion control member, which have nearly the same thermal expansion coefficient, are arranged above and below the semiconductor chip, and this prevents warpage in the semiconductor device.

According to a third aspect of the present invention, there is provided a semiconductor device, comprising:

a substrate including

a base material,

a connection pad that is disposed on a first primary surface of the base material, and

an external connection terminal that is disposed on a second primary surface of the base material opposite to the first primary surface, and is electrically connected to the connection pad,

a semiconductor chip disposed on the first primary surface of the base material and is electrically connected to the connection pad; and

a sealing resin that seals the semiconductor chip;

wherein

a first thermal expansion control member having a thermal expansion coefficient approximately equal to a thermal expansion coefficient of the base material is arranged on the semiconductor chip, and

an upper surface of the first thermal expansion control member is nearly in the same plane as an upper

surface of the sealing resin.

According to the present invention, since the first thermal expansion control member having nearly the same thermal expansion coefficient with the base material is arranged on the semiconductor chip, and the upper surface of the first thermal expansion control member and the upper surface of the sealing resin are nearly in the same plane, the base material and the first thermal expansion control member, which have nearly the same thermal expansion coefficient, are arranged above and below the semiconductor chip, and this prevents warpage in the semiconductor device.

These and other objects, features, and advantages of the present invention will become more apparent from the following detailed description of the preferred embodiments given with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of a semiconductor device of the related art;

FIG. 2 is a top view of the semiconductor device shown in FIG. 1;

FIG. 3 is a cross-sectional view of another semiconductor device of the related art;

FIG. 4 is a cross-sectional view of a semiconductor device according to a first embodiment of the present invention;

FIG. 5 is a top view of the semiconductor device shown in FIG. 4;

FIG. 6 is a top view of a lead frame group for fabricating the semiconductor device of the first embodiment;

FIG. 7 is a cross-sectional view of a modification of the semiconductor device according to the first embodiment of the present invention;

FIG. 8 is a cross-sectional view of a semiconductor device according to a second embodiment of the present invention;

FIG. 9 is a top view of a lead frame group used for fabricating the semiconductor device of the second embodiment;

FIG. 10 is a cross-sectional view illustrating a process for fabricating the semiconductor device of the second embodiment;

FIG. 11 is a cross-sectional view, continuing from FIG. 10, illustrating the process for fabricating the semiconductor device of the second embodiment;

FIG. 12 is a cross-sectional view, continuing from FIG. 11, illustrating the process for fabricating the semiconductor device of the second embodiment;

FIG. 13 is a cross-sectional view, continuing from FIG. 12, illustrating the process for fabricating the semiconductor device of the second embodiment;

FIG. 14 is a cross-sectional view, continuing from FIG. 13, illustrating the process for fabricating the semiconductor device of the second embodiment;

FIG. 15 is a cross-sectional view, continuing from FIG. 14, illustrating the process for fabricating the semiconductor device of the second embodiment;

FIG. 16 is a cross-sectional view of a first modification of the semiconductor device according to the second embodiment of the present invention;

FIG. 17 is a cross-sectional view of a second modification of the semiconductor device according to the second embodiment of the present invention;

FIG. 18 is a cross-sectional view of a third modification of the semiconductor device according to the second embodiment of the present invention;

FIG. 19 is a cross-sectional view of a fourth modification of the semiconductor device according to the second embodiment of the present invention;

FIG. 20 is a cross-sectional view of a semiconductor device according to a third embodiment of the present invention;

FIG. 21 is a cross-sectional view of a modification of the semiconductor device according to the third embodiment of the present invention; and

FIG. 22 is a cross-sectional view of a semiconductor device according to a fourth embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Below, preferred embodiments of the present invention are explained with reference to the accompanying drawings.

First Embodiment

FIG. 4 is a cross-sectional view of a semiconductor device according to a first embodiment of the present invention.

In FIG. 4, a letter "A" indicates a region where the semiconductor chip 12 is disposed. Below, this region is referred to as a "chip disposing region" A.

Referring to FIG. 4, a semiconductor device 10 includes a lead frame 11, a semiconductor chip 12, a first thermal expansion control member 13, and sealing resin 14.

FIG. 5 is a top view of the semiconductor device shown in FIG. 4.

Referring to FIG. 4 and FIG. 5, the lead frame 11 includes a chip supporter 15, and plural terminal portions 16. The chip supporter 15 has the chip disposing region A in which the semiconductor chip 12 is disposed. The terminal portions 16 are separated from the edge of the chip supporter 15, and are arranged to face the edge of the chip supporter 15. In addition, the terminal portions 16 are arranged to be separated from each other. Between the chip supporter 15 and the terminal portions 16 there are formed penetration portions 21 to separate the chip supporter 15 from the terminal portions 16. The penetration portions 21 are filled with the sealing resin 14.

Wires 18 for connection with electrode pads 23 are connected to the upper surfaces 16A of the terminal portions 16. With this structure, the semiconductor chip 12 is bonded with the terminal portions 16 by wire-bonding. The terminal portions 16 are external connection terminals for connecting the semiconductor device 10 to other semiconductor devices, or a mounting board such as a mother board. The lower surfaces 16B of the terminal portions 16 are exposed from the sealing resin 14.

The lead frame 11 may be formed from metals, for example, copper.

FIG. 6 is a top view of a lead frame group for fabricating the semiconductor device of the present embodiment.

Referring to FIG. 6, a lead frame group 25 includes plural lead frames 11 and a frame body 26 which supports the lead frames 11. The lead frames 11 are formed by cutting the lead frame group 25 into individual pieces.

The semiconductor chip 12 includes a semiconductor substrate 22, a not-illustrated

semiconductor element and a multilayer interconnection structure, and plural electrode pads 23.

The semiconductor substrate 22 is a substrate on which the semiconductor element and the multilayer interconnection structure (not illustrated) are fabricated. The back surface 22B of the semiconductor substrate 22 is attached to the chip supporter 15, which corresponds to the chip disposing region A, by an adhesive agent 29. The adhesive agent 29 may be a die Attach film. The semiconductor substrate 22 may be formed of silicon or Ga-As.

The semiconductor element (not illustrated) may be a transistor or other elements, and is disposed on the surface 22A of the semiconductor substrate 22. The multilayer interconnection structure (not illustrated) is arranged between the surface 22A of the semiconductor substrate 22 and the electrode pads 23. The multilayer interconnection structure electrically connects the semiconductor element and the electrode pads 23.

The electrode pads 23 are disposed on the edge of the upper surface of the semiconductor chip 12 like a frame. The electrode pads 23 are electrically connected to the semiconductor element through the multilayer interconnection structure. The electrode pads 23 are electrically connected to the terminal portions 16 through wires 18. Therefore, the semiconductor chip 12 is bonded with the terminal portions 16 by wire-bonding.

The first thermal expansion control member 13 is attached to the semiconductor chip 12 by an adhesive agent 31 at a position on the inner side of the electrode pads 23. The upper surface 13A of the first thermal expansion control member 13 is approximately in the same plane as the upper surface 14A of the sealing resin 14.

The first thermal expansion control member 13 has a thermal expansion coefficient approximately the same as the thermal expansion coefficient of the lead frame 11. The first thermal expansion control member 13 may be formed of the same material as the lead frame 11. For example, when the lead frame 11 is formed of copper, the first thermal expansion control member 13 may also be formed of copper. It should be noted that the first thermal expansion control member 13 may also be formed of the same material as the semiconductor substrate 22. The adhesive agent 31 may be formed from a die attach film.

The first thermal expansion control member 13 having nearly the same thermal expansion coefficient as the lead frame 11 is arranged on the semiconductor chip 12, which is disposed on the chip supporter 15. The upper surface 13A of the first thermal expansion control member 13 and the upper surface 14A of the sealing resin 14 are nearly in the same plane. The chip supporter 15 and the first thermal expansion control member 13, which have nearly the same thermal expansion coefficient, are arranged above and below the semiconductor chip 12. This structure prevents warpage in the semiconductor device 10.

The sealing resin 14 is applied to seal the semiconductor chip 12 and the wires 18, and to fill up the penetration portions 21. The upper surface 14A of the sealing resin 14 and the upper surface 13A of the first thermal expansion control member 13 are nearly in the same plane. For example, the sealing resin 14 is formed of an epoxy resin and by transfer molding.

Similarly, the first thermal expansion control member 13 having nearly the same thermal expansion coefficient as the lead frame 11 is arranged on the semiconductor chip 12, which is disposed on the chip

supporter 15. The upper surface 13A of the first thermal expansion control member 13 and the upper surface 14A of the sealing resin 14 are nearly in the same plane. The chip supporter 15 and the first thermal expansion control member 13, which have nearly the same thermal expansion coefficient, are arranged above and below the semiconductor chip 12. This structure prevents warpage in the semiconductor device 10.

The semiconductor device 10 of the present embodiment may be fabricated in the following way. The semiconductor chip 12 is disposed on the chip supporter 15 of the lead frame group 25 as shown in FIG. 6. Next, the first thermal expansion control member 13 is disposed on the semiconductor chip 12. Then the electrode pads 23 are connected to the terminal portions 16 with the wires 18. Then the semiconductor chip 12 and the wires 18 are sealed with the sealing resin 14, and then the lead frame group 25 is cut at a position where the semiconductor device 10 of the present embodiment is to be fabricated. In this way, the semiconductor device 10 of the present embodiment is obtained.

FIG. 7 is a cross-sectional view of a modification of the semiconductor device according to the first embodiment of the present invention.

In FIG. 7, the same reference numbers are assigned to the same elements as those explained previously, and overlapping explanations are omitted.

Referring to FIG. 7, a semiconductor device 35 has basically the same structure as the semiconductor device 10 as shown in FIG. 4, except that a second thermal expansion control member 36 is additionally provided.

The second thermal expansion control member 36 is attached to the first thermal expansion control member

13 and the sealing resin 14 by an adhesive agent 38. The adhesive agent 38 may be formed from a die attach film. The second thermal expansion control member 36 is like a plate, and has nearly the same thermal expansion coefficient as the lead frame 11. The area of the upper surface 36A of the second thermal expansion control member 36 is greater than the area of the upper surface 13A of the first thermal expansion control member 13. Preferably, the area of the upper surface 36A of the second thermal expansion control member 36 is nearly the same as the area of the upper surface of the lead frame 11, that is, the upper surface 15A of the chip supporter 15 and the upper surface 16A of the terminal portion 16.

The second thermal expansion control member 36 having nearly the same thermal expansion coefficient as the lead frame 11 is arranged on the first thermal expansion control member 13 and the sealing resin 14. The area of the upper surface 36A of the second thermal expansion control member 36 is nearly the same as the area of the upper surface of the lead frame 11, that is, the upper surface 15A of the chip supporter 15 and the upper surface 16A of the terminal portion 16. The second thermal expansion control member 36 and the lead frame 11, which have nearly the same thermal expansion coefficient, are arranged above and below the semiconductor chip 12 and the sealing resin 14. This structure is able to further prevent warpage in the semiconductor device 35 compared to the semiconductor device 10, which has only the first thermal expansion control member 13.

The semiconductor device 35 may be fabricated in the following way. After a structure corresponding to the semiconductor device 10 is fabricated, the second thermal expansion control member 36 is pasted on the first

thermal expansion control member 13, and the sealing resin 14 is applied to seal the second thermal expansion control member 36.

Second Embodiment

FIG. 8 is a cross-sectional view of a semiconductor device according to a second embodiment of the present invention.

In FIG. 8, the same reference numbers are assigned to the same elements as those of the semiconductor device 10, and overlapping explanations are omitted.

Referring to FIG. 8, a semiconductor device 40 is basically the same as the semiconductor device 10 in the first embodiment, except that the chip supporter 15 in the semiconductor device 10 is not provided in the semiconductor device 40, and a first thermal expansion control member 41 is provided in the semiconductor device 40 instead of the first thermal expansion control member 13 in the semiconductor device 10. The back surface 22B of the semiconductor substrate 22 is nearly in the same plane as the lower surface 16B of the terminal portions 16, and the back surface 22B of the semiconductor substrate 22 is exposed from the sealing resin 14.

The first thermal expansion control member 41 is attached to the semiconductor chip 12 by the adhesive agent 31 at a position on the inner side of the electrode pads 23, and has nearly the same thermal expansion coefficient as the semiconductor substrate 22. The upper surface 41A of the first thermal expansion control member 41 is approximately in the same plane as the upper surface 14A of the sealing resin 14. The first thermal expansion control member 41 may be formed of the same material as

the semiconductor substrate 22. For example, when the semiconductor substrate 22 is formed of silicon, the first thermal expansion control member 41 may also be formed of silicon.

According to the present embodiment, the first thermal expansion control member 41, which has nearly the same thermal expansion coefficient as the semiconductor substrate 22, is disposed on the semiconductor chip 12. The upper surface 41A of the first thermal expansion control member 41 is approximately in the same plane as the upper surface 14A of the sealing resin 14. The semiconductor substrate 22 and the first thermal expansion control member 41, which have nearly the same thermal expansion coefficient, are arranged above and below the semiconductor chip 12. This structure prevents warpage in the semiconductor device 40.

FIG. 9 is a top view of a lead frame group used for fabricating the semiconductor device of the present embodiment.

In FIG. 9, a letter "B" indicates a region where the semiconductor device 40 is disposed (below, this region is referred to as a "semiconductor device formation region" B).

In FIG. 9, a lead frame group 45 is basically the same as the lead frame group 25 in FIG. 6 except that the chip supporter 15 in the lead frame group 25 shown in FIG. 6 is absent.

FIG. 10 through FIG. 15 are cross-sectional views illustrating a process for fabricating the semiconductor device of the present embodiment. In FIG. 10 through FIG. 15, the same reference numbers are assigned to the same elements as those explained previously.

In FIG. 10, a letter "C" indicates positions

where the lead frame group 45 is cut by dicing (below, such a position is referred to as a "dicing position" C).

In FIG. 11, a letter "D" indicates a region where the semiconductor chip 12 is disposed. Below, this region is referred to as a "chip disposing region" D.

Below, with reference to FIG. 10 through FIG. 15, a process of fabricating the semiconductor device 40 is described while taking the fabrication of plural semiconductor devices 40 in the lead frame group 45 as an example.

First, as shown in FIG. 10, on a supporting tape 47, which is adhesive, the lead frame group 45 is disposed. For example, the supporting tape 47 may be formed from polyimide film, and the supporting tape 47 may be 30 μm in thickness.

Next, as shown in FIG. 11, the back surface 22B of the semiconductor substrate 22 is pasted on an area of the supporting tape 47 corresponding to the chip disposing region D. Next, the first thermal expansion control member 41 is attached to the semiconductor chip 12 by the adhesive agent 31.

Next, as shown in FIG. 12, the wires 18 for connecting the electrode pads 23 and the terminal portions 23 are formed. Thereby, the semiconductor chip 12 is bonded with the terminal portions 16 by wire-bonding.

Next, as shown in FIG. 13, the sealing resin 14 is applied to seal the semiconductor chip 12 and the wires 18. In this step, the sealing resin 14 is formed so that the upper surface 41A of the first thermal expansion control member 41 is approximately in the same plane as the upper surface 14A of the sealing resin 14. In this way, a structure corresponding to the semiconductor device 40 is fabricated in the semiconductor device formation region

B. For example, the sealing resin 14 is formed of an epoxy resin and by transfer molding.

Next, as shown in FIG. 14, the supporting tape 47 is removed.

Next, as shown in FIG. 15, the sealing resin 14 and the lead frame group 45 are cut by dicing at positions corresponding to the dicing positions C. Thus, plural semiconductor devices 40 are fabricated.

FIG. 16 is a cross-sectional view of a first modification of the semiconductor device according to the second embodiment of the present invention.

In FIG. 16, the same reference numbers are assigned to the same elements as those of the semiconductor device 40, and overlapping explanations are omitted.

Referring to FIG. 16, a semiconductor device 48 has basically the same structure as the semiconductor device 40, except that bumps 49 are formed in the semiconductor device 48 instead of the wires 18 in the semiconductor device 40 of the present embodiment to connect the semiconductor chip 12 with the terminal portion 16 by flip-chip bonding.

The semiconductor device 48 of the above structure has the same effect as the semiconductor device 40.

FIG. 17 is a cross-sectional view of a second modification of the semiconductor device according to the second embodiment of the present invention.

In FIG. 17, the same reference numbers are assigned to the same elements as those of the semiconductor device 40, and overlapping explanations are omitted.

Referring to FIG. 17, a semiconductor device 50

has basically the same structure as the semiconductor device 40, except that a second thermal expansion control member 51 is provided additionally.

The second thermal expansion control member 51 is arranged on the first thermal expansion control member 41 while facing the semiconductor substrate 22. The second thermal expansion control member 51 is sealed by the sealing resin 14 with the upper surface 51B of the second thermal expansion control member 51 exposed. The upper surface 51B of the second thermal expansion control member 51 is approximately in the same plane as the upper surface 14A of the sealing resin 14.

The second thermal expansion control member 51 is a plate, and has nearly the same thermal expansion coefficient as the semiconductor substrate 22. The area of the upper surface 51B of the second thermal expansion control member 51 is nearly the same as the area of the surface 22B of the semiconductor substrate 22. That is, the outer appearance of the second thermal expansion control member 51 is nearly the same as the outer appearance of the semiconductor substrate 22. The second thermal expansion control member 51 is attached to the first thermal expansion control member 41 by an adhesive agent 52. The adhesive agent 52 is applied to cover the whole lower surface 51A of the second thermal expansion control member 51. For example, the adhesive agent 52 is formed from a die attach film.

As described above, since the second thermal expansion control member 51, which has nearly the same thermal expansion coefficient as the semiconductor substrate 22, and has nearly the same outer appearance as the outer appearance of the semiconductor substrate 22, is disposed on the first thermal expansion control member 41,

and the second thermal expansion control member 51 is arranged to face the semiconductor substrate 22, it is possible to further prevent warpage in the semiconductor device 50 compared to the semiconductor device 40, which has only the first thermal expansion control member 41.

The semiconductor device 50 may be fabricated in the following way. After a structure corresponding to the semiconductor device 40 as shown in FIG. 12 is fabricated, the second thermal expansion control member 51 is pasted on the first thermal expansion control member 41, and the sealing resin 14 is applied to seal the second thermal expansion control member 51.

FIG. 18 is a cross-sectional view of a third modification of the semiconductor device according to the second embodiment of the present invention.

In FIG. 18, the same reference numbers having suffixes "-1" or "-2" are assigned to the same elements as those of the semiconductor device 40, and overlapping explanations are omitted.

Referring to FIG. 18, a semiconductor device 55 includes sealing resin 14, a terminal portion 16, semiconductor chips 56, 57, and a first thermal expansion control member 61.

The semiconductor chip 56 includes a semiconductor substrate 22-1 and plural electrode pads 23-1 arranged in a row on one side of the semiconductor chip 56, and the semiconductor substrate 22-1 and the electrode pads 23-1 are sealed by the sealing resin 14.

The semiconductor substrate 22-1 is arranged so that the back surface 22-1B of the semiconductor substrate 22-1 is approximately in the same plane as the lower surface 14B of the sealing resin 14. The electrode pads 23-1 are electrically connected to the terminal portions

16 through the wires 18-1.

The semiconductor chip 57 includes a semiconductor substrate 22-2 and plural electrode pads 23-2 arranged in a row on one side of the semiconductor chip 57, and the semiconductor substrate 22-2 and the electrode pads 23-2 are sealed by the sealing resin 14.

The semiconductor substrate 22-2 is formed of the same material as the semiconductor substrate 22-1. The back surface 22-2B of the semiconductor substrate 22-2 is attached to the semiconductor chip 56 by an adhesive agent 59, and thereby, the semiconductor chip 57 is stacked on the semiconductor chip 56. The adhesive agent 59 may be a die Attach film. The electrode pads 23-2 are electrically connected to the terminal portions 16 through the wires 18-2.

The first thermal expansion control member 61 is attached to the semiconductor chip 57, which is the semiconductor chip at the uppermost position, by an adhesive agent 62. The upper surface 61A of the first thermal expansion control member 61 is approximately in the same plane as the upper surface 14A of the sealing resin 14. The first thermal expansion control member 61 has a thermal expansion coefficient approximately the same as the thermal expansion coefficient of the semiconductor substrate 22-1 and the semiconductor substrate 22-2. The first thermal expansion control member 61 may be formed of the same material as the semiconductor substrate 22-1 and the semiconductor substrate 22-2. For example, the semiconductor substrate 22-1 and the semiconductor substrate 22-2 may be formed of silicon or Ga-As.

The first thermal expansion control member 61 is arranged on the semiconductor chip 57, which is at the uppermost position among the semiconductor chips 56, 57.

The upper surface 61A of the first thermal expansion control member 61 and the upper surface 14A of the sealing resin 14 are nearly in the same plane. The semiconductor substrate 22-1 and the first thermal expansion control member 61, which have nearly the same thermal expansion coefficient, are arranged on the upper side and lower side of the semiconductor device 55. This structure prevents warpage in the semiconductor device 55.

The semiconductor device 55 may be fabricated in the same way as the semiconductor device 40 of the present embodiment.

FIG. 19 is a cross-sectional view of a fourth modification of the semiconductor device according to the second embodiment of the present invention.

In FIG. 19, the same reference numbers are assigned to the same elements as those of the semiconductor device 55, and overlapping explanations are omitted.

Referring to FIG. 19, a semiconductor device 65 is basically the same as the semiconductor device 55, except that a second thermal expansion control member 66 is additionally provided.

The second thermal expansion control member 66 is attached to the first thermal expansion control member 61 to face the stacked structure of the semiconductor chip 56 and the semiconductor chip 57. The second thermal expansion control member 66 is sealed by the sealing resin 14 with the upper surface 66A of the second thermal expansion control member 66 exposed. The upper surface 66A of the second thermal expansion control member 66 is approximately in the same plane as the upper surface 14A of the sealing resin 14.

The second thermal expansion control member 66

is attached to the first thermal expansion control member 61 by an adhesive agent 67. The adhesive agent 67 is applied to cover the whole lower surface 66B of the second thermal expansion control member 66. For example, the adhesive agent 67 is formed from a die attach film.

The second thermal expansion control member 66 is a plate, and has nearly the same thermal expansion coefficient as the semiconductor substrate 22-1 and the semiconductor substrate 22-2.

As described above, since the second thermal expansion control member 66, which has nearly the same thermal expansion coefficient as the semiconductor substrate 22-1 and the semiconductor substrate 22-2, is disposed on the first thermal expansion control member 61 to face the stacked semiconductor chips 56, 57, it is possible to further prevent warpage in the semiconductor device 65 compared to the semiconductor device 55, which has only the first thermal expansion control member 61.

The semiconductor device 65 may be fabricated in the same way as the semiconductor device 55 of the present embodiment.

Third Embodiment

FIG. 20 is a cross-sectional view of a semiconductor device according to a third embodiment of the present invention.

In FIG. 20, the same reference numbers are assigned to the same elements as those explained previously, and overlapping explanations are omitted.

Referring to FIG. 20, a semiconductor device 70 includes a substrate 71, a semiconductor chip 12, a first thermal expansion control member 73, and sealing resin 74.

The substrate 71 includes base material 75,

penetration vias 76, interconnections 77, 81, connection pads 78, pads 82, solder resist 84, and external connection terminals 85.

The base material 75 has a plate shape, and has penetration holes 87. For example, the base material 75 may be formed from a glass epoxy board.

The penetration vias 76 are provided in the penetration holes 87. Each of the penetration vias 76 has a hollow portion 76A. The interconnection 77 electrically connects the connection pads 78 and the penetration vias 76.

The connection pads 78 are disposed on the upper surface 75A of the base material 75. The connection pads 78 are electrically connected to the interconnection 77, and are electrically connected to the electrode pads 23 of the semiconductor chip 12 through the wires 88.

The interconnection 81 is formed on the lower surface 75B of the base material 75. The interconnection 81 is electrically connected to the penetration vias 76 and the pads 82. The pads 82 are formed on the lower surface 75B of the base material 75, and are electrically connected to the interconnection 81.

The solder resist 84 is provided on the upper and lower surfaces 75A, 75B of the base material 75 to cover the interconnections 77 and 81 with the solder resist 84 exposing the connection pads 78 and the pads 82. In addition, the solder resist 84 fills up the hollow portion 76A of the penetration via 76.

The external connection terminals 85 are provided on the pads 82, and serve as terminals for connecting the semiconductor device 70 to a mounting board such as a mother board.

The semiconductor chip 12 is attached to the

solder resist 84 disposed on the upper surface 75A of the base material 74 by the adhesive agent 29.

The first thermal expansion control member 73 is attached to the semiconductor chip 12 by an adhesive agent 31. The upper surface 73A of the first thermal expansion control member 73 is approximately in the same plane as the upper surface 74A of the sealing resin 74. The first thermal expansion control member 73 has a thermal expansion coefficient approximately the same as the thermal expansion coefficient of the base material 75. For example, the first thermal expansion control member 73 may be formed of the same material as the base material 75.

The sealing resin 74 is applied to seal the semiconductor chip 12 and the wires 88 with the upper surface 73A of the first thermal expansion control member 73 exposed. The upper surface 74A of the sealing resin 74 and the upper surface 73A of the first thermal expansion control member 73 are nearly in the same plane. For example, the sealing resin 74 is formed of an epoxy resin and by transfer molding.

In the semiconductor device 70, the first thermal expansion control member 73 having nearly the same thermal expansion coefficient with the base material 75 is arranged on the semiconductor chip 12 disposed on the substrate 71. The upper surface 73A of the first thermal expansion control member 73 and the upper surface 74A of the sealing resin 74 are nearly in the same plane. The base material 75 and the first thermal expansion control member 73, which have nearly the same thermal expansion coefficient, are arranged above and below the semiconductor chip 12. This structure prevents warpage in the semiconductor device 70.

FIG. 21 is a cross-sectional view of a

modification of the semiconductor device according to the third embodiment of the present invention.

In FIG. 21, the same reference numbers are assigned to the same elements as those of the semiconductor device 70, and overlapping explanations are omitted.

Referring to FIG. 21, a semiconductor device 90 has basically the same structure as the semiconductor device 70, except that a second thermal expansion control member 91 is additionally provided.

The second thermal expansion control member 91 is formed to cover the upper surface 73A of the first thermal expansion control member 73 and the upper surface 74A of the sealing resin 74.

The second thermal expansion control member 91 is attached to the first thermal expansion control member 73 by an adhesive agent 92. For example, the adhesive agent 92 is formed from a die attach film.

The second thermal expansion control member 91 has a plate shape, and has nearly the same thermal expansion coefficient as the base material 75. For example, the second thermal expansion control member 91 is formed of the same material as that of the base material 75.

In the semiconductor device 90, the second thermal expansion control member 91, which has nearly the same thermal expansion coefficient as the base material 75, is disposed to cover the upper surface 73A of the first thermal expansion control member 73 and the upper surface 74A of the sealing resin 74. The base material 75 and the first thermal expansion control member 91, which have nearly the same thermal expansion coefficient, are arranged above and below the semiconductor chip 12 and the sealing resin 74. With this structure it is possible to

further prevent warpage in the semiconductor device 90 compared to the semiconductor device 70, which has only the first thermal expansion control member 73.

In the above, it is described as an example that the base material 75 is formed from a glass epoxy board; it is apparent that the base material 75 in the semiconductor device 70 or the semiconductor device 90 may be formed from any tape-like materials instead of the glass epoxy board.

The first thermal expansion control member 73 may be formed of the same material of the semiconductor substrate 22.

Fourth Embodiment

FIG. 22 is a cross-sectional view of a semiconductor device according to a fourth embodiment of the present invention.

In FIG. 22, the same reference numbers are assigned to the same elements as those of the semiconductor device 40 and the semiconductor device 70 as described previously, and overlapping explanations are omitted.

Referring to FIG. 22, a semiconductor device 95 is basically the same as the semiconductor device 40 of the second embodiment, except that the terminal portions 16 in the semiconductor device 40 of the second embodiment are not provided in the semiconductor device 95, and a substrate 121 is provided in the semiconductor device 95 instead of the terminal portions 16 in the semiconductor device 40.

The substrate 121 is basically the same as the substrate 71 of the semiconductor device 70 in the third embodiment, except that a chip holding portion 121A is

formed near the center of the substrate 121 in the semiconductor device 95 for accommodating the semiconductor chip 12. The chip holding portion 121A is formed to penetrate the base material 75.

The semiconductor device 120 of the above structure has the same effect as the semiconductor device 40 in the second embodiment.

While the present invention has been described with reference to specific embodiments chosen for purpose of illustration, it should be apparent that the invention is not limited to these embodiments, but numerous modifications could be made thereto by those skilled in the art without departing from the basic concept and scope of the invention.

This patent application is based on Japanese Priority Patent Applications No. 2005-333959 filed on November 18, 2005 and No. 2006-230862 filed on August 28, 2006, the entire contents of which are hereby incorporated by reference.

WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a semiconductor chip;

a lead frame including

a chip supporter with the semiconductor chip disposed thereon, and

a terminal portion that is electrically connected to the semiconductor chip; and

a sealing resin that seals the semiconductor chip;

wherein

a first thermal expansion control member having a thermal expansion coefficient approximately equal to a thermal expansion coefficient of the lead frame is arranged on the semiconductor chip, and

an upper surface of the first thermal expansion control member is nearly in the same plane as an upper surface of the sealing resin.

2. The semiconductor device as claimed in claim 1, wherein

the semiconductor chip has a semiconductor substrate, and

a second thermal expansion control member having a thermal expansion coefficient approximately equal to a thermal expansion coefficient of the semiconductor

substrate is arranged on the first thermal expansion control member and the sealing resin.

3. The semiconductor device as claimed in claim 2, wherein

a connection pad is disposed on a primary surface of the semiconductor substrate, and

another semiconductor chip is disposed between said semiconductor chip and the first thermal expansion control member, and is electrically connected to the connection pad.

4. A semiconductor device, comprising:

a semiconductor chip including

a semiconductor substrate, and

a semiconductor element formed on the semiconductor substrate;

a sealing resin that seals the semiconductor chip; and

an external connection terminal that is electrically connected to the semiconductor element, and is exposed from the sealing resin;

wherein

a first thermal expansion control member having a thermal expansion coefficient approximately equal to a thermal expansion coefficient of the semiconductor substrate is arranged on the semiconductor chip, and

an upper surface of the first thermal expansion control member is nearly in the same plane as an upper surface of the sealing resin.

5. The semiconductor device as claimed in claim 4, wherein

a second thermal expansion control member having a thermal expansion coefficient approximately equal to a thermal expansion coefficient of the semiconductor substrate is arranged on the first thermal expansion control member and the sealing resin, and

the second thermal expansion control member has an appearance nearly the same as an appearance of the semiconductor substrate, and is arranged to face the semiconductor substrate.

6. The semiconductor device as claimed in claim 4, wherein

a connection pad is disposed on a primary surface of the semiconductor substrate, and

another semiconductor chip is disposed between said semiconductor chip and the first thermal expansion control member, and is electrically connected to the connection pad.

7. A semiconductor device, comprising:

a substrate including

a base material,

a connection pad that is disposed on a first primary surface of the base material, and

an external connection terminal that is disposed on a second primary surface of the base material opposite to the first primary surface, and is electrically connected to the connection pad;

a semiconductor chip that is disposed on the first primary surface of the base material and is electrically connected to the connection pad; and

a sealing resin that seals the semiconductor chip;

wherein

a first thermal expansion control member having a thermal expansion coefficient approximately equal to a thermal expansion coefficient of the base material is arranged on the semiconductor chip, and

an upper surface of the first thermal expansion control member is nearly in the same plane as an upper surface of the sealing resin.

8. The semiconductor device as claimed in claim 7, wherein

a second thermal expansion control member having a thermal expansion coefficient approximately equal to a thermal expansion coefficient of the base material is arranged on the first thermal expansion control member and

the sealing resin.

9. The semiconductor device as claimed in claim 7, wherein a semiconductor chip is disposed between said semiconductor chip and the first thermal expansion control member, and is electrically connected to the connection pad.