

In monitors for data processing equipment and also for television receivers for multi norm operation, there is often the need to selectively display signals having different line frequencies. This is the case for example in a monitor for a computer if signals from various signal sources which have different line frequencies are to be selectively displayed on the monitor. The line deflection circuit of the monitor or the television receiver then has to be switched to the various line frequencies or matched to them.

In the line deflection circuit during the forward sweep period, a constant operating voltage is applied to an inductance so that the current in the inductance rises approximately linearly. The value of the current at the end of the forward sweep period, which determines the width of the picture, is thus dependent, amongst other things, on the value of the inductance, the duration of the forward sweep period and the magnitude of the applied operating voltage. At higher line frequencies and thus shorter forward sweep period, the deflection current must reach the predefined value in a shorter time if the picture width is to be maintained. Since the value of the inductance remains unaltered, the applied operating voltage must be increased correspondingly. This requirement also exists because the high tension obtained from the line fly back pulse likewise has to remain constant for the individual norms.

It is known to apply different high operating voltages to the line deflection circuit for the various line frequencies. From a technical viewpoint, this solution has disadvantages particularly as the operating voltage, which in general is stabilised, has to be switched over.

It is also known to connect the operating voltage to different taps of the primary winding of the line output stage for the various line frequencies. This solution however requires additional taps on the primary winding and is in practice only useable for two different frequencies which only differ from one another by about 20%.

It is also known to supply the operating voltage to the primary winding of the line transformer via an electronically controllable switch in the form of a switching transistor and to turn on the switch, in dependence on the line frequency, at a time point during the forward sweep period which occurs at a defined interval before the start of the fly back. For a high line frequency and thus a necessarily high operating voltage, the switch must be turned on earlier and for a low line frequency, later. For a very low line frequency, the switch is

closed for only a very small portion of the forward line sweep period and for maximum line frequency is practically always conductive. In this way, the average value of the operating voltage applied to the line output stage is altered and matched to the actual line frequency.

The just described solution requires a switching pulse for the electronic switch whose switching flank lies at a defined and regulable interval before the leading edge of the fly back pulse. This interval extends over almost the whole forward line sweep period. For a cyclical voltage, such a switching pulse can be derived at a defined interval before the leading edge of a pulse from the preceding pulse by pulse shaping or time delay stages. In the present case, this solution is of only limited use because, due to the different frequencies, the time interval between two fly back pulses is not constant but dependent on the actual line frequency.

The object of the invention is to develop a simple circuit with which a switching pulse having a defined and regulable phase angle relative to the following line fly back pulse can be generated.

This object is achieved by the invention defined in claim 1. Advantageous developments of the invention are specified in the appendant claims.

The invention is based on the following manner of operation: The line frequency pulse voltage, whose edge directed in the direction of a blocked transistor corresponds to the start of the fly back, is applied to the base of the transistor via a capacitor serving for the coupling of alternating current and an RC element serving for the integration. The control current is supplied to the base on the other hand. As long as the control current is zero, no base current can flow into the transistor due to the effect of the said capacitor. The transistor therefore remains blocked. The integrated, saw tooth shaped signal on the capacitor of the filter element is thereby clamped to the base/emitter path of the transistor without this causing the transistor to become conducting. The current flowing through the resistor of the filter element thereby causes the discharge of the capacitor of the RC element in the sense that a saw tooth shaped voltage appears on the capacitor. Only the sum of the current flowing through the resistor and the control current is capable of generating a base current in the transistor and thus of rendering the transistor conductive. The current flow of the transistor sets in when the voltage at the base is about 0.6 V more positive than the voltage on the emitter. For this, the

3

resistor in the collector circuit of the transistor is made so high ohmic that the transistor works as a pure switch. The transistor goes into saturation with a very low base current i.e. becomes fully conductive. The rectangular voltage thus occurring on the collector, with values between zero for a conductive transistor and operating voltage for blocked transistors, is thereby pulse width modulated in correspondence with the duration of the pulse. For increasing control current, the pulse duration i.e. the duration of the zero portion of the pulse for conductive transistors, becomes correspondingly greater. The circuit works in the sense of a PWM namely a pulse width modulation whereby the width of the pulse is a function of the control current. Particularly advantageous here is that the circuit works in the manner described independently of the frequency of the currently supplied control voltage i.e. the line frequency.

The position in time of the pulse edge for the onset of current in the transistor before the start of the fly back pulse is thus dependent on the value of the control current. In turn, this position in time determines the period for which the operating voltage for the line output stage is turned on and thus the maximum value of the deflection current, the width of the picture and the high tension. Thus, if the control current is obtained from the prevailing maximum value of the deflection current or the amplitude of the fly back voltage occurring on the output stage transistor, the control current can be used for the regulation of the amplitude of the deflection current and thus of the width of the picture to its preferred value, by altering the turn on time point of the transistor in the path of the operating voltage. There is thus provided a simple circuit using simple circuit means which, for the different line frequencies, automatically so adjusts the time point of the connection of the operating voltage to the line output stage that, independently of the line frequency, the maximum value of the deflection current, the picture width and the high tension generated from the line fly back pulse remain constant.

The invention will be explained hereinafter by means of an embodiment with the help of the drawing. Therein

Fig. 1 shows the basic manner of operation of the line deflection circuit with applied operating voltage,

Fig. 2 curves for explaining the manner of operation of the circuit in accordance with Fig. 1,

Fig. 3 in principle, the circuit according to the invention,

Fig. 4 curves for explaining the circuit in accordance with Fig. 3,

Fig. 5 an overview of the interaction of the individual stages,

Fig. 6 a detailed circuit diagram of the circuit in accordance with Fig. 5 and

Fig. 7 curves for explaining the manner of operation of the circuit in accordance with Fig. 6.

Fig. 1 shows a line deflection circuit having the operating voltage UB , the primary winding $L1$ and the high tension winding $L2$ of the line transformer Tr , the line output stage transistor $T1$, the fly back capacitor CR , the fly back diode $D1$, the line deflecting coil AE , the coupling capacitor Cs and the high tension rectifier HG for the production of the high tension UH . The constant operating voltage UB present on the filter capacitor CL is applied via the electronic switch $T2$ to the winding $L1$. The line oscillator G controls on the one hand the transistor $T1$ and on the other hand the switch $T2$ via the modulator 4.

Fig. 2 shows the voltage U_{cT1} having the forward sweep duration of $t_0 - t_2$ and the fly back duration of $t_2 - t_4$ which appears at the collector of the transistor $T1$. The switch $T2$ is respectively conductive during the fly back period and blocked during a portion of the forward sweep period which is dependent on the actual frequency. According to Fig. 2, the switch $T2$ is controlled to be conductive by a switching pulse at time point t_1 from the modulator 4 so that the current i_R can flow. The time interval t_c between the turn on time point t_1 and the start of the fly back pulse at time point t_2 determines the average value of the operating voltage E_2 supplied to the output stage and is dependent on the actual line frequency. The time t_c from t_1 to t_2 must therefore have a defined regulable value. For minimum line frequency, t_c is a minimum, for maximum line frequency, a maximum, namely practically $= t_0$ to t_2 . The diode $D2$ illustrated in Fig. 1 serves to draw the negative portion of the current i_R .

Fig. 3 shows the circuit for the generation of the switching pulse for the switch $T2$, i.e. the circuit of the modulator 4 in Fig. 1. The line frequency, rectangular voltage U_{c1} whose negative flank occurs at the start of the fly back period is applied via the capacitor $C5$ serving for the coupling of the alternating voltage and the integrating element having the

resistor R4 and the capacitor C4 to the base of the transistor T4. Additionally, a control current i_c from the current source S is supplied to the base of the transistor T4. It is assumed initially that i_c is $= 0$. The base/emitter path of the transistor T4 forms a diode so that the voltage U_{bT4} , which is present on the base and is obtained by integration of U_{c1} , is clamped to the transistor path and thus can only be negative or 0 (Fig. 4). Due to the effect of C5, the transistor T4 thus remains blocked. If the current source S delivers a direct control current i_c of a few mA, this current is added to the current delivered by resistor R4. If the time constant of the integrating element R4, C4 is sufficiently great, the transistor T4 functions as a pulse width modulator (PWM) in that the duration of the pulse U_{cT4} produced at its collector is dependent on the magnitude of the control current i_c .

As is illustrated in Fig. 4, the interval t_c , i.e. the position in time of the trailing edge of the generated pulse U_{cT4} before the start of the fly back period at time point t_{13} , is dependent on the control current i_c . The trailing edge of the generated pulse U_{cT4} is thus linked in phase with the negative flank of the voltage U_{c1} delivered by the oscillator G. If the control current i_c increases, then t_c also increases. If i_c is $= 0$, t_c is also $= 0$. For a very small control current i_c , the duration of the pulse during the conductive phase of the transistor T4, namely the period from t_{12} - t_{14} , is correspondingly small. Independently of the line frequency, i.e. of the frequency of U_{c1} , the pulse U_{cT4} thus occurs in dependence on i_c before the negative flank of the voltage U_{c1} and therefore can be used as a switching pulse for the electronic switch T2. The switching pulse does not occur, only then, when i_c is $= 0$. Due to a correspondingly large value of RCL of approximately 10 kOhm, it is ensured that T4 operates as a pure switch. The voltage U_{c1} may be that voltage which also controls the driver stage of the deflection circuit. The negative i.e. falling flank of this voltage corresponds to the start of the fly back period. The described relationships for two different frequencies f_1 and f_2 are illustrated in Fig. 4. It is apparent, that despite differing frequencies and thus differing durations of the forward sweep period, the time t_c between the turn on time point t_{12} of the transistor T4 and the switch off time point t_{14} are approximately the same. Thus, the time point t_{12} can be so controlled by the control current i_c derived from the deflection current or the fly back voltage of the line output stage that, independently of the line frequency, the maximum value of the deflection current, the picture width and the high tension are constant.

Fig. 5 shows the interaction of the individual stages of a circuit which is illustrated in detail in Fig. 6. Fig. 5 shows the PLL and oscillator circuit 1 to which the line frequency voltage Z derived from the television signal is applied, the driver stage 2, the line output stage 3 with the transistor T_1 , the modulator 4 with the transistor T_4 of Fig. 3 which corresponds to the modulator 4 in Fig. 1, a driver stage 5 for the switching stage 6 with the transistor T_2 , a peak detector 7 for the voltage U_{cT1} at the collector of the line output stage transistor T_1 and a comparator stage 8. The inserted symbols indicate which components in Fig. 6 form the individual stages in Fig. 5. The stages 1, 2, 3 in Fig. 5 form a usual line deflection circuit. The control of the line deflection circuit for different line frequencies is effected by the stages 4 - 8. The fly back voltage on the collector of the line output stage transistor T_1 is detected in the peak detector 7 whereby a direct voltage corresponding to the fly back amplitude is produced. This direct voltage is also proportional to the generated high tension UH . A comparison of this direct voltage with an internally defined voltage or reference voltage is effected in the comparator stage 8. The control of the magnitude of the control current i_c follows from the result of this comparison. The control current i_c is effective in the described manner on the modulator 4 with the transistor T_4 corresponding to Fig. 3.

Fig. 6 shows a detailed circuit diagram of the circuit in accordance with Fig. 5 wherein similar references are used for components corresponding to each other. The line frequency voltage U_{c1} from the generator G controls the output stage transistor T_1 via the driver stage 2. The transistor T_5 amplifies the voltage U_{c1} whereby the delay network VN serves for the compensation of the delay in the blocking of the driver stage 2 and of the transistor T_1 . The components C_5 , R_4 , C_4 , T_4 function as in Fig. 3. The transistor T_3 serves as current amplifier for the direct control of the transistor T_2 via a capacitive coupling with the capacitor C_{b2} . The diode D_5 and the capacitor C_{60} produce a direct voltage having the peak value of the voltage U_{cT1} on the collector of T_1 . This voltage is adjustable with the potentiometer P_{15} and is applied to the base of the transistor T_6 . The transistor T_6 has the function of the comparator stage 8 in accordance with Fig. 5 and produces the control current i_c that is dependent on the magnitude of U_{cT1} and which flows into the base of transistor T_4 . By means of this described control of the turn on time point of T_2 which originates with U_{cT1} , the deflection amplitude, the picture width and the high tension are maintained constant. If UH falls, the amplitude of U_{cT1} falls, and with it the positive direct

voltage obtained from capacitor C60, the collector current of T6 namely the value of the control current i_c increases, the time interval t_c increases, the value of the current through T2 increases so that U_{cT1} and U_H again increase and thus are regulated at the desired value.

Fig. 7 shows the individual current and voltage characteristics of the voltages in the circuit according to Fig. 6. U_{cT1} is the previously described fly back voltage at the collector of T1 whose amplitude is regulated at a constant value. i_{T1} is the current in the collector/emitter path of T1, i_{D1} the current through the free running or fly back diode D1. i_R is the current flowing through T2 and D2 into the winding L1 which is turned off from $t_1 - t_3$ by T2 and whose negative portion flows via D2. E2 is the operating voltage effective on L1 which is turned off from $t_1 - t_3$, and is turned on by T2 at the controlled time t_c before the start of the fly back t_5 , at time point t_3 . U_{c1} is the described line frequency pulse voltage which, as voltage U_{cT5} in Fig. 6 with the polarity in accordance with Fig. 4, is extended to the input of the filter element R4, C4. Corresponding to Fig. 4, U_{bT4} is the voltage on the base of T4, and U_{cT4} , the switching voltage appearing at the collector of T4 and serving for the control of T2.



Claims

1. Line deflection circuit for different line frequencies in which, in the path of the operating voltage (U_B) for the line output stage (T_1), there is located a switch (T_2) which is closed during each forward sweep period by a switching pulse (U_{cT4}), characterised in that, the switching pulse (U_{cT4}) is derived from the collector of a transistor (T_4) to whose base there is supplied a line frequency pulse voltage (U_{c1}) via an alternating voltage coupling (C_5) and an integrating element (R_4 , C_4) and a control current (i_c) serving for the influencing of the amplitude of the line deflection current (i_L).
2. Circuit in accordance with claim 1, characterised in that, the resistor (R_{CL}) in the collector circuit of the transistor (T_4) is dimensioned such that the transistor (T_4) operates as a switch.
3. Circuit in accordance with claim 1, characterised in that, the pulse edge of the pulse voltage (U_{c1}) is in a direction effective for the blocking of the transistor (T_4) at the start of the fly back period of the line deflection circuit.
4. Circuit in accordance with claim 1, characterised in that, the value of the control current (i_c) is obtained from a comparison of the amplitude of the line deflection current (i_L) or the fly back voltage (U_{cT1}) with a predefined value.
5. Circuit in accordance with claim 4, characterised in that, the collector of the output stage transistor (T_1) is connected via a rectifier (D_5) and a potentiometer (P_{15}) to the base of a transistor (T_6) whose collector - emitter path, which delivers the control current (i_c), is located between an operating voltage and the base of the transistor (T_4) delivering the switching pulse (U_{cT4}).