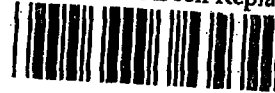


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SPECIFICATION

TITLE OF THE INVENTION

TRANSMISSION LINE DRIVE CIRCUIT, OUTPUT DRIVER CIRCUIT
AND ATM-LAN ADAPTER CARD

5 BACKGROUND OF THE INVENTION

The present invention relates to transmission line drive
circuits and output driver circuits for an ATM-LAN and to ATM-
LAN adapter cards, and more specifically to a technology
which, when applied to output driver circuits in a
10 semiconductor integrated circuit (IC) for a physical layer
interface in the ATM-LAN, enables low voltage operation of the
semiconductor IC circuit.

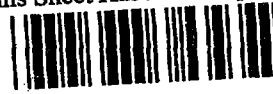
One of the LAN (Local Area Network) specifications,
generally known as the Ethernet, is standardized by the IEEE
15 (Institute of Electrical and Electronics Engineers) 802.3.
With regard to a medium attachment unit as a transceiver that
conforms to such a standard, Japanese Patent Laid-Open No.
213940/1992 discloses a driver circuit of CMOS configuration
for driving twisted pair circuits or a pair of twisted lines
20 as a transmission medium.

This driver circuit has a first circuit consisting of a
PMOS transistor and an NMOS transistor connected in series and
a second circuit consisting of a PMOS transistor and an NMOS
transistor connected in series. The NMOS transistors of these
25 circuits have their source terminals connected to a reference



voltage biased to a potential higher than the ground, whereas the PMOS transistors of the circuits have their source terminals connected to a power supply voltage. A common drain terminal of the MOS transistors in the first circuit forms a first output terminal. A common drain terminal of the MOS transistors in the second circuit forms a second output terminal. Further, the two output terminals are connected through an impedance that functions as a terminating resistor. The driver circuit, based on an input differential signal, switches between the first and second circuits in opposite phases complementarily and, via the first and second output terminals, drives the twisted pair circuits or lines.

Furthermore, Japanese Patent Laid-Open No. 213940/1992 shows that for the aforementioned driver circuit with CMOS configuration, it is necessary to solve a problem called backswing or undershoot that is caused by the end of transmission delimiting signal (ETD). That is, if the driver circuit includes an isolation transformer and if the input to the transformer is held high by the ETD, the isolation transformer will introduce into the signal an undershoot due to backswing by an electromotive force when the ETD is turned off. This backswing is an insignificant signal transition, which, when its duration is long, gives rise to a possibility that it may be monitored on the receiving side as a significant signal change representing the start of transmission, lowering the efficiency of the system operation. According to the publication, to suppress the backswing in an



allowable range, transistors need to be added that will short-circuit the first output terminal and the second output terminal (the impedance mentioned earlier) when the ETD is terminated, making it possible to fabricate a CMOS Ethernet driver circuit conforming the IEEE802.3 standard.

Today, the ATM (Asynchronous Transfer Mode) technology is beginning to be introduced into LAN. Determining the specifications of the ATM technology is being done by The ATM Forum established in the United States. In the Ethernet, because a plurality of LAN nodes share a single communication medium, as the number of LAN nodes increase, the band available for each LAN node (determining the range of speed at which information is transmitted) decreases. When many nodes attempt to transmit data virtually at the same time, the overall throughput deteriorates sharply. The LAN that has introduced the ATM technology (referred to as ATM-LAN) incorporates an ATM switching technology that allows the transmission speed range to be changed freely even during communication and aims at realizing a superhigh speed data transfer with improved throughput, which enables a wide range of communication, from low-speed communication with a small amount of information to communication at a high and wide transmission speed range and in which transmission and reception are performed in a one-to-one relationship.



SUMMARY OF THE INVENTION

For the physical layer interface of the ATM-LAN, the number of succeeding logical values, bits "0" and "1", contained in the information being transmitted is limited, and a template (pulse mask) is standardized and assigned for each group of succeeding bits to define a waveform for each bit group to enable scrambling and encoding and to improve the transmission efficiency. For example, the sending signal waveform defined by the template for an ATM Forum 25Mb/s ATM-LAN physical layer, which has already been standardized as the specification, has a waveform--- not a simple rectangular waveform---that requires a relatively high accuracy. The signal amplitude defined by the template is required to be about 2V (zero to peak), for example. When such a specification is assumed, it is required that a filter be provided in a stage after the transmission driver circuit for the ATM-LAN physical layer interface so as to make the sending signal waveform conform to the signal waveform defined by such a template. It is also necessary to establish impedance matching with the transmission line by providing an output impedance adjust resistor after the driver circuit.

Because the output signal from the aforementioned driver circuit is expected to have voltage losses or voltage drop due to the filter and impedance, the power supply voltage of the driver circuit needs to be relatively high enough to meet the signal amplitude requirements defined by the template, and thus cannot be set too low.



The driver circuit, however, requires a relatively large current supply capability because of its function as the output buffer, so that the power consumption increases as the power supply voltage increases. Hence, unless a technology for operating the driver circuit used on the ATM-LAN physical interface at a low voltage is established, it has been found that the operating power supply voltage of a semiconductor integrated circuit for ATM-LAN physical layer interface that will include such a driver circuit cannot be lowered. Today, in personal computers and communications terminals that are reduced in size to such an extent as will make them portable, a growing importance is being attached to the reduction in power consumption of the circuit because of the fact that they operate on batteries. Considering the fact that the ATM-LAN interface circuit or the ATM-LAN adapter card in the form of an integrated circuit card, which is applied to such personal computers and communications terminals, will be equipped with semiconductor integrated circuits for physical layer interface, the inventors have found that the low-voltage operation of the driver circuit has significance involving the reduced power consumption on the part of the ATM-LAN adapter card.

The object of the present invention is to provide a technology for operating at a low voltage a driver circuit used for the ATM-LAN physical interface.

Another object of this invention is to provide a transmission line drive circuit for ATM-LAN physical layer



that makes it possible to reduce the power supply voltage of the physical layer interface semiconductor integrated circuit used in the ATM-LAN system.

5 Still another object of this invention is to provide an ATM-LAN adapter IC card that can be operated at a low voltage.

These and other objects and novel features of this invention will become apparent from the following description in this specification and the accompanying drawings.

10 Representative aspects of the present invention will be briefly explained as follows.

In the ATM-LAN, a transmitting circuit (for example, the element 10 shown in Fig. 1) and a receiving circuit (11) are connected in a one-to-one relation to each other via a transmission line (3). An output driver circuit (50) of the transmitting circuit (10) has its output circuit (21) formed in the CMOS (complementary MOS transistor circuit) configuration. That is, the output circuit (21) includes CMOS output stages (51, 52, 57) each comprising first and second pairs of a P-channel MOS transistor and an N-channel MOS transistor connected in series. The sources of the P-channel MOS transistors are connected to a power supply voltage (V_{dd}) and the sources of the N-channel MOS transistors are connected to a ground potential (V_{ss}). The common drains of the MOS transistors making up the first pair are connected to one of transmission terminals (TxA), and the common drains of the MOS transistors making up the second pair are connected to the other transmission terminal (TxB). An output control circuit

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(20) controlling this output circuit uses the power supply voltage and the ground potential as the operating power supply and performs a push-pull operation on the first pair and the second pair in the CMOS output circuit in phase opposition.

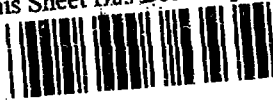
5 The pair of transmission terminals of the output driver circuit are connected to output impedance adjusting resistors (33, 34), which are connected to input terminals of a filter (35) that shapes the transmitted signal waveforms. The output terminals of the filter are coupled to the primary side of a
10 transformer (36) (whose secondary side is connected to the transmission line). As a result, a transmission line drive circuit for an ATM-LAN physical layer is formed, in which the transmitting circuit is connected to the receiving circuit via a transmission line in one-to-one correspondence.

15 Because the CMOS output stages are used in the output circuit (21) of the output driver circuit (50) for transmission, the gate-source voltage of the P-channel MOS transistors connected to the power supply voltage side when they are turned on does not depend on the voltage of the
20 transmission terminal but is virtually at the level of the power supply voltage. This can reduce the on resistances of the MOS transistors (Q1, Q3, Q5, Q7, Q9, Q11) on the power supply voltage side that make up the output circuit, compared with an output circuit that performs the push-pull operation
25 on the series-connected NMOS transistors. Hence, not only can the operation voltage of the output driver circuit be reduced, but it is also possible to lower the operation voltage of



internal circuits making up a semiconductor integrated circuit chip (9) for ATM-LAN physical layer control that includes the output driver circuit.

As described above, in a system configuration that
5 employs a filter 35 (45) to provide the required transmitted signal waveform defined by the template for a 25 Mb/s (megabits/sec) ATM-LAN physical layer described in the ATM_Forum/94-1008R5 and also output impedance adjusting resistors (33, 34), for example, it is possible to produce the
10 signal amplitude defined by the template with a lower power supply voltage of 3.3 volts than 5 volts by forming the output circuit (21) in a CMOS configuration to reduce the on resistances of the constituent MOS transistors. In this way, forming the output circuit (21) in the CMOS configuration is
15 best suited for reducing the operation power supply voltage of the semiconductor integrated circuit chip (9) such as a PMD semiconductor chip applied to the 25 Mb/s ATM-LAN physical layer described in the ATM_Forum/94-1008R5, which will be explained later. Because the output signal amplitude that
20 satisfies the template can be obtained easily even when the turn ratio between the primary and the secondary coil of the transformer (36) is set at 1:1, there is no need to increase the number of turns on the secondary side of the transformer (36) even by increasing the operating current flowing in the
25 output circuit. This also contributes to reducing the power consumption of the semiconductor integrated circuit chip (9) for the ATM-LAN physical layer control.



The transformer has an inductance of more than 1 mH, a series resistance of less than 5 ohm, a coupling coefficient of more than 0.999, an equivalent capacitance of less than 5 pF and a frequency band of 12 kHz to about 16 MHz.

5 In a state that the power supply to the semiconductor integrated circuit chip (9) for ATM-LAN physical layer control is cut off, N-type well regions of the PMOS transistors (Q1, Q3, Q5, Q7, Q9, Q11) making up the output stages of the output driver circuit (50) in the semiconductor chip (9) are not
10 supplied with a power supply voltage (Vdd) and are floated. In the ATM-LAN, because the transmitting circuit and the receiving circuit are coupled to the transmission line in the one-to-one relationship, the drain regions of the PMOS transistors (Q1, Q3, Q5, Q7, Q9, Q11) are not supplied with a
15 high level of current through the transmission lines (3, 4) even when the N-type well regions are floated, so that a large current will not flow from the drains to the N-type well regions, eliminating the possibility of damage to the PMOS transistors (Q1, Q3, Q5, Q7, Q9, Q11). When, however, the
20 CMOS type output driver circuit is applied to the Ethernet where the output terminals of a plurality of output driver circuits are commonly connected to one transmission line, there is a possibility that the N-type well region of the output driver circuit at a certain node, when it is floated,
25 may be supplied with a high level of current by the output operation of other node. That is, when the output stages of the output driver circuit of the Ethernet are formed in CMOS



duration, a large current may flow from the drain into
N-type well region, damaging the PMOS transistors.

Because of their function as the output circuit, the MOS
transistors making up the CMOS output stages of the output
driver circuit (50) have their current supply capabilities
(transistor sizes) set relatively high. Further, two or more
CMOS output stages each with the first and second pairs are
arranged in parallel and a first timing control means (54)
that shifts the timing of push-pull operation of each stage is
incorporated in the output control circuit (20). This makes it
possible to reduce the rate of change of current per unit time
in the supply lines of the power supply voltage (V_{dd}) and the
ground potential (V_{ss}) to the CMOS output stage, which in turn
reduces the power supply noise.

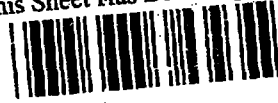
Second timing control means (for example, elements 80,
81, 82, 83 in Fig. 16) that delay the turn-on operation of the
MOS transistors making up the CMOS output stages, compared
with the turn-off operation, are also adopted in the output
control circuit (20). This reduces the through-current
flowing in the CMOS output stages during the transient
response. In this respect, too, the present invention
contributes to reduction in power supply noise and power
consumption.

When three CMOS output stages are arranged in parallel,
the size ratio between the MOS transistors making up the first
CMOS output stage (52), the MOS transistors making up the
second CMOS output stage (51) and the MOS transistors making



up the third CMOS output stage (57) is set roughly to
1:2.5:6.25. Delay means (80, 81, 82, 83), which, with respect
to the turn-on operation of the MOS transistors included in
the first CMOS output stage, delay the start of the turn-on
5 operation of the MOS transistors included in the second CMOS
output stage by about 3 ns and the start of the turn-on
operation of the MOS transistors included in the third CMOS
output stage by about 6 ns, are employed in the output control
circuit (20). This arrangement achieves a significant
10 reduction in power supply noise.

An ATM-LAN adapter card (200), an IC card, that is
attached to a terminal device and connected to the
transmission line and performs the ATM-LAN interface control
between this terminal device and another terminal device
15 connected to this terminal device via the transmission line,
is provided on a card substrate: an ATM-LAN physical layer
control chip (9) having a transmitting circuit (10) and a
receiving circuit (11) for ATM-LAN physical layer; resistors
(33, 34) for adjusting the output impedance of the
20 transmitting circuit; a filter (35) connected in series to the
resistors for shaping the transmitted signal waveform; a
transmission coupling transformer (36) for transmitting the
output of the filter to the transmission line (3); a reception
coupling transformer (47) for transmitting received signals
25 from the transmission line (4) to the receiving circuit (11);
and a control circuit (202, 203, 204, 205) that performs
transmission and reception protocol processing for ATM-LAN.



The transmitting circuit (10) on the ATM-LAN physical layer control chip may use the output driver circuit (50). The output driver circuit (50) can include an output circuit (21) and an output control circuit (20 in Fig. 16). The output circuit (21) includes a plurality of CMOS output stages each consisting of first and second pairs of a P-channel MOS transistor and an N-channel MOS transistor connected in series, with the source of the P-channel MOS transistor in each CMOS output stage connected to the power supply voltage (Vdd), with the source of the N-channel MOS transistor connected to the ground potential (Vss), with the common drain of the MOS transistors making up the first pair connected to one transmission terminal (TxA) and with the common drain of the MOS transistors making up the second pair connected to the other transmission terminal (TxB). The output control circuit uses the power supply voltage and the ground potential as the operating power supply, causes the first and second pairs of each CMOS output stage to perform push-pull operation in phase opposition, staggers the push-pull operation timings for the respective CMOS output stages, and delays the start of the turn-on operation of the MOS transistors in a certain CMOS output stage compared with that of the turn-off operation.

By forming the PMD_@(Physical Media Dependent) semiconductor chip 9 so as to satisfy the requirements of the transmitted signal waveform defined by the template for a 25 Mb/s ATM-LAN physical layer specified in the ATM_Forum/94-1008R5 with the operating voltage of 3.3 volts, it is possible



to suppress the power consumption of the ATM-LAN physical layer control chip (9) to a low level of, for example, 200 mW. Because the ATM-LAN physical layer control chip (9) is a circuit portion that consumes power most in the ATM-LAN adapter card (200), if the power consumption of the ATM-LAN physical layer control chip (9) can be kept at around 200 mW, it is possible to reduce the overall power consumption of the ATM-LAN adapter card (200) to about 1W.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram showing an example of an output driver circuit for transmission in which the PMD semiconductor chip for an ATM physical layer is connected to the transmission line in one-to-one correspondence.

Fig. 2 is a block diagram showing an example of a system configuration of the ATM-LAN physical layer.

Fig. 3 is an example of a block diagram of the PMD semiconductor chip.

Fig. 4 is a block diagram of the output circuit for comparison that comprises series circuits of NMOS transistors.

Fig. 5 is an explanatory diagram showing a template for one-bit consecutive data repetition described in the ATM_Forum/94-1008R5.

Fig. 6 is an explanatory diagram showing a template for two-bit consecutive data repetition described in the ATM_Forum/94-1008R5.



Fig. 7 is an explanatory diagram showing a template for three-bit consecutive data repetition described in the ATM_Forum/94-1008R5.

5 Fig. 8 is an explanatory diagram showing a template for four-bit consecutive data repetition described in the ATM_Forum/94-1008R5.

Fig. 9 is an explanatory diagram showing a template for five-bit consecutive data repetition described in the ATM_Forum/94-1008R5.

10 Fig. 10 is an example of an equivalent circuit of a filter that meets the requirement of the transmission waveform defined by the template.

Fig. 11 (A) and Fig. 11(B) are explanatory diagrams for illustrating return loss.

15 Fig. 12 is a layout diagram of the MOS transistors forming the output stages of the output drive circuit.

Fig. 13 is a cross section taken along the line a-a of Fig. 12.

20 Fig. 14 is a circuit diagram showing another example of an output driver circuit for transmission that has its PMD semiconductor chip for an ATM physical layer connected to the transmission line in a one-to-one correspondence.

Fig. 15 is an example of a delay circuit included in the output driver circuit of Fig. 14.

25 Fig. 16 is an example of the output driver circuit 50 having three CMOS output stages arranged in parallel.

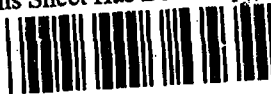


Fig. 17 is an equivalent circuit of the circuit to be simulated for evaluating power supply noise.

Fig. 18 (A) is a delay circuit (DEL 1) for the second CMOS output stage used in the simulation.

5 Fig. 18 (B) is a delay circuit (DEL 2) for the second CMOS output stage used in the simulation.

Fig. 19 (A) is a delay circuit (DEL 3) for the third CMOS output stage used in the simulation.

10 Fig. 19 (B) is a delay circuit (DEL 4) for the third CMOS output stage used in the simulation.

Fig. 20 is an explanatory diagram showing a plurality of simulation conditions in connection with the transistor size ratios and delay times.

15 Fig. 21 is an explanatory diagram showing example size conditions for MOS transistors to obtain the transistor size ratios and delay times under the simulation conditions #1 to #6.

20 Fig. 22 is an explanatory diagram showing examples of transistor size ratios to produce delay times set in the delay circuits under the simulation conditions #5, #7 to #10.

Fig. 23(A) and 23(B) are explanatory diagrams showing an example of the supply current waveform obtained by the simulation.

25 Figs. 24(A), 24(B) and 24(C) are explanatory diagrams, among which Fig. 24(A) showing the method of determining the amount of power supply current noise based on the power supply current waveform obtained by the simulation and, at Figs.



24(B) and 24 (C), the amount of power supply current noise thus determined.

Fig. 25 is an example of a block diagram of the ATM-LAN adapter card.

5 DETAILED DESCRIPTION

System Configuration of ATM-LAN Physical Layer

Fig. 2 shows one example of the system configuration of the ATM-LAN physical layer. The ATM-LAN is a LAN with a dedicated transmission line. The dedicated transmission line
10 LAN has each transmission line connected to only one node and these transmission lines are concentrated to a hub and switched. In Fig. 2, reference numeral 1 (1a-1i) represents terminal devices such as personal computers and workstations, 2 (2a-2i) represents ATM-LAN interface circuits provided one-
15 to-one for respective terminal devices, 3 (3a-3i) and 4 (4a-4i) represent transmission lines, 5 represents an ATM hub where the transmission lines 3, 4 are concentrated, and 6 and 7 represent high-speed transmission cables.

The ATM-LAN interface circuits 2 (2a-2i) and the hub 5
20 include PMD (Physical Media Dependent) sublayer semiconductor chips 9 for ATM-LAN (hereinafter referred to simply as PMD semiconductor chips), each of which has a transmitting circuit 10 and a receiving circuit 11. The PMD semiconductor chips 9 of the ATM-LAN interface circuits 2 (2a-2i) and the PMD
25 semiconductor chips 9 of the ATM hub 5 are so arranged that the output of the transmitting circuit 10 on the interface



circuit side or the hub side is connected to the input of the receiving circuit 11 on the other side via the transmission lines 3, 4. Though not shown, the transmission lines 3, 4 are connected to the transmitting circuit 10 and the receiving circuit 11 through transformers (coupling transformers) having super wide band characteristics.

The ATM hub 5 has, in addition to the PMD semiconductor chips 9, a switch matrix 12 as an ATM exchange and a multiplex separator 13 for high speed transmission between hubs. The high-speed transmission cables 6, 7 connected to the multiplex separator 13 are connected to other hubs similar to the hub 5 and to routers (not shown). As is obvious from the figure, the ATM-LAN at least in the physical layer has no output data collision problem because the transmission and reception between the transmitting circuit 10 and the receiving circuit 11 are performed in one-to-one correspondence.

When user data for transmission is given from the terminal device 1 to the ATM-LAN interface circuit 2, the ATM-LAN interface circuit 2 divides the data into sections of 48 bytes and adds a 5-byte header as destination header information to each section and transmits the data one cell at a time through the transmission line 3, the cell having a fixed length of 53 bytes, which is the sum of 48-byte data and 5-byte header. The ATM hub 5, upon receiving the cell through the transmission line 3 by the receiving circuit 11, rapidly switches or routes the cell by the switch matrix 12 according to the destination header information contained in the cell.

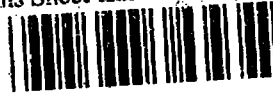


The cell is then routed to a destination terminal device 1 on the receiving side. After having arrived at the ATM-LAN interface circuit 2 of the destination terminal device on the receiving side, the cell is checked for the destination header and then recovered into the original user data. If the destination terminal device on the receiving side is not connected to the same ATM hub 5 as of the transmitting side, the cell is transmitted through the multiplex separator 13 through the high-speed transmission cable 6.

10 PMD Semiconductor Chip

Fig. 3 shows a block diagram of the PMD semiconductor chip 9. The PMD semiconductor chip 9 is formed, for example, on a single semiconductor substrate such as a single crystalline silicon by the CMOS integrated circuit fabrication technology. The PMD semiconductor chip 9 includes a transmitting circuit 10 and a receiving circuit 11 and also has a pair of transmission terminals TxA, TxB, a pair of reception terminals RxA, RxB, a data output terminal RxDATA, a data input terminal TxDATA, a clock input terminal TxCLK, and a clock output terminal RxCLK, these terminals being representatively shown. There are shown, as external power supply terminals, terminals that receive a power supply voltage Vdd such as 3.3 volts and a ground potential Vss such as 0 volts.

25 The transmitting circuit 10 includes a flip-flop 25 such as D-type latch, an output control circuit 20, and an output



circuit 21. The output control circuit 20 and the output circuit 21 form an output driver circuit 50 on the transmitting side. Data received from the data input terminal TxDATA is latched by the flip-flop 25 in synchronism with the clock signal TxCLK. The latched data is fed to the output control circuit 20. The output control circuit 20 sends a control signal based on the logical value of the data supplied thereto to the output circuit 21, which in turn drives the terminal TxA to the power supply voltage Vdd and the terminal TxB to the ground potential Vss, or drives the terminals TxA, TxB to the opposite states. Although detailed explanation will be given later, to the circuit configuration considerations are given so as to minimize the power supply noise caused by the output operation of the output circuit 21 as well as the through-current.

The receiving circuit 11 on the PMD semiconductor chip 9 includes an input buffer 22, a PLL circuit 23 and an output latch 24. The reception terminals RxA, RxB are supplied with a bias voltage VB from a voltage follower circuit 222 through resistors 220, 221. The signals fed to the reception terminals RxA, RxB are sent to a waveform equalizer 223 that shapes the waveforms of the signals which were degraded on the transmission line.

The PLL circuit 23 includes a phase comparator (PC) 230, a frequency comparator (FC) 231, a signal detection circuit (E-Det) 232, a selector (SEL) 234, a charge pump (C-Pump) 235, and a voltage controlled oscillator (VCO) 236. The frequency



comparator 231 produces an error signal according to the frequency difference between a clock signal fed from the clock terminal TxCLK and a clock signal fed back from the voltage control oscillator 236. The phase comparator 230 generates an error signal according to the phase difference between the output signal of the waveform equalizer 223 and the clock signal fed back from the voltage control oscillator 236. The signal detection circuit 232 detects whether the output of the waveform equalizer 223 contains an effective signal component, according to the energy of that signal, for example. The signal detection circuit 232, when it detects an effective signal, causes the selector 234 to select the output of the phase comparator 230 and, when it does not detect an effective signal, causes it to select the output of the frequency comparator 231. The charge pump 235 generates a current according to the error signal output from the selector 234, the generated current being converted into a specified voltage signal by a low-pass filter in the charge pump. The voltage controlled oscillator 236 produces a signal having an oscillation frequency corresponding to the level of the voltage signal supplied thereto.

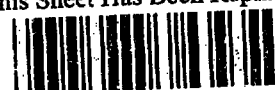
When the output signal of the waveform equalizer 223 is not an effective signal, the PLL circuit 23 performs synchronization with the clock signal supplied from the clock terminal TxCLK, so that when the output signal of the waveform equalizer 223 later becomes effective, the phase pull-in can be performed efficiently. When the output signal of the

waveform equalizer 223 becomes effective, the output of the voltage control oscillator 236 is made a clock signal synchronized with the output signal of the waveform equalizer 223. The data latch 24 latches the output signal of the waveform equalizer 223 in synchronism with the output clock signal from the voltage controlled oscillator 236. As a result, the received data is output from the data output terminal RXDATA and at the same time a clock signal synchronized with it is output from the clock terminal RXCLK.

Coupling of PMD Semiconductor Chip and Transmission Line

Fig. 1 shows a detailed example of the output circuit 21 with the PMD semiconductor chips 9 on the transmitting and receiving sides connected one-to-one through the transmission lines 3, 4. The PMD semiconductor chips 9 on the transmitting and receiving sides can selectively assume one of three states---transmitting, receiving and transmitting/receiving states. Hence, in the PMD semiconductor chip 9, the transmitting circuit 10 and the receiving circuit 11 on the same semiconductor substrate are affected mutually by the noise. Because the receiving circuit 11 in particular is susceptible to influences of power supply noise produced by the transmitting circuit 10, reducing the noise of the transmitting circuit 10 is important.

In Fig. 1, the transmission line 3 is shown as a twisted pair including 31 and 32 and the transmission line 4 is illustrated as a twisted pair made up of 41 and 42. The



twisted pair may use STP (shielded 150 ohm twisted pair), UTP (unshielded 100 ohm twisted pair) and FTP (unshielded 120 ohm twisted pair). In the transmission channel between the transmitting circuit 10 and the receiving circuit 11 connected by the transmission line 3, the transmission terminals TxA, TxB of the transmitting circuit 10 are connected through the input impedance adjusting resistors 33, 34 to the input terminals of the filter 35, whose output terminals are connected to the primary side of the transformer 36. The secondary side of the transformer 36 is connected to one end of the transmission line 3 (31, 32), whose other end is connected to the primary side of a transformer 37. The secondary side of the transformer 37 is connected to the reception terminals RxA, RxB of the receiving circuit 11, and the transmission channel between the transmitting circuit 10 and the receiving circuit 11 interconnected by the transmission line 3 is terminated by the receiving circuit 11. Similarly, in the transmission channel between the transmitting circuit 10 and the receiving circuit 11 interconnected by the transmission line 4, the transmission terminals TxA, TxB of the transmitting circuit 10 are connected through the output impedance adjusting resistors 43, 44 to the input terminals of the filter 45, whose output terminals are connected to the primary side of a transformer 46. The secondary side of the transformer 46 is connected to one end of the transmission line 4 (41, 42), whose other end is connected to the primary side of a transformer 47. The



secondary side of the transformer 47 is connected to the reception terminals RxA and RxB of the receiving circuit 11, and the transmission channel between the transmitting circuit 10 and the receiving circuit 11 interconnected by the transmission line 4 is terminated by the receiving circuit 11. In Fig. 1, while the details of the receiving circuit 11 and the transmitting circuit 10 are shown only for the ATM-LAN interface circuit 2 side, the receiving circuit 11 and the transmitting circuit 10 in the ATM hub 5 are also similarly configured.

Configuration of the Output Driver Circuit

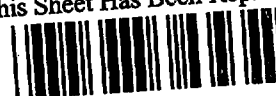
As shown in Fig. 1, the output circuit 21 forming the output driver circuit 50 of the transmitting circuit 10 has, for example, a second output stage 51 and a first output stage 52 connected in parallel. The second output stage 51 has a third CMOS circuit and a fourth CMOS circuit, the third CMOS circuit including a P-channel MOS (simply referred to as PMOS) transistor Q1 and an N-channel MOS (simply referred to as NMOS) transistor Q2 connected in series, the fourth CMOS circuit including a PMOS transistor Q3 and an NMOS transistor Q4 connected in series. The first output stage 52 has a first CMOS circuit and a second CMOS circuit, the first CMOS circuit including a PMOS transistor Q5 and an NMOS transistor Q6 connected in series, the second CMOS circuit including a PMOS transistor Q7 and an NMOS transistor Q8 connected in series. The source terminals of the NMOS transistors Q2, Q4, Q6, Q8



are connected to the ground potential V_{ss} while the source terminals of the PMOS transistors Q1, Q3, Q5, Q7 are connected to the power supply voltage V_{dd} . The common drain of the PMOS transistor Q1 and the NMOS transistor Q2 is connected to the common drain of the PMOS transistor Q5 and the NMOS transistor Q6, and their connecting point is connected to one of the transmission terminals TxA. Similarly, the common drain of the PMOS transistor Q3 and the NMOS transistor Q4 is connected to the common drain of the PMOS transistor Q7 and the NMOS transistor Q8, and their connecting point is connected to the other transmission terminal TxB.

The output control circuit 20 includes a CMOS inverter 53 for inverting the logical value of the signal Vs output from the flip-flop 25, a delay circuit 54 for delaying the signal Vs and a CMOS inverter 55 for inverting the logical value of the output of the delay circuit 54. The signal Vs is fed to the gates of the PMOS transistor Q7 and the NMOS transistor Q8, and the output of the CMOS inverter 53 is sent to the gates of the PMOS transistor Q5 and the NMOS transistor Q6.

The output of the delay circuit 54 is fed to the gates of the PMOS transistor Q3 and the NMOS transistor Q4, and the output of the CMOS inverter 55 is given to the gates of the NMOS transistor Q2 and the PMOS transistor Q1. The delay circuit 54, when the logic value of the signal Vs is changed, causes the transient response timing of the CMOS circuit making up the second output stage 51 to differ from the transient response timing of the CMOS circuit making up the first output



stage 52. For example, even numbered CMOS inverters may be connected in series to produce a desired delay time.

When the input signal V_s goes to a high level (a level of the power supply voltage V_{dd}), the NMOS transistor Q8 and the PMOS transistor Q5 are turned on and the PMOS transistor Q7 and the NMOS transistor Q6 are turned off, causing a current to flow through the primary side coil of the transformer 36 from the transmission terminal TxA to the transmission terminal TxB. Next, when the output of the delay circuit 54 is held high with a certain delay time, the NMOS transistor Q4 and the PMOS transistor Q1 are turned on and the PMOS transistor Q3 and the NMOS transistor Q2 are turned off, further increasing the current flowing through the primary side coil of the transformer 36 from the transmission terminal TxA to the transmission terminal TxB. When the input signal V_s goes to a low level (the ground potential V_{ss}), the PMOS transistor Q7 and the NMOS transistor Q6 are turned on and the NMOS transistor Q8 and the PMOS transistor Q5 are turned off, causing a current to flow through the primary side coil of the transformer 36 from the transmission terminal TxB to the transmission terminal TxA. Next, when the output of the delay circuit 54 is held low after a specified delay time, the PMOS transistor Q3 and the NMOS transistor Q2 are turned on and the NMOS transistor Q4 and the PMOS transistor Q1 are turned off, further increasing the current flowing through the primary coil of the transformer 36 from the transmission terminal TxB to the transmission terminal TxA. As a result, when the input





signal V_s is changed like a pulse, a pulse voltage is induced in the primary side of the transformer 36. Thus, on the secondary side of the transformer 36, a pulse voltage is generated according to the turn ratio of the coil. The pulse voltage generated on the secondary side of the transformer 36 is transmitted through the transmission line 3 and through the transformer 37 to the reception terminals R_{xA} , R_{xB} of the receiving circuit 11. The reception terminals R_{xA} , R_{xB} have between them series connected resistors 220, 221, to the connecting point of which is applied a bias voltage V_B . The pulse voltage signals fed to the reception terminals R_{xA} , R_{xB} are shaped by the waveform equalizer 223 before being taken in.

Sequential Driving of the First Output Stage and the Second Output Stage

In the output driver circuit 50 of Fig. 1, because in the event of a change in the signal V_s , the on-off operation start timing of the MOS transistors making up the second output stage 51 is shifted from the on-off operation start timing of the MOS transistors making up the first output stage 52, it is possible to reduce the rate of change of current per unit time in the power supply lines of the power supply voltage V_{dd} and the ground potential V_{ss} . This in turn reduces power supply noise in the voltage V_{dd} power supply line and the ground potential V_{ss} power supply line on the PMD semiconductor chip 9. While the example of Fig. 1 uses two output stages, the



output driver circuit may have three or more output stages for the purpose of reducing the power supply noise.

Forming the Output Stage in CMOS Configuration

The output circuit 21 forming the output driver circuit 50 of Fig. 1 is fabricated using CMOS transistors as described above. Hence, the gate-source voltages of the MOS transistors Q1-Q8 are not affected by the voltages of the transmission terminals TxA, TxB connected to the primary coil of the transformer 36. For the embodiment shown in Fig. 1, the operating voltages of the internal circuits of the PMD semiconductor chip 9 are the power supply voltage Vdd and the ground potential Vss. Therefore, the output circuit 21 uses as the operating voltage the power supply voltage Vdd and the ground potential Vss. Because the MOS transistors Q1-Q8 of the output circuit 21 are selectively supplied with the power supply voltage Vdd or the ground potential Vss at their gates for their switching control, the gate-source voltages of the MOS transistors Q1-Q8 are at the level of the power supply voltage Vdd when they are on. This means that the on resistance of the MOS transistors Q1-Q8 can be reduced well below the impedance of the transformer 36.

On the other hand, as shown in Fig. 4 in an output circuit in which a series circuit of NMOS transistors Q20, Q21 and a series circuit of NMOS transistors Q22, Q23, both operating on the power supply voltage Vdd and the ground potential Vss, are push-pull operated in phase opposition, the



gate-source voltages of the NMOS transistors Q20, Q22 depend on the voltages of the transmission terminals TxA and TxB, so that when the output circuit and its control circuit are operated by a single operation voltage, the gate-source
5 voltages of the NMOS transistors Q20, Q22 cannot be given the level of power supply voltage Vdd when they are on. If the gate-source voltages of the NMOS transistors Q20, Q22 when they are on are to be set at the level of the power supply voltage Vdd to sufficiently reduce the on resistance of the
10 MOS transistors Q20, Q22, the amplitude of the signal Vs (refer to Fig. 3) needs to be set greater than the power supply voltage Vdd and also the operating voltage of the inverter 56 needs to be set higher than the power supply voltage Vdd.

15 Letting β be a constant determined by the MOS transistor, ω the gate width of the MOS transistor, L the gate length of the MOS transistor, VGS the gate-source voltage of the MOS transistor, Vth the threshold voltage of the MOS transistor, and VDS the drain-source voltage of the MOS transistor, the
20 alternating current on resistance Rm of the MOS transistor can be expressed as follows, based on the approximation expression of the MOS transistor drain-source current in non-saturated regions.

$$R_m = 1 / \{ \beta \times W/L \times (V_{GS} - V_{th} - V_{DS}) \}$$

25 In the case of the CMOS output circuit 21 of Fig. 1, the VGS is set at the power supply voltage Vdd level even when the operating voltage of the PMD semiconductor chip 9 is a single



operating voltage, V_{dd} and V_{ss} . So we obtain

$$R_m = 1/\{\beta \times W/L \times (V_{dd} - V_{th} - V_{DS})\}$$

Thus, the on resistance is determined only by the levels of power supply voltage V_{dd} and ground potential V_{ss} and the size of the MOS transistor and thus can be reduced. In the case of Fig. 4, on the contrary, the gate-source voltage V_{GS} of the NMOS transistors Q20, Q22 cannot be set at the level of the power supply voltage V_{dd} unless the gate voltages of the NMOS transistors Q20, Q22 are set higher than the power supply voltage V_{dd} .

Hence, when the on resistance of the MOS transistors making up the output circuit needs to be reduced and when the operating voltages of the internal circuits making up the PMD semiconductor chip 9 needs to be lowered, it is considered that the output circuit of the output driver circuit 50 is essentially formed of CMOS transistors.

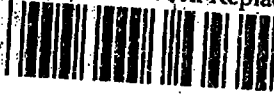
Specifications of ATM-LAN Physical Layer

Next, we will explain about the case where the circuit configuration of Fig. 1 conforms to a particular ATM-LAN specification. The ATM Forum, set up to spread the use of ATM as an easy-to-use network buildup technique for user, has produced the ATM technical specifications, and there is a working group on the ATM-LAN. Today, the interface specifications on the 25 Mb/s (Mega-bit/sec) ATM-LAN (data transmission speed in physical layer is 32 Mb/s) also are about to be established. Here, we will focus on the physical



layer part of these interface specifications. This specifications (under consideration) have not yet become a standardized specification at the ATM forum.

Figs. 5 to 9 show the templates (pulse masks) described from p.4 to p.8 of ATM_Forum/94-1008R5, a draft on such physical layers. The copyright of the draft is owned by the ATM Forum. In the ATM-LAN physical layer interface, to improve the transmission efficiency, the number of consecutive bits (number of symbols) of logical "0" or "1" in the information transmitted is limited to five in connection with the scrambling and encoding. The template is a standard for defining a signal waveform (output signal waveform of the transformer) for each group of symbols with the same logical value. Fig. 5 represents a case where the number of symbols with the same logical value is one (one-bit consecutive data repetition), Fig. 6 represents a case of two symbols (two-bit consecutive data repetition), Fig. 7 represents a case of three symbols (three-bit consecutive data repetition), Fig. 8 represents a case of four symbols (four-bit consecutive data repetition), and Fig. 9 represents a case of five symbols (five-bit consecutive data repetition). In these templates shown in the Figures that define the signal waveforms for the respective numbers of symbols, the abscissa represents a relative value of time (%) and the ordinate represents a relative value of the amplitude (zero-to-peak). The template defines an upper limit waveform and a lower limit waveform, and actual output waveforms need to be within the range



between these limits. The actual time on the abscissa of the waveform defined by the template is determined by the transmission rate and the number of symbols. The actual amplitude on the ordinate of the waveform defined by the

5 template is determined by the amplitude defined based on the kind of transmission line and the relative value on the ordinate. For example, in the ATM_Forum/94-1008R5, the peak-to-peak transmitter launch amplitude (TLA) is defined to be 2.7 volts < TLA < 3.4 volts for UTP, 3.3 volts < TLA < 4.2
10 volts for STP and 2.95 volts < TLA < 3.75 volts for FTP. Hence, in each template, a relative value of 1 on the ordinate is taken as the center value in the zero-to-peak amplitude range, which is half of the peak-to-peak amplitude range defined by the kind of transmission line.

15 To transmit the transmitted waveforms that satisfy the templates shown in Figs. 5 to 9 from the secondary coils of the transformers 36, 46, the filters 35, 45 shown in Fig. 1 are provided. One example of an equivalent circuit of the filters 35, 45 is shown in Fig. 10. This filter circuit
20 shapes the almost rectangular pulse signals output from the transmission terminals TxA, TxB into waveforms that meet the templates.

Regarding the ATM-LAN physical layer, the ATM_Forum/94-1008R5 further defines a transmitter return loss (TRL). The
25 return loss is defined to be more than 14 dB for the frequency band of 1-6 MHz, more than 12 dB for the frequency band of 6-17 MHz, and more than 8 dB for the frequency band of 17-25



MHz. Now, the return loss will be explained referring to Figs. 11(A) and 11(B). For easy understanding, the signal source V_s , the impedance on the signal source side r_0 , the transformer, the transmission line and the load side impedance R_L , all shown on Fig. 11(A), are modeled and represented as an equivalent circuit shown in Fig. 11(B). In Fig. 11(B), symbol L represents the inductance of the transformer, r_t represents the series resistance of the transformer, and k represents the coupling factor. Symbol kL designates the inductance of the main magnetic flux of the transformer and $(1-k)L$ denotes the leakage inductance. The impedance Z_L of the load side as seen from the signal source V_s is expressed by

$$Z_L = r_t + j\omega(1-k)L + \{ \omega^2 kLL(1-k) + j\omega kL(r_t + R_L) \} / (r_t + R_L + j\omega L)$$

where $\omega = 2\pi f$ and f is frequency.

In the above expression of the impedance Z_L , assuming that $k=1$ and $\omega L \gg r_t + R_L$, the impedance Z_L can be simplified as follows: $Z_L \approx 2r_t + R_L$.

The return loss is defined to be expressed by $10 \times \log(1/(PP))$ where P (reflection factor) is $P = |(r_0 - Z_L)/(r_0 + Z_L)|$. Hence, to satisfy the return loss defined by the ATM_Forum/94-1008R3 relatively easily, it is desirable that a high performance transformer that meets the above conditions of $k=1$ and $\omega L \gg$ be used. Considering these factors, an example of desirable specifications of the actually used transformers 36, 37, 46, 47 is the inductance

(L) = 1 mH, the series resistance (rt) = 5 ohm, the coupling factor (k) = 0.999 and the equivalent capacitance = 5 pF.

Another example of desirable specifications may be the inductance (L) of 1 mH or higher, the series resistance (rt) of 5 ohm or lower, the coupling factor (k) of 0.999 or higher and the equivalent capacitance of 5 pF or lower.

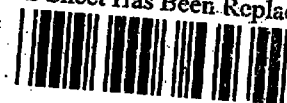
The transformers 36, 37, 46, 47 used in the 25 Mb/s ATM-LAN (data transmission rate in physical layer is 32 Mb/s) require a super wide band specification of from 12KHz to approximately 16 MHz. The lower limit of the band is stipulated by the ATM_Forum/94-1008R3 and its upper limit is determined by the data transmission rate in the physical layer of 32 Mb/s.

Relationship between ATM-LAN Physical Layer Specifications and Use of CMOS Output Stages

As described above, to meet the requirements of the sending signal waveform defined by the template for 25 Mb/s ATM-LAN physical layer described in the ATM_Forum/94-1008R5, the filter 35 (45) with the circuit configuration of Fig. 10 must be used and the transmitted signal from the transformer 36 (46) needs to have a zero-to-peak signal amplitude of about 2 V as defined by the template. In addition, a resistor 33 (34) for impedance matching with the transmission line side must be provided before the filter 35 (45) to minimize the influences of the voltage reflection.



Therefore, because the signals output from the output circuit 21 have voltage losses and drops due to the filters and resistors, the on resistances of the MOS transistors making up the output stages of the output circuit 21 should desirably be as small as possible in view of meeting the signal amplitude requirements defined by the template. As described above, because this embodiment has the output stage (output circuit 21) formed of CMOS transistors (i.e., the on resistances of MOS transistors making up the circuit are small), this embodiment is particularly suited for reducing the operation voltage of the PMD semiconductor chip 9. Thus, in this embodiment, the power supply voltage Vdd is set at 3.3 volts. Further, because the output stage (output circuit 21) is formed into a CMOS configuration, i.e., the on resistances of the MOS transistors connected to the power supply voltage Vdd side are made small, it is possible to produce easily the output signal amplitude that meets the template even when the turn ratio between the primary coil and the secondary coil of the transformer 36 (46) is set at 1:1. If the output stage is formed of only NMOS transistors, although it may be possible to obtain an output signal amplitude that meets the template by increasing the number of turns of the secondary coil of the transformer even when the on resistance of the NMOS transistors are large, the amount of current flowing into the output stage increases contrary to the intention of lowering the power consumption. In a simulation, the inventors of this invention were able to produce a transmitted waveform



conforming to the template by driving the output driver circuit 50 with the power supply voltage Vdd of 3.3 volts.

Non-breakdown of PMOS Transistors Included in the Output Stage

In a state that the power supply to the PMD semiconductor chip 9 is cut off, the N-type well regions of the PMOS transistors Q1, Q3, Q5, Q7 making up the output stage of the output driver circuit 50 on the transmitting side of the PMD semiconductor chip 9 are not supplied with the power supply voltage Vdd and are floated. At this time, as can be seen from Figs. 2 and 1, because the ATM-LAN at least in the physical layer performs transmission and reception in one-to-one relationship, the transmitting circuit 10 is not supplied with signals from other transmitting circuits 10. Hence, even when the N-type well regions are floated, the drains of the PMOS transistors Q1, Q3, Q5, Q7 are not supplied with high level signals through the transmission line 3, so that no large current flows from the drains into the N-type well regions, eliminating the possibility that the PMOS transistors Q1, Q3, Q5, Q7 be broken down. The transmitting circuit 10 receives only the reflection signal of the signal it outputted. The reflection of the output signal can be reduced by establishing the impedance match.

Countermeasure against Latchup of the Output Stage

Fig. 12 shows a layout of the MOS transistors Q1-Q4 making up the second output stage of Fig. 1. In Fig. 12,



reference numerals 60, 61 represent N-type well regions (N-WELL); 62 and 63 P-type well regions (P-WELL); 64 to 71 the drain or source electrodes of the MOS transistors Q1-Q4; 72 the gates of the MOS transistors Q1, Q2; 73 the gates of the MOS transistors Q3, Q4; and 74 and 75 electrodes for supplying the PMOS transistor substrate. The substrate power supply electrodes 74, 75 are supplied with the power supply voltage Vdd. Fig. 13 is the cross section taken along the line a-a of Fig. 12. As is seen from the figure, the substrate power supply electrode 74 is located adjacent to the P-WELL 63 and the substrate power supply electrode 75 is arranged adjacent to the P-WELL 62. In the layout of Fig. 12, the combination of transistors that turn on simultaneously is Q1 and Q4, or Q2 and Q3, creating a potential gradient in the Y direction, that is, reducing the potential difference between N-WELL 60 and P-WELL 63 and the potential difference between N-WELL 61 and P-WELL 62. At this time, because the N-WELL 60, 61 are supplied with substrate power from the electrodes 74, 75 arranged adjacently to the P-WELL 62, 63, the latchup of the output stage can be effectively prevented.

Reducing the Through-Current in CMOS Output Stage

Fig. 14 shows another configuration of the output driver circuit 50. In Fig. 14, the second output stage 51 that forms the output circuit 21 has its MOS transistors Q1-Q4 larger in size (gate width/gate length) than the MOS transistors Q5-Q8 of the first output stage 52. The output control circuit 20



of Fig. 14, as in Fig. 1, changes the output of the second output stage 51 with a certain delay from a change in the output operation of the first output stage 52. Considering the relatively large size of the MOS transistors of the second output stage 51, a measure is taken to reduce the through-current flowing in the second output stage 51 during the transient response. That is, the measure is delay circuits 80, 81, which, although their control on the first output stage 52 is the same as that of Fig. 1, perform control on the second output stage 51 in such a way as to reduce the delay due to rise change of switch control signals $\phi p1$, $\phi p2$ fed to the PMOS transistors (the off timing is made relatively early) and increase the delay due to fall change of these signals (the on timing is made relatively late), and also to increase the delay due to rise change of switch control signals $\phi n1$, $\phi n2$ fed to NMOS transistors (the on timing is made relatively late) and reduce the delay due to fall change of these signals (the off timing is made relatively early). The input to the delay circuit 80 is the signal V_s and the input to the delay circuit 81 is the output signal of the inverter 53, which is opposite in phase to the input signal V_s .

Fig. 15 shows an example of a circuit configuration of the delay circuits 80, 81. Between the power supply voltage V_{dd} and the ground potential V_{ss} there are provided a series circuit including a PMOS transistor Q30 and an NMOS transistor Q31, a series circuit including a PMOS transistor Q32 and an NMOS transistor Q34, and a series circuit including a PMOS



transistor Q35 and an NMOS transistor Q37. These series circuits each operates as an inverter. Between the MOS transistor Q32 and Q34 is interposed an NMOS transistor Q33 that serves as a delay element or resistor element. Between the MOS transistor Q35 and Q37 is provided a PMOS transistor Q36 that functions as a delay element or resistor element. The gates of the MOS transistors Q32, Q34, Q35, Q37 are commonly connected to the coupling point of the MOS transistors Q32 and Q31; the gate of the MOS transistor Q33 is connected to the power supply voltage Vdd; and the gate of the MOS transistor Q36 is connected to the ground potential Vss. In the delay circuit 80, the signal Vs is fed to the gates of the MOS transistors Q30 and Q31. In the delay circuit 81, the gates of the MOS transistors Q30 and Q31 are fed with the output of the inverter 53. The switch control signal $\phi p1$ ($\phi p2$) is output from the drain of the PMOS transistor Q32, and the switch control signal $\phi n1$ ($\phi n2$) is output from the drain of the NMOS transistor Q37.

In the delay circuit 80 (81), a change in the input signal Vs (output of the inverter 53) is delayed by the two stages of series circuit inverters made up of MOS transistors Q30-Q34 and is reflected on the switch control signal $\phi n1$ ($\phi n2$). It is also delayed by the two stages of series circuit inverters made up of MOS transistors Q30, Q31, Q35-Q37 and is reflected on the switch control signal $\phi p1$ ($\phi p2$). At this time, the switch control signal $\phi p1$ ($\phi p2$) is delayed greater due to fall change than due to rise change by the on



resistance of the MOS transistor Q33. The switch control signal ϕ_{n1} (ϕ_{n2}) is delayed greater due to rise change than due to fall change by the on resistance of the MOS transistor Q36. That is, the on operation of the MOS transistors Q1-Q4

5 of the second output stage 51 is delayed greater than the off operation. Hence, when the output of the second output stage 51 is inverted, the series connected PMOS transistor and NMOS transistor are not turned on simultaneously, thereby reducing the through-current flowing during the transient response.

10 Because the output circuit 21 is required to have relatively large drive capability and current supply capability, such reduction in the through-current can significantly reduce power consumption by the PMD semiconductor chip 9 and power supply noise.

15 Configuration of Three Parallel CMOS Output Stages

Fig. 16 shows an embodiment of the output driver circuit 50 comprising three parallel CMOS output stages. The output circuit 21 of Fig. 16 is a combination of the output circuit of Fig. 14 and third output stage 57. The output control

20 circuit 20 of Fig. 16 is a combination of the output control circuit of Fig. 14 and delay circuits 82, 83.

The third output stage 57 has a fifth CMOS circuit comprising a PMOS transistor Q9 and an NMOS transistor Q10 connected in series and a sixth CMOS circuit comprising a PMOS

25 transistor Q11 and an NMOS transistor Q12 connected in series, with the sources of the MOS transistors Q9, Q11 connected to



the power supply voltage V_{dd} and with the sources of the NMOS transistors Q10, Q12 connected to the ground potential V_{ss} . The common drains of the PMOS transistor Q9 and the NMOS transistor Q10 are connected to one transmission terminal TxA and the common drains of the PMOS transistor Q11 and the NMOS transistor Q12 are connected to the other transmission terminal TxB.

The delay circuits 82, 83 have structures similar to the circuit shown in Fig. 15. The delay circuit 82 sends a switch control signal $\phi p3$ to the gate of the PMOS transistor Q11 and a switch control signal $\phi n3$ to the gate of the NMOS transistor Q12. The delay circuit 83 sends a switch control signal $\phi p4$ to the gate of the PMOS transistor Q9 and a switch control signal $\phi n4$ to the gate of the NMOS transistor Q10. The relation between the switch control signal $\phi p3$ ($\phi p4$) for PMOS transistors and the switch control signal $\phi n3$ ($\phi n4$) for NMOS transistors is the same as that explained referring to Fig. 15. That is, the MOS transistors Q9-Q12 of the third output stage 57 are so arranged that the on operation is delayed greater than the off operation is. The delay times produced by the delay circuits 82, 83 are greater than the delay times produced by the delay circuits 80, 81, and the operation of the third output stage 57 is delayed from the operation of the second output stage 51. For example, when the signal V_s changes from a low level to a high level, the first output stage 52 starts turning on the MOS transistors Q7, Q6 and turning off the MOS transistors Q8, Q5. Then the second

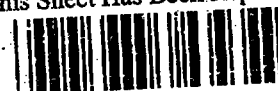


output stage 51 starts to turn on the MOS transistors Q3, Q2 and turn off the MOS transistors Q4, Q1. Finally in the third output stage 57 the MOS transistors Q11, Q10 starts turning on and the MOS transistors Q9, Q12 starts turning off. At this time, in the second and third output stages 51, 57, the turn-on action of the MOS transistors that are to be turned on is started shortly after the turn-off action of the MOS transistors that are to be turned off has been started.

Hence, the parallel configuration of three CMOS output stages is considered to be able to reduce the power supply noise more than the parallel configuration of two CMOS output stages of Fig. 14 can.

Optimization of Transistor Size Ratio and Delay Time of CMOS Output Stage

Next, the result of simulation on the power supply noise will be explained. Fig. 17 shows the circuit for which the simulation was performed. The operation voltage of the circuit of Fig. 17 is the power supply voltage $V_{dd} = 3.3$ volts and the ground potential $V_{ss} = 0$ volts. The signal V_s has a high level of 3.3 volts and a low level of 0 volts. Reference symbols for the MOS transistors shown in Fig. 17 are different from those of Fig. 16, and their correspondence is as follows: MB 1 = Q5, MB 2 = Q6, MB 3 = Q7, MB 4 = Q8, MB 7 = Q1, MB 8 = Q2, MB 9 = Q3, MB 10 = Q4, MB 11 = Q9, MB 12 = Q10, MB 13 = Q11, and MB 14 = Q12. MB 5 and MB 6 denote MOS transistors making up the CMOS inverter 53 of Fig. 16. Figs. 18 (A) and (B) show



the configurations of the delay circuit 80 (DEL1) and the delay circuit 81 (DEL2) , respectively. Figs. 19 (A) and (B) show the configurations of the delay circuit 82 (DEL3) and the delay circuit 83 (DEL4), respectively. The transistors of the circuits shown in Figs. 18(A), 18(B), 19(A) and 19(B) are designated by different symbols from those of Fig. 15, but their circuit configurations correspond to those of Fig. 15.

Fig. 20 shows the simulation conditions, which include #1 to #10. The condition #1 differs from that of Fig. 17 and the output circuit is formed of one CMOS output stage. For example, the output circuit is formed of the first output stage 52 with different transistor size from that of Fig. 17. The conditions #2 to #10 represent cases where the circuit shown in Figs. 17, 18(A), 18(B), 19(A) and 19(B) are used. In the circuits of Figs. 17 to 19(B), the power supply voltage V_{dd} is set at 3.3 volts, the ground potential V_{ss} is set at 0 volts, the high level of the input signal V_s is made the power supply voltage, and the low level is made the ground potential.

The conditions #2 to #6 shown in Fig. 20 represent cases where the delay times of the delay circuits 80, 81 (DEL1, DEL2) are set at a constant value of 2 ns, the delay times of the delay circuits 82, 83 (DEL3, DEL4) are set at a constant value of 4 ns, and the sizes of the transistors making up the three CMOS output stages differ for every stages. The delay times referred to in this simulation are a delay time from the change of the signal V_s to the moment when the gate control



signal of the PMOS transistor changes to low level, and a delay time from the change of signal Vs to the moment when the gate control signal of the NMOS transistor changes to high level. That is, the delay time after the signal Vs has changed until the PMOS transistor or NMOS transistor is turned on is taken into consideration. The delay time after the signal Vs has changed until the PMOS transistor or NMOS transistor is turned off is not positively controlled nor considered. There is no problem with this time delay.

The ratio b:c:d shown in the transistor size column of Fig. 20 means the ratio, the first CMOS output stage 52: second CMOS output stage 51: third CMOS output stage 57. The conditions #7 to #10 represent the case where the size ratio of the transistors making up the three CMOS output stages is set at 1:2.5:6.25 (as described later, the size ratio is the one determined from the simulation results under the conditions #1 to #6 which minimizes the supply current noise) for every output stage and where the delay times of the delay circuits 80, 81 (DEL1, DEL2) are made different from the delay times of the delay circuits 82, 83 (DEL3, DEL4). The transistor size ratio is the ratio of the gate width to the gate length (W/L). As described above, the delay times of the delay circuits 80-83 (DEL1-DEL3) is a delay time of the trailing edge of the gate control signal for the PMOS transistors and a delay time of the leading edge of the gate control signal for the NMOS transistors, with respect to the change in the signal Vs fed to the output control circuit.



Fig. 21 shows one example of size conditions for MOS transistors under which the transistor sizes and delay times are achieved under the above conditions #1 to #6. For example, the condition #8 of Fig. 20 is that the delay times of the delay circuits DEL1, 2 and the delay circuits DEL3, 4 are 3 ns and 6 ns respectively. This means that the PMOS transistors or NMOS transistors of the second CMOS output stage 51 turn on 3 ns after the turn-on of those transistors of the first CMOS output stage 52, and that the PMOS transistors or NMOS transistors of the third CMOS output stage 57 turn on 3 ns after the turn-on of those transistors of the second CMOS output stage.

Fig. 22 shows one example of transistor size ratio at which the delay times are set for the delay circuits DEL1-DEL4 under the conditions #5, #7-#10. The description of W/L:MB18:7 times shown in the remarks column of Fig. 22 means that the W/L value of the MOS transistor MB18 is 7.

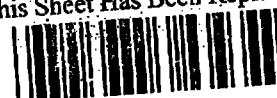
In the simulation, the waveform of a supply current I_{dd} is obtained based on the above conditions. For example, Fig. 23(A) shows a power supply current waveform obtained when simulation was conducted under the condition #1; and Fig. 23(B) shows a power supply current waveform produced when the simulation was performed under the condition #8. To evaluate the power supply noise from the power supply current waveforms obtained under various conditions, an evaluation value $IX = ISUM/(t_2-t_1)$ is determined by calculating the total amount of current $ISUM$ in the region shaded in Fig. 24(A), during the



period (t_2-t_1) corresponding to the transient response time of the output circuit. Hence, the smaller the value of I_X , the smaller the variation of power supply current (the amount of power supply current noise) during the transient response action of the output circuit. Fig. 24(B) shows evaluation values I_X under the above conditions #1 to #6. It will be understood that the smallest power supply current noise is produced under the condition #5. The use of the output driver circuit 50 formed under such a condition did not adversely affect the output voltage waveform of the transformer 36. With the transistor size ratio of the three parallel CMOS output stages provided under the condition #5, the evaluation values I_X similarly determined by the simulation under the conditions #5, #7-#10 are shown in Fig. 24(C). This shows that the smallest power supply current noise is realized under the condition #8. The adoption of the output driver circuit 50 under such a condition did not adversely affect the output voltage waveforms of the transformer 36. Therefore, by adopting the transistor size ratio and the delay time of the condition #8 in the output driver circuit 50, it is verified that the power supply noise can be reduced to very small level.

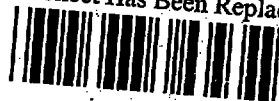
ATM-LAN Card

Fig. 25 shows one embodiment of an ATM-LAN adapter card. The ATM-LAN adapter card 200 is an IC card that is configured in conformity with the standard of PCMCIA (Personal Computer



Memory Card international Association) and constitutes one example of the ATM-LAN interface circuit 2. The ATM-LAN adapter card 200 comprises a microprocessor 202, a ROM 03 which is a firmware in which microprograms are stored, a RAM 204 used as a work area by the microprocessor, an ATM controller 205, a RAM 206 used by the transmission data buffer and the reception data buffer, the PMD semiconductor chip 9 as a physical layer control chip, and a filter-transformer 207, all of which are formed as individual semiconductor integrated circuits are assembled on a card substrate 201 having interconnection on its surface or back. The ATM controller 25, configured to he interface specifications in conformity with the PCMCIA standard, is removably mounted in a terminal device 1 such as of a personal computer. The filter-transformer 207 is connected to the transmission line such as a twisted pair. The filter-transformer 207 is formed as a single chip containing the output resistors 33 and 34, filter 35 and transformer 36, explained referring to Fig. 14.

The ATM controller 205 performs scrambling and encoding processing on the data supplied from the terminal device, generates cells and multiplexes the cells before passing them to the PMD semiconductor chip 9. Also, the ATM controller 205, upon receiving the information received from the PMD semiconductor chip 9, checks the destination header and then performs decomposition of the cells and the decoding processing. Control of the ATM controller 205 is performed by the microprocessor 202 according to the program stored in the



ROM 203. The microprocessor 202, ROM 203, RAM 204, and ATM controller 205 function as control means to control the ATM-LAN transmission protocol.

As can be seen from the foregoing description, the PMD semiconductor chip 9 satisfies the requirement of the transmission signal waveform defined by the template for the 25 Mb/s ATM-LAN physical layer described in the ATM_Forum/94-1008R5 and also meets the requirement of the zero-to-peak signal amplitude of about 2 V defined by the template for the transmission signal from the transformer 36 (46). This enables reduction in power consumption of the PMD semiconductor chip 9 to about 200 mW. The PMD semiconductor chip 9 is a circuit part that has the largest power consumption in the ATM-LAN adapter card 200. The calculation done by the inventors has shown that if the power consumption of the PMD semiconductor chip 9 can be suppressed to about 200 mW, the overall power consumption of the ATM-LAN adapter card 200 can be reduced to around 1 W.

Effects and Advantages of the Embodiment

The embodiment explained above has the following effects and advantages.

[1] By using a CMOS output circuit 21 of the output driver circuit 50, it is possible to reduce the on resistances of the MOS transistors making up the output circuit and lower the operating voltage of the internal circuits making up the PMD semiconductor chip 9, compared with the output circuit of



a type in which the NMOS transistors connected in series are push-pull operated.

[2] Even when the filter 35 (45) to satisfy the requirements of the transmission signal waveform defined by the template for the 25 Mb/s ATM-LAN physical layer described in the ATM_Forum/94-1008R5 is used and the resistors 33, 34 for adjusting the output impedance are provided, the signal amplitude defined by the template is produced with a lower power supply voltage of 3.3 volts than 5 volts by employing a CMOS output circuit comprising MOS transistors of small on resistances. In this way, using a CMOS output circuit 21 is best suited for lowering the operating voltage of the PMD semiconductor chip 9 applied to the 25 Mb/s ATM-LAN physical layer described in the ATM-LAN physical layer. This in turn makes it possible to easily produce the output signal amplitude that meets the template even when the turn ratio between the primary and secondary coils of the transformer 36 (46) is set at 1:1, so that there is no need to increase the number of turns of the secondary coil of the transformer by increasing the operating current flowing in the output circuit. In this respect, too, the employment of CMOS output circuit contributes to reducing the power consumption of the PMD semiconductor chip 9.

[3] In a state that the power supply to the PMD semiconductor chip 9 is cut off, the N-type well regions of the PMOS transistors Q1, Q3, Q5, Q7, Q9, Q11 making up the output stages of the output driver circuit 50 in the PMD



semiconductor chip 9 are not supplied with the power supply voltage Vdd and are floated. Because in the ATM-LAN, the transmitting circuits and the receiving circuits are connected through the transmission line in a one-to-one relationship, the drains of the PMOS transistors Q1, Q3, Q5, Q7, Q9, Q11 are not supplied with a high level of voltage through the transmission line 3 even when the N-type well regions are floated, so that a large current will not flow from the drains into the N-type well regions, eliminating the possibility of breakdown of the PMOS transistors Q1, Q3, Q5, Q7. On the other hand, when the CMOS type output driver circuit is applied to the Ethernet in which the output terminals of a plurality of output driver circuits are commonly connected to a single transmission line, the N-type well regions of the output driver circuit at a certain node, when they are floated, may be supplied with a high level of voltage as a result of output operation of other nodes, causing a large current to flow from the drains into the N-type well regions, damaging the PMOS transistors.

[4] As explained referring to Figs. 1, 14 and 16, by parallelly arranging two or more CMOS output stages 52, 51, 57 in the output driver circuit 50 of the ATM-LAN physical layer and slightly shifting the timings at which the output stages are driven from each other by the output control circuit 20, it is possible to lower the rate of change of current per unit time in the feed lines of power supply voltage Vdd and ground potential Vss. This in turn enables reduction in the power



supply noise in the power supply voltage Vdd feed line and the ground potential Vss feed line in the PMD semiconductor chip 9.

[5] As is obvious from the simulation conditions shown in Fig. 20 and the simulation results shown in Figs. 24(A), (B) and 24(C), the contrivance that the sizes of the MOS transistors forming the output stage turned on after the output stage turned on firstly are made larger than those of the firstly turned-on output stage can reduce the power supply noise.

[6] As shown in Fig. 16, in the second and third output stages 51, 57, by starting the turn-on of the MOS transistors that are to be turned on shortly after the turn-off of those MOS transistors that are to be turned off, the through-current flowing in the output stages 51, 57 can be reduced, further lowering the power consumption and power supply noise.

[7] As is apparent from the simulation results of Fig. 20, in the output circuit of Fig. 16 having three parallel output stages, the transistor size ratio between the first CMOS output stage 51, the second CMOS output stage 51, and the third CMOS output stage 57 is at around 1:2.5:6.25, the delay times of the delay circuits 80, 81 are at around 3 ns and the delay times of the delay circuits 82, 83 are at around 6 ns, making it possible to reduce the power supply noise to a very level.

[8] Because the PMD semiconductor chip 9 satisfies, with the operating voltage of 3.3 volts, the requirements of the



transmission signal waveform defined by the template for the 25 Mb/s ATM-LAN physical layer described in the ATM_Forum/94-1008R5, the power consumption of the PMD semiconductor chip 9 can be reduced to about 200 mW. The PMD semiconductor chip 9 is a circuit component that consumes the largest power in the ATM-LAN adapter card 200, so that if the power consumption of the PMD semiconductor chip 9 can be suppressed to about 200 mW, the overall power consumption of the ATM-LAN adapter card 200 can be lowered to about 1 W.

The embodiments of the present invention accomplished by the inventor have been described. It should be noted that the present invention is not limited to these embodiments and that a variety of modifications may be made without departing from the spirit of the invention.

For example, in the parallel two-stage output circuit of Fig. 1, the turn-on of the MOS transistors to be turned on can be also started after the turn-off of the MOS transistors to be turned off has been started, as in the case of Fig. 16. The output driver circuit may be constructed of one CMOS output stage. In the single CMOS output stage configuration, too, the turn-on operation of the constitutional MOS transistors can be delayed from the turn-off operation of other MOS transistors.

Although the invention made by the inventor has been explained, taking the case in which the invention is adapted to 25 Mb/s ATM-LAN physical layer described in the ATM_Forum/94-1008R5 that is a field of application which is



the background of this invention, it should be noted that this invention is not limited to this application but can also be applied to other ATM-LAN specifications which will be standardized in the future. The present invention can be applied to at least a case where the output stages of the ATM-LAN output driver circuit are constructed of CMOS transistors.

EFFECTS OF THE INVENTION

Effects brought about by representative examples of the present inventions disclosed in the present invention will be briefly summarized below.

Because the transmitting circuits and the receiving circuits are connected in a one-to-one relationship via the transmission line, and because in the output driver circuit (50) of the transmitting circuit (10) the output stage of its output circuit (21) is formed of CMOS transistors, the gate-source voltages of the P-channel MOS transistors included in the CMOS output stage and connected to the power supply voltage side do not depend on the voltage of the transmission terminal but can virtually be set at the power supply voltage level. This makes it possible to reduce the on resistance of the MOS transistors (Q1, Q3, Q5, Q7, Q9, Q11) on the power supply voltage side that make up the output circuit, compared with the output circuit of a type such that the series connected NMOS transistors are push-pull operated. Hence, the operating voltage of the output driver circuit can be reduced, and the operating voltage of the internal circuits making up



such a semiconductor integrated circuit chip 9 which is used for ATM-LAN physical layer control and includes the output driver circuit can be lowered.

As described above, even when a filter 35 (45) is used that satisfies the requirement of transmission signal waveform defined by a template for the 25 Mb/s ATM-LAN physical layer described in the ATM_Forum/94-1008R5 and output impedance adjusting resistors (33, 34) are incorporated, it is possible to obtain a signal amplitude defined by the template with a relatively low power supply voltage of 3.3 volts by employing a CMOS output circuit (21) to lower the on resistances of the MOS transistors.

Employment of the CMOS output circuit (21) is best suited for lowering the operating voltage of the semiconductor integrated circuit chip (9) applied to the 25 Mb/s ATM-LAN physical layer described in the ATM_Forum/94-1008R5. This makes it possible to easily produce an output signal amplitude that meets the template even when the turn ratio between the primary and the secondary coil of the transformer (36) is 1:1. Hence, there is no need to increase the number of turns of the secondary coil of the transformer (36) even by increasing the operating current flowing through the output circuit. This contributes to lowering the power consumption of the semiconductor integrated circuit chip (9) for the ATM-LAN physical layer.

Unlike the Ethernet, the ATM-LAN has the transmitting circuit and the receiving circuit connected in one-to-one



correspondence to the transmission line, so that even when the N-type well regions of the CMOS output stages are floated, the drains of the PMOS transistors of the CMOS output stages (Q1, Q3, Q5, Q7, Q9, Q11) are not supplied with a high level of voltage through the transmission line (3, 4) and no large current flows from the drains into the N-type well regions, eliminating the possibility of breakdown of the PMOS transistors (Q1, Q3, Q5, Q7, Q9, Q11).

Because of their properties of the output circuit, the MOS transistors making up the CMOS output stages of the output driver circuit (50) are given a relatively large current supply capability (transistor size). At the same time, two or more CMOS output stages each comprising first and second pairs of CMOS transistors are arranged parallelly and a first timing control means (54) for shifting the timings of the push-pull operation of these stages is used in the output control circuit (20). This arrangement reduces the rate of change of current per unit time in the power supply voltage Vdd line and the ground potential Vss supply line to the CMOS output stages, which in turn lowers the power supply noise.

By incorporating in the output control circuit (20) second timing control means (80, 81, 82, 83) that delay the timing of the turn-on of the MOS transistors making up the CMOS output stages from the timings of the turn-off, it is possible to reduce the through-current flowing in the CMOS output stages during the transient response. This in turn



contributes to the reduction in the power supply noise and power consumption.

When three CMOS output stages are arranged in parallel, the transistor size ratio between the MOS transistors making up the first CMOS output stage (52), the MOS transistors making up the second CMOS output stage (51) and the MOS transistors making up the third CMOS output stage (57) is 1:2.5:6.25. Delay means (80, 81, 82, 83) are provided in the output control circuit (20) to delay the timings of the turn-on of the MOS transistors included in the second CMOS output stage and the turn-on of the MOS transistors included in the third CMOS output stage from the timing of the turn-on of the MOS transistors included in the first CMOS output stage by about 3 ns and 6 ns, respectively. This enables significant reduction in the power supply noise.

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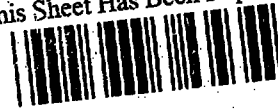
WHAT IS CLAIMED IS:

1. A transmission line drive circuit for an ATM-LAN physical layer that is connected one-to-one to a receiving circuit through a transmission line, comprising:
 - an output driver circuit having a pair of transmission terminals;
 - output impedance adjusting resistors connected to the respective paired transmission terminals;
 - a filter connected in series to the resistors; and
 - a transformer having a primary side thereof connected to an output terminal of the filter and a secondary side thereof connected to the transmission line;wherein the output driver circuit includes an output circuit and an output control circuit, the output circuit includes a CMOS output stage comprising a first and a second pair which are each comprised of a P-channel MOS transistor and an N-channel MOS transistor connected in series, the P-channel MOS transistors of the first and second pairs have their sources connected to a line from a power supply voltage different than a ground potential, the N-channel MOS transistors of the first and second pairs have their sources connected to a line for the ground potential, the MOS transistors forming the first pair have a common drain connected to one of the transmission terminals, and the MOS transistors forming the second pair have a common drain connected to the other transmission terminal;





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wherein the output control circuit uses the power supply voltage and the ground potential as operating voltages thereof and causes the first and second pairs of the CMOS output stage to perform a push-pull operation in phase opposition.

2. A transmission line drive circuit according to claim 1, wherein the output circuit has two or more parallelly-connected CMOS output stages each having the first and second pairs and the output control circuit has a first timing control means that shifts the timings of push-pull operations of the parallelly-connected CMOS output stages.

3. A transmission line drive circuit according to claim 1, wherein the output control circuit has a second timing control means that delays the start of a turn-on operation of the P-channel and N-channel MOS transistors of the first and second pairs.

4. A transmission line drive circuit according to claim 1, wherein the transformer has an inductance of 1 mH or higher, a series resistance of 5 ohm or less, a coupling factor of 0.999 or higher, an equivalent capacitance of 5 pF or lower, and a frequency band of from 12 KHz to about 16 MHz.

5. A transmission line drive circuit according to claim 1, wherein the turn ratio of the primary and secondary sides of the transformer is 1 : 1.



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6. A transmission line drive circuit according to claim 1, wherein the supply voltage of the output driver circuit is 3.3 volt.

7. An output driver circuit for an ATM-LAN physical layer connected one-to-one to a receiving circuit through a transmission line, comprising:

an output circuit; and

an output control circuit;

wherein the output circuit includes a plurality of CMOS output stages each comprising a first and a second pair of a P-channel MOS transistor and an N-channel MOS transistor connected in series, the P-channel MOS transistors in each stage have their sources connected to a line for a power supply voltage different from a ground potential, the N-channel MOS transistors in each stage have their sources connected to a line for a ground potential, the MOS transistors in each stage forming the first pair have a common drain connected to a first transmission terminal, and the MOS transistors in each stage forming the second pair have a common drain connected to a second transmission terminal;

wherein the output control circuit uses the power supply voltage and the ground potential as operating voltages, causing the first and second pairs of each CMOS output stage to perform a push-pull operation in phase opposition, and shifting the timings of the push-pull operations of the plurality of CMOS output stages from each other.



8. An output driver circuit for an ATM-LAN physical layer connected one-to-one to a receiving circuit through a transmission line, comprising:

an output circuit; and

an output control circuit;

wherein the output circuit includes a plurality of CMOS output stages each comprising a first and a second pair of a P-channel MOS transistor and an N- channel MOS transistor connected in series, the P-channel MOS transistors in each stage have their sources connected to a line for a power supply voltage different from a ground potential, the N-channel MOS transistors in each stage have their sources connected to a line for the ground potential, the MOS transistors in each stage forming the first pair have a common drain connected to a first transmission terminal, and the MOS transistors in each stage forming the second pair have a common drain connected to a second transmission terminal;

wherein the output control circuit uses the power supply voltage and the ground potential as operating voltages thereof, causing the first and second pairs of each CMOS output stage to perform a push-pull operation in phase opposition, and delaying the start of a turn-on operation of the MOS transistors in a predetermined CMOS output stage.

9. An output driver circuit according to claim 8, wherein the output circuit includes first, second and third parallelly-connected CMOS output stages each comprising the





first and second pairs, and the output control circuit includes a first delay means and a second delay means, the first delay means delaying the start of the turn-on operation of the MOS transistors included in the second CMOS output stage from the start of the turn-on operation of the MOS transistor included in the first CMOS output stage by a first length of time, the second delay means delaying the start of the turn-on operation of the MOS transistors included in the third CMOS output stage from the start of the turn-on operation of the MOS transistors included in the second CMOS output stage by a second length of time.

10. An output driver circuit according to claim 8, wherein the output circuit includes first, second and third parallelly connected CMOS output stages each comprising the first and second pairs, wherein the ratio between the size of the MOS transistors forming the first CMOS output stage, the size of the MOS transistors forming the second CMOS output stage and the size of the MOS transistors forming the third CMOS output stage is approximately 1:2.5:6.25, and wherein the output control circuit includes a delay means that delays the start of the turn-on operation of the MOS transistors included in the second CMOS output stage and the start of the turn-on operation of the MOS transistors included in the third CMOS output stage from the start of the turn-on operation of the MOS transistors included in the first CMOS output stage by about 3 ns and about 6 ns, respectively.





11. An ATM-LAN integrated circuit adapter card which is installed in a terminal device, connected to a transmission line and performs an ATM-LAN interface control between the terminal device and another terminal device connected to the first terminal device through the transmission line, comprising:

an ATM-LAN physical layer control chip having a transmitting circuit and a receiving circuit for the ATM-LAN physical layer;

resistors for adjusting the output impedance of the transmitting circuit;

a filter connected in series to the resistors for shaping the transmitted signal waveform;

a transmission coupling transformer for transmitting the output of the filter to the transmission line;

a reception coupling transformer for transmitting the received signal from the transmission line to the receiving circuit; and

a control means for performing transmission and reception protocol processing for the ATM-LAN,

wherein the control chip, the resistors, the filter, the transformers and the control means are all formed on a card substrate;

wherein the transmitting circuit in the ATM-LAN physical layer control chip includes an output driver circuit having a pair of transmission terminals connected to the resistors;





wherein the output driver circuit includes an output circuit and an output control circuit;

wherein the output circuit includes a CMOS output stage comprising a first and a second pair each comprised of a P-channel MOS transistor and an N-channel MOS transistor connected in series, the P-channel MOS transistors have their sources connected to a line for a power supply voltage different from a ground potential, the N-channel MOS transistors of the first and second pairs have their sources connected to a line for the ground potential, the MOS transistors forming the first pair have a common drain connected to one of the transmission terminals, and the MOS transistors forming the second pair have a common drain connected to the other transmission terminal;

wherein the output control circuit uses the power supply voltage and the ground potential as operating voltages thereof and causes the first and second pairs of the CMOS output stage to perform a push-pull operation in phase opposition.

12. An ATM-LAN integrated circuit adapter card which is installed in a terminal device, connected to a transmission line and performs an ATM-LAN interface control between the terminal device and another terminal device connected to the first terminal device through the transmission line, comprising:

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an ATM-LAN physical layer control chip having a transmitting circuit and a receiving circuit for the ATM-LAN physical layer;

resistors for adjusting the output impedance of the transmitting circuit;

a filter connected in series to the resistors for shaping the transmitted signal waveform;

a transmission coupling transformer for transmitting the output of the filter to the transmission line;

a reception coupling transformer for transmitting the received signal from the transmission line to the receiving circuit; and

a control means for performing transmission and reception protocol processing for the ATM-LAN;

wherein the control chip, the resistors, the filter, the transformers and the control means are all formed on a card substrate;

wherein the transmitting circuit in the ATM-LAN physical layer control chip includes an output driver circuit having a pair of transmission terminals connected to the resistors;

wherein the output driver circuit includes an output circuit and an output control circuit;

wherein the output circuit includes a plurality of CMOS output stages each comprising a first and a second pair of a P-channel MOS transistor and an N-channel MOS transistor connected in series, the P-channel MOS transistors in each stage have their sources connected to a line for a power



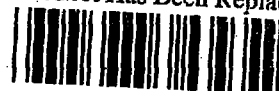


supply voltage different from a ground potential, the N-channel MOS transistors in each stage have their sources connected to a line for the ground potential, the MOS transistors in each stage forming the first pair have a common drain connected to one of the transmission terminals, and the MOS transistors in each stage forming the second pair have a common drain connected to the other transmission terminal;

wherein the output control circuit uses the power supply voltage and the ground potential as operating voltages, causing the first and second pairs in each CMOS output stage to perform a push-pull operation in phase opposition, shifting the timings of the push-pull operations of the CMOS output stages from each other, and delaying the start of a turn-on operation of the MOS transistors in a predetermined CMOS output stage.

13. A transmission line drive circuit according to claim 3, wherein the second timing control means includes means to reduce the delay of the turn-off operation of the MOS transistors of the first and second pairs to turn off the MOS transistors relatively early.

14. An output driver circuit according to claim 8, wherein the output control circuit reduces the delay of the turn-off operation of the MOS transistors in the predetermined CMOS output to turn off the MOS transistors relatively early.





15. An ATM-LAN integrated circuit adapter card according to claim 12, wherein the output control circuit reduces the delay of the turn-off operation of the MOS transistors in the predetermined CMOS output to turn off the MOS transistors relatively early.

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