

CLAIMS

What is claimed is:

1. An electronic package, comprising:
 - a mold layer having a first surface and a second surface opposite the first surface;
 - a plurality of first dies embedded in the mold layer, wherein each of the plurality of first dies has a surface that is substantially coplanar with the first surface of the mold layer; ~~and~~
 - a second die embedded in the mold layer, wherein the second die is positioned between the plurality of first dies and the second surface of the mold layer; and
a plurality of high speed input/out (HSIO) dies embedded in the mold layer, wherein the plurality of HSIO dies are electrically coupled to the second die.
2. The electronic package of claim 1, wherein the plurality of first dies are electrically coupled to the second die with first level interconnects (FLI).
3. The electronic package of claim 2, wherein active surfaces of the plurality of first dies are oriented to be facing an active surface of the second die.
4. The electronic package of claim 1, wherein the plurality of first dies comprise dies fabricated at a first process node, and wherein the second die is fabricated at a second process node that is less advanced than the first process node.
5. ~~The electronic package of claim 1, further comprising:~~
~~a plurality of high speed input/out (HSIO) dies embedded in the mold layer.~~

~~6.~~ The electronic package of claim ~~5~~, wherein the plurality of HSIO dies are electrically coupled to the second die.

~~75.~~ The electronic package of any one of claims ~~51 to 4~~, wherein each of the plurality of HSIO dies has a surface that is substantially coplanar with the first surface of the mold layer.

~~86.~~ The electronic package of claim 1, further comprising:
a plurality of second dies.

~~97.~~ The electronic package of claim ~~86~~, wherein the plurality of second dies are electrically coupled to each other by a bridge embedded in the mold layer.

~~108.~~ The electronic package of claim ~~97~~, wherein the plurality of second dies is positioned between the bridge and the plurality of first dies.

~~119.~~ The electronic package of claim 1, further comprising:
mid-level interconnects (MLIs) extending from the second surface of the mold layer.

~~1210.~~ The electronic package of claim ~~119~~, wherein the MLIs are electrically coupled to the plurality of first dies and the second die by conductive pillars and pads embedded in the mold layer.

~~13~~11. An electronic package, comprising:

a mold layer having a first surface and a second surface opposite the first surface;

a plurality of first dies embedded in the mold layer;

a second die embedded in the mold layer, wherein the second die is positioned between the plurality of first dies and the second surface of the mold layer; ~~and~~

a solder resist layer between the plurality of first dies and the second die; ~~and~~

~~_____ a plurality of high speed input/out (HSIO) dies electrically coupled to the second die.~~

~~14~~12. The electronic package of claim ~~13~~11, wherein each of the plurality of first dies is entirely embedded in the mold layer.

~~15. The electronic package of claim 13, further comprising:~~

~~_____ a plurality of high speed input/out (HSIO) dies electrically coupled to the second die.~~

~~16~~13. The electronic package of claim ~~15~~11 or 12, wherein the plurality of HSIO dies have a first thickness and the plurality of first dies have a second thickness that is different than the first thickness.

~~17~~14. The electronic package of claim ~~13~~11, wherein the plurality of first dies are fabricated at a first process node, and wherein the second die is fabricated at a second process node that is less advanced than the first process node.

~~18~~15. The electronic package of claim ~~13~~11, further comprising:

a plurality of second dies, wherein each of the second dies are electrically coupled to each other by one or more bridges embedded in the mold layer.

~~19~~16. A method of fabricating an electronic package, comprising:

placing a plurality of first dies on a carrier;

disposing a first mold layer over the plurality of first dies, wherein contact pads of the first dies are exposed;

attaching a second die to the plurality of first dies with first level interconnects (FLIs);

and

disposing a second mold layer over the second die.

~~20~~17. The method of claim 19, wherein the first dies are placed on the carrier with a die mounter, and wherein the second die is attached to the plurality of first dies with a thermal compression bonding (TCB) tool.

~~21~~18. The method of claim 19, further comprising:

fabricating a redistribution layer above the second die;

disposing a solder resist over the redistribution layer;

forming openings in the solder resist;

disposing mid-level interconnects (MLIs) in the openings; and

removing the carrier.

2219. An electronic system, comprising:

a board;

a multi-die package coupled to the board, wherein the multi-die package comprises:

a mold layer having a first surface and a second surface;

a plurality of first dies, wherein the plurality of first dies are embedded in the mold layer; and

a second die coupled to the plurality of first dies, wherein active surfaces of the first dies face an active surface of the second die, wherein the second die is embedded in the mold layer, and wherein the second die is between the active surface of the first dies and the second surface of the mold layer; and

a plurality of high speed input/out (HSIO) dies embedded in the mold layer, wherein the plurality of HSIO dies are electrically coupled to the second die.

2320. The electronic system of claim 2219, wherein the plurality of first dies are first process node dies, and wherein the second die is a second process node die, wherein the first process node is more advanced than the second process node.

~~24. The electronic system of claim 22, further comprising:~~

~~a plurality of high speed input/out (HSIO) dies embedded in the mold layer.~~

~~25. The electronic system of claim 24, wherein the plurality of HSIO dies are electrically coupled to the second die.~~

26. — ~~A multi-die electronic package, comprising:~~

~~————— a first die in a first mold layer, the first die comprising interconnections;~~

~~————— a first plurality of vias in the first mold layer, the first plurality of vias laterally adjacent to a first side of the first die, each of the first plurality of vias extending from a top surface of the first mold layer to a bottom surface of the first mold layer;~~

~~————— a second plurality of vias in the first mold layer, the second plurality of vias laterally adjacent to a second side of the first die, each of the second plurality of vias extending from the top surface of the first mold layer to the bottom surface of the first mold layer;~~

~~————— a second die electrically coupled to the first die, and the second die electrically coupled to the first plurality of vias;~~

~~————— a third die electrically coupled to the first die, the third die electrically coupled to the second die by the interconnections of the first die; and~~

~~————— a second mold layer between and in contact with the second die and the third die, the second mold layer having an upper surface co-planar with an upper surface of the second die, the second mold layer between the second die and the first die, and the second mold layer between the third die and the first die.~~

27. — ~~The multi-die electronic package of claim 26, wherein the upper surface of the second mold layer is co-planar with an upper surface of the third die.~~

28. — ~~The multi-die electronic package of claim 26, wherein the second die is electrically coupled to the third die by an electrical pathway directly between the third die and the second die.~~

29. ~~The multi-die electronic package of claim 26, wherein the third die is co-planar with the second die.~~

30. ~~The multi-die electronic package of claim 26, further comprising:~~

~~————— a fourth die between the second die and the third die, the fourth die coupled to the first die.~~

31. ~~The multi-die electronic package of claim 26, further comprising:~~

~~————— a plurality of mid-level interconnects vertically beneath the first die.~~

32. ~~The multi-die electronic package of claim 31, further comprising:~~

~~————— a solder resist beneath the first die, wherein the plurality of mid-level interconnects is in the solder resist.~~

33. ~~A multi-die electronic package, comprising:~~

~~————— a first die in a first mold layer, the first die comprising interconnections;~~

~~————— a first via in the first mold layer, the first via laterally adjacent to a first side of the first die, and the first via extending from a top surface of the first mold layer to a bottom surface of the first mold layer;~~

~~————— a second via in the first mold layer, the second via laterally adjacent to a second side of the first die, and the second via extending from the top surface of the first mold layer to the bottom surface of the first mold layer;~~

~~_____ a second die electrically coupled to the first die, and the second die electrically coupled to the first via;~~

~~_____ a third die electrically coupled to the first die, the third die electrically coupled to the second die by the interconnections of the first die; and~~

~~_____ a second mold layer between and in contact with the second die and the third die, the second mold layer having a surface co-planar with a surface of the second die, the second mold layer between the second die and the first die, and the second mold layer between the third die and the first die.~~

~~34. The multi die electronic package of claim 33, wherein the surface of the second mold layer is co-planar with a surface of the third die.~~

~~35. The multi die electronic package of claim 33, wherein the second die is electrically coupled to the third die by an electrical pathway directly between the third die and the second die.~~

~~36. The multi die electronic package of claim 33, wherein the third die is co-planar with the second die.~~

~~37. The multi die electronic package of claim 33, further comprising:~~

~~_____ a fourth die between the second die and the third die, the fourth die coupled to the first die.~~

~~38. The multi-die electronic package of claim 33, further comprising:~~

~~————— a plurality of mid-level interconnects vertically beneath the first die.~~

~~39. The multi-die electronic package of claim 38, further comprising:~~

~~————— a solder resist beneath the first die, wherein the plurality of mid-level interconnects is in the solder resist.~~

~~40. A multi-die electronic package, comprising:~~

~~————— a first die in a first mold layer, the first die comprising interconnections;~~

~~————— a first plurality of vias in the first mold layer, the first plurality of vias laterally adjacent to a first side of the first die, each of the first plurality of vias extending from a first surface of the first mold layer to a second surface of the first mold layer;~~

~~————— a second plurality of vias in the first mold layer, the second plurality of vias laterally adjacent to a second side of the first die, each of the second plurality of vias extending from the first surface of the first mold layer to the second surface of the first mold layer;~~

~~————— a second die electrically coupled to the first die, and the second die electrically coupled to the first plurality of vias;~~

~~————— a third die electrically coupled to the first die, the third die electrically coupled to the second die by the interconnections of the first die; and~~

~~————— a second mold layer between and in contact with the second die and the third die, the second mold layer having a surface co-planar with a surface of the second die, the second mold layer between the second die and the first die, and the second mold layer between the third die and the first die.~~

~~41. The multi die electronic package of claim 40, wherein the second die is electrically coupled to the third die by an electrical pathway directly between the third die and the second die.~~

~~42. The multi die electronic package of claim 40, wherein the third die is co-planar with the second die.~~

~~43. The multi die electronic package of claim 40, further comprising:
a fourth die between the second die and the third die, the fourth die coupled to the first die.~~

~~44. The multi die electronic package of claim 40, further comprising:
a plurality of mid-level interconnects proximate a surface of the first die opposite the second die and the third die.~~

~~45. The multi die electronic package of claim 44, further comprising:
a solder resist proximate the surface of the first die opposite the second die and the third die, wherein the plurality of mid-level interconnects is in the solder resist.~~