CLAIMS

1. A method of fabricating a semiconductor structure including at least one resistive memory cell, the method comprising:

forming a dielectric layer on inner sidewalls of a cell contact hole above a cavity in a semiconductor structure, wherein a seam is formed in the dielectric layer between the inner sidewalls of the cell contact hole;

forming a bottom electrode within a portion of the cavity, the bottom electrode in contact with a top surface of a target electrical contact and with a bottom surface of the dielectric layer and a bottom surface of the seam; and

forming a top electrode over the dielectric layer and in direct contact with a top surface of the dielectric layer and a top surface of the seam.

2. The method of claim 1, further comprising:

forming a sacrificial layer on, and in contact with, the target electrical contact;

forming a second dielectric layer over, and in contact with, the sacrificial layer;

forming the cell contact hole through the second dielectric layer and exposing a first portion of the sacrificial layer;

forming an access contact hole through the second dielectric layer and exposing a second portion of the sacrificial layer; and

removing remaining portions of the sacrificial layer thereby forming the cavity directly connecting a bottom opening of the cell contact hole and a bottom opening of the access contact hole.

3. The method of claim 1, wherein the dielectric layer is formed by atomic layer deposition of dielectric material on the inner sidewalls of the cell contact hole above the cavity, and wherein the seam in the dielectric layer is formed by the atomic layer deposition of the dielectric material.

4. The method of claim 1, wherein the seam is formed vertically oriented and located proximate to a center region of the dielectric layer between the inner sidewalls of the cell contact hole above the cavity.

5. The method of claim 1, wherein the dielectric layer comprises at least one material selected from the following set of materials consisting of:

metal oxide, non-conductive metal nitride, Silicon Oxide, Silicon Dioxide (SiO_2), Silicon Nitride (SiN), Silicon Oxy-Nitride, Silicon Oxycarbonitride (SiOCN), Carbon-Doped Silicon Nitride (SiCN), or Silicon-Boron-Carbon Nitride (SiBCN), or any combination of aforementioned materials.

6. The method of claim 1, wherein the dielectric layer comprises at least one material selected from a set of materials consisting of:

metal oxide, non-conductive metal nitride, Aluminum (Al), Hafnium (Hf), Zirconium (Zr), Titanium (Ti), Silicon (Si), Germanium (Ge), Copper (Cu), or Lanthanum (La).

7. The method of claim 1, further comprising:

doping the seam with at least one of a mobile element or a non-stoichiometric compound by adding reactive elements.

8. The method of claim 1, further comprising:

doping the seam with a conductive material selected from a set of conductive materials consisting of: Copper (Cu), Titanium (Ti), Aluminum (Al), Hafnium (Hf), or Lanthanum (La).

9. The method of claim 1, wherein the seam comprises a conductive filament extending from the top electrode to the bottom electrode.

10. The method of claim 1, wherein the top electrode, the dielectric layer, the seam comprising a conductive filament, the bottom electrode, and the target electrical contact, collectively form a resistive memory cell in a semiconductor structure fabricated according to the method.

11. The method of claim 1, wherein at least one of the top electrode or the bottom electrode, comprises a conductive material selected from a set of conductive materials consisting of: Copper (Cu), Cobalt (Co), Aluminum (Al), Tungsten (W), Titanium (Ti), Tantalum (Ta), Ruthenium (Ru), Hafnium (Hf), Zirconium (Zr), Nickel (Ni), Platinum (Pt), Tin (Sn), Silver (Ag), Gold (Au), a conducting metallic compound material, or a conducting metal alloy including at least one preceding conductive material.

12. A method of fabricating a semiconductor structure including at least one resistive memory cell, the method comprising:

providing a semiconductor material stack including:

a substrate;

a gate stack including a gate metal contact;

a first source-drain stack including a first source/drain metal contact; and

a second source-drain stack including a second source/drain metal contact, the substrate supporting the gate stack and the first and second source-drain stacks;

performing deposition of an amorphous silicon (a-Si) layer directly on, and contacting, a top surface of a target metal contact, the target metal contact being electrically connected to at least one of

the first source/drain metal contact, or

the second source/drain metal contact;

performing deposition of an inter-layer dielectric (ILD) layer directly on, and contacting, a top surface of the a-Si layer;

performing vertical directional etching in the ILD layer from a top surface thereof downward to at least a bottom surface thereof forming a vertical cell contact hole in the ILD layer exposing the a-Si layer in the vertical cell contact hole;

performing vertical directional etching in the ILD layer from a top surface thereof downward to at least a bottom surface thereof forming a vertical access contact hole in the ILD layer and exposing the a-Si layer in the vertical access contact hole, the vertical access contact hole being located horizontally proximate to the vertical cell contact hole;

performing isotropic etching removing the a-Si layer leaving a void space therefor;

performing atomic layer deposition of dielectric material filling the vertical cell contact hole in the ILD layer and forming a vertical seam near a center of a vertical memory cell formed in the vertical cell contact hole;

performing deposition of conductive material in the vertical access contact hole filling the vertical access contact hole and the void space forming a bottom electrode of the vertical memory cell directly on, and contacting, a top surface of the target metal contact, and contacting a bottom surface of the vertical memory cell and the vertical seam; and

performing deposition of conductive material on, and contacting, a top surface of the vertical memory cell and the vertical seam, forming a top electrode of the vertical memory cell.

13. The method of claim 12, further comprising:

doping the vertical seam with a conductive material selected from a set of conductive materials consisting of: Copper (Cu), Titanium (Ti), Aluminum (Al), Hafnium (Hf), or Lanthanum (La).