

WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a first device layer including a plurality of first semiconductor devices, a first cover insulating layer, and a plurality of first through-electrodes passing through at least a portion of the first device layer;

a second device layer including a plurality of second semiconductor devices, a second cover insulating layer, and a plurality of second through-electrodes passing through at least a portion of the second device layer, the plurality of second semiconductor devices vertically overlapping the plurality of first semiconductor devices, respectively, the second cover insulating layer in contact with the first cover insulating layer;

a third device layer including an upper semiconductor chip, the upper semiconductor chip vertically overlapping at least two of the plurality of first semiconductor devices and vertically overlapping at least two of the plurality of second semiconductor devices; and

a plurality of device bonded pads passing through the first cover insulating layer and the second cover insulating layer, the plurality of device bonded pads electrically connecting the plurality of first through-electrodes and the plurality of second through-electrodes to the upper semiconductor chip,

wherein each of the plurality of device bonded pads is a diffusion-bonded integral structure of two sub-structures.

2. The semiconductor package of claim 1, wherein

the first device layer comprises a first semiconductor substrate including a plurality of first semiconductor chip regions and one or more first scribe lane regions, the plurality of first semiconductor chip regions spaced apart from one another with the one or more first scribe lane regions therebetween, the first semiconductor substrate including an active surface on which the plurality of first semiconductor devices are located, and

the first cover insulating layer covers the active surface of the first semiconductor substrate.

3. The semiconductor package of claim 2, wherein

the second device layer comprises a second semiconductor substrate including, a plurality of second semiconductor chip regions and one or more second scribe lane regions, the plurality of second semiconductor chip regions spaced apart from one another with the one or more second scribe lane regions therebetween, the second semiconductor substrate including an active surface on which the plurality of second semiconductor devices are located, and

the second cover insulating layer covers the active surface of the second semiconductor substrate.

4. The semiconductor package of claim 3, wherein

the upper semiconductor chip comprises,

a third semiconductor substrate having an active surface on which a third semiconductor device is located, and

a chip cover insulating layer covering the active surface of the third semiconductor substrate, and

the semiconductor package further comprises,

a third cover insulating layer covering a surface of the second semiconductor substrate facing the third device layer and contacting the chip cover insulating layer, and

a plurality of chip bonded pads passing through the third cover insulating layer and the chip cover insulating layer and electrically connecting the third semiconductor device to the plurality of second through-electrodes.

5. The semiconductor package of claim 4, wherein the second semiconductor substrate has a recess on a surface facing the third device layer, and the upper semiconductor chip is attached to a protrusion of the second semiconductor substrate defined by the recess of the second semiconductor substrate.

6. The semiconductor package of claim 2, wherein the second device layer comprises a plurality of lower semiconductor chips and a filling molding member, the plurality of lower semiconductor chips spaced apart from one another with the filling molding member therebetween, each of the plurality of lower semiconductor chips including a second semiconductor substrate having an active surface on which the plurality of second semiconductor devices are located and a second cover insulating layer covering the active surface of the second semiconductor substrate.

7. The semiconductor package of claim 6, wherein

the filling molding member has a through-hole accommodating a through-mold via connected to the upper semiconductor chip, and

the semiconductor package further comprises an additional through-electrode that is in a corresponding one of the one or more first scribe lane regions, passes through the first semiconductor substrate, and is connected to the through-mold via.

8. The semiconductor package of claim 7, wherein the first semiconductor substrate further includes a plurality of interposer regions each provided between a pair of the one or more first scribe lane regions, the each of the plurality of interposer regions including an additional connection pad connecting the through-mold via to the additional through-electrode.

9. The semiconductor package of claim 6, wherein

the first semiconductor substrate further comprises at least two interposer regions spaced apart from each other with at least one corresponding first scribe lane of the one or more first scribe lane regions therebetween,

the filling molding member has a plurality of through-holes in the at least two interposer regions accommodating a plurality of through-mold vias connected to the upper semiconductor chip, and

the at least two interposer regions comprises a plurality of additional through-electrodes passing through the first semiconductor substrate and connected to the plurality of through-mold vias.

10. The semiconductor package of any one of claims 6 to 9, wherein the first semiconductor substrate has a recess on a surface facing the second device layer, and

the plurality of lower semiconductor chips are attached to a protrusion of the first semiconductor substrate defined by the recess of the first semiconductor substrate.

11. The semiconductor package of any one of claims 1 to 10, further comprising: a rewiring structure on a first surface of the first device layer, the first surface of the first device layer being opposite to a second surface of the first device layer that faces the second device layer, the rewiring structure including,

a plurality of rewiring insulating layers,

a plurality of rewiring conductive patterns each on one of top surfaces or bottom surfaces of one of the plurality of rewiring insulating layers, and

a plurality of rewiring via patterns each connecting a vertically neighboring pair of the plurality of rewiring conductive patterns and passing through at least one of the plurality of rewiring insulating layers,

wherein the plurality of rewiring conductive patterns and the plurality of rewiring via patterns are electrically connected to the plurality of first through-electrodes.

12. A semiconductor package comprising:

a first device layer including,

a first semiconductor substrate having an active surface, the first semiconductor substrate including,

one or more first scribe lane regions, and

a plurality of first semiconductor chip regions spaced apart from one another with the one or more first scribe lane regions therebetween, each of the plurality of first semiconductor chip regions provided with a first semiconductor device on the active surface of the first semiconductor substrate, a plurality of first through-electrodes in the plurality of first semiconductor chip regions and passing through the first semiconductor substrate, and

a first cover insulating layer covering the active surface of the first semiconductor substrate;

a second device layer including,

a second semiconductor substrate including an active surface, the second semiconductor substrate including,

one or more second scribe lane regions, and

a plurality of second semiconductor chip regions spaced apart from one another with the one or more second scribe lane regions therebetween, each of the plurality of second semiconductor chip regions provided with a second semiconductor device on the active surface of the second semiconductor

substrate, the second semiconductor device being of a same type as the first semiconductor device,

a plurality of second through-electrodes in the plurality of second semiconductor chip regions and passing through the second semiconductor substrate, and

a second cover insulating layer covering the active surface of the second semiconductor substrate and in contact with the first cover insulating layer;

a third device layer including an upper semiconductor chip, the upper semiconductor chip being on the second device layer and electrically connected to the plurality of second through-electrodes; and

a plurality of device bonded pads passing through the first cover insulating layer and the second cover insulating layer and electrically connecting the first device layer to the second device layer,

wherein each of the plurality of device bonded pads is a diffusion-bonded integral structure of two sub-structures.

13. The semiconductor package of claim 12, wherein

the upper semiconductor chip includes a plurality of chip connection pads, and the semiconductor package further includes,

a plurality of upper connection pads on a first surface of the second semiconductor substrate, the first surface of the second semiconductor substrate being opposite to a second surface of the second semiconductor substrate that faces the first

device layer, and the plurality of upper connection pads connected to corresponding ones of the plurality of second through-electrodes,

a plurality of chip connection terminals between the plurality of chip connection pads and corresponding ones of the plurality of upper connection pads, and

an encapsulation member on the second semiconductor substrate and surrounding a side surface of the upper semiconductor chip.

14. The semiconductor package of claim 12 or claim 13, wherein

the first semiconductor substrate further includes first residual scribe lane regions that surrounds the plurality of first semiconductor chip regions at edges of the first semiconductor substrate,

the second semiconductor substrate further includes second residual scribe lane regions that surrounds the plurality of second semiconductor chip regions at edges of the second semiconductor substrate, and

each of the one or more first scribe lane regions and the one or more second scribe lane regions has a first width, and each of the first residual scribe lane regions and the second residual scribe lane region has a second width, the second width is less than the first width.

15. The semiconductor package of any one of claims 12 to 14, further comprising:

a first additional through-electrode in a corresponding one of the one or more first scribe lane regions and passing through the first semiconductor substrate;

a second additional through-electrode in a corresponding one of the one or more second scribe lane regions, passing through the second semiconductor substrate, and electrically connected to the upper semiconductor chip; and

an additional bonded pad passing through the first cover insulating layer and the second cover insulating layer and electrically connecting the first additional through-electrode to the second additional through-electrode.

16. The semiconductor package of claim 15, wherein each of the additional bonded pad is a diffusion-bonded integral structure of two sub-structures.

17. The semiconductor package of any one of claims 12 to 16, wherein
the first semiconductor substrate further includes a first interposer region spaced apart from a corresponding one of the plurality of first semiconductor chip regions with a corresponding one of the one or more first scribe lane regions interposed therebetween, and
the second semiconductor substrate further comprises a second interposer region spaced apart from a corresponding one of the plurality of second semiconductor chip regions with a corresponding one of the one or more second scribe lane regions interposed therebetween,

the first interposer region comprises a plurality of first additional through-electrodes passing through the first semiconductor substrate, and

the second interposer region comprises a plurality of second additional through-electrodes passing through the second semiconductor substrate and electrically connecting the plurality of first additional through-electrodes to the upper semiconductor chip,

the semiconductor package further comprises a plurality of additional bonded pads passing through the first cover insulating layer and the second cover insulating layer and electrically connecting the plurality of first additional through-electrodes to the plurality of second additional through-electrodes.

18. A semiconductor package comprising:

a first semiconductor substrate including an active surface, the first semiconductor substrate including,

a plurality of scribe lane regions, and

a plurality of first semiconductor chip regions spaced apart from one another with corresponding ones of the plurality of scribe lane regions therebetween, each of the plurality of first semiconductor chip regions provided with at least one first semiconductor device on the active surface of the first semiconductor substrate;

a plurality of first through-electrodes in the plurality of first semiconductor chip regions and passing through the first semiconductor substrate;

a first cover insulating layer covering the active surface of the first semiconductor substrate;

a plurality of lower semiconductor chips on the first semiconductor substrate and corresponding to the plurality of first semiconductor chip regions, respectively, each of the plurality of lower semiconductor chips including,

a second semiconductor substrate having an active surface on which at least one second semiconductor device is located,

the second semiconductor substrate including a plurality of second through-electrodes passing therethrough, and

a second cover insulating layer covering the active surface of the second semiconductor substrate and in contact with the first cover insulating layer;

a plurality of device bonded pads passing through the first cover insulating layer and the second cover insulating layer and electrically connecting the plurality of first through-electrodes to the plurality of second through-electrodes; and

an upper semiconductor chip including a third semiconductor device, the upper semiconductor chip vertically overlapping at least two of the plurality of lower semiconductor chips and electrically connected to the plurality of second through-electrodes,

wherein each of the plurality of device bonded pads is a diffusion-bonded integral structure of two sub-structures.

19. The semiconductor package of claim 18, further comprising:

a filling molding member on the first semiconductor substrate, the filling molding member filling spaces between the plurality of lower semiconductor chips.

20. The semiconductor package of claim 18 or claim 19, wherein the first semiconductor device and the second semiconductor device are of a same type, and
a third semiconductor device is of a different type from the first semiconductor device and the second semiconductor device.