SEMICONDUCTOR DEVICE WITH THIN PROFILE WLCSP WITH VERTICAL INTERCONNECT OVER PACKAGE FOOTPRINT

Field of the Invention

The present invention relates in general to semiconductor devices and, more particularly, to a semiconductor device and method of forming a thin profile WLCSP containing face to face semiconductor die with vertical interconnect capability over the entire package footprint.

Background of the Invention

Semiconductor devices are commonly found in modern electronic products. Semiconductor devices vary in the number and density of electrical components. Discrete semiconductor devices generally contain one type of electrical component, e.g., light emitting diode (LED), small signal transistor, resistor, capacitor, inductor, and power metal oxide semiconductor field effect transistor (MOSFET). Integrated semiconductor devices typically contain hundreds to millions of electrical components. Examples of integrated semiconductor devices include microcontrollers, microprocessors, charged-coupled devices (CCDs), solar cells, and digital micro-mirror

Claims

What is claimed:

1. A semiconductor device, comprising:

a first semiconductor die including a first thickness during fabrication;

a second semiconductor die including a first thickness during fabrication and an active surface of the second semiconductor die disposed over an active surface of the first semiconductor die;

an encapsulant deposited over the first semiconductor die and second semiconductor die;

a conductive pillar formed through the encapsulant within a footprint of the first semiconductor die;

a build-up interconnect structure including an insulating layer and a redistribution layer each formed directly on the encapsulant and a non-active surface of the second semiconductor die, the redistribution layer of the build-up interconnect structure directly contacting the conductive pillar;

wherein the first semiconductor die includes a second thickness less than the first thickness of the first semiconductor die and the second semiconductor die includes a second thickness less than the first thickness of the second semiconductor die in the semiconductor device; and

a contact pad formed on a non-active surface of the first semiconductor die, the contact pad electrically connected to the conductive pillar and the build-up interconnect structure.

2. The semiconductor device of claim 1, further including a discrete semiconductor component disposed over the first semiconductor die.

3. The semiconductor device of claim 1, wherein the conductive pillar includes a post, bump, or microbump.

4. The semiconductor device of claim 1, further including a heat sink or shielding layer disposed over the first semiconductor die, the shielding layer electrically connected to the contact pad.

5. The semiconductor device of claim 1, further including an interconnect structure disposed over the contact pad on the non-active surface of the first semiconductor die opposite the active surface of the first semiconductor die.

6. The semiconductor device of claim 1, further including a third semiconductor die disposed over the first semiconductor die and the non-active surface of the second semiconductor die.

7. A semiconductor device, comprising:

a first semiconductor die;

a second semiconductor die disposed over the first semiconductor die;

an encapsulant deposited over the first semiconductor die and second semiconductor die, the encapsulant coplanar with a non-active surface of the second semiconductor die;

a first interconnect structure formed through the encapsulant and extending to the first semiconductor die; and

a build-up interconnect structure including an insulating layer and a redistribution layer each formed in direct contact with the encapsulant and the non-active surface of the second semiconductor die, the build-up interconnect structure directly contacting the first interconnect structure.

8. The semiconductor device of claim 7, further including a third semiconductor die disposed over the first semiconductor die.

9. The semiconductor device of claim 7, further including a discrete semiconductor device disposed over the first semiconductor die.

10. The semiconductor device of claim 7, further including a third semiconductor die disposed over the first interconnect structure.

11. The semiconductor device of claim 7, further including a second interconnect structure disposed over a surface of the first semiconductor die opposite an active surface of the first semiconductor die.

12. The semiconductor device of claim 11, further including the encapsulant deposited around the first and second semiconductor die.

13. The semiconductor device of claim 7, further including a heat sink or shielding layer disposed over the first semiconductor die.

14. A semiconductor device, comprising:

a first semiconductor die including a contact pad;

a second semiconductor die disposed over the contact pad of the first semiconductor die;

an encapsulant deposited over the first semiconductor die and second semiconductor die, the encapsulant coplanar with a

non-active surface of the second semiconductor die;

a first interconnect structure formed through the encapsulant over the first semiconductor die; and

a second interconnect structure including an insulating layer and a conductive layer each formed in direct contact with the encapsulant and second semiconductor die, the conductive layer formed in direct contact with the first interconnect structure.

15. The semiconductor device of claim 14, further including a third semiconductor die including a fabrication thickness disposed over the first semiconductor die, the third semiconductor die including a reduced thickness relative to the fabrication thickness in the semiconductor device.

16. The semiconductor device of claim 14, further including a discrete semiconductor device disposed over the first semiconductor die.

17. The semiconductor device of claim 14, wherein the first interconnect structure includes a conductive pillar, post, bump, or microbump.

18. The semiconductor device of claim 14, further including a third semiconductor die disposed over the encapsulant.

19. The semiconductor device of claim 14, further including a third interconnect structure disposed over a surface of the first semiconductor die opposite an active surface of the first semiconductor die.