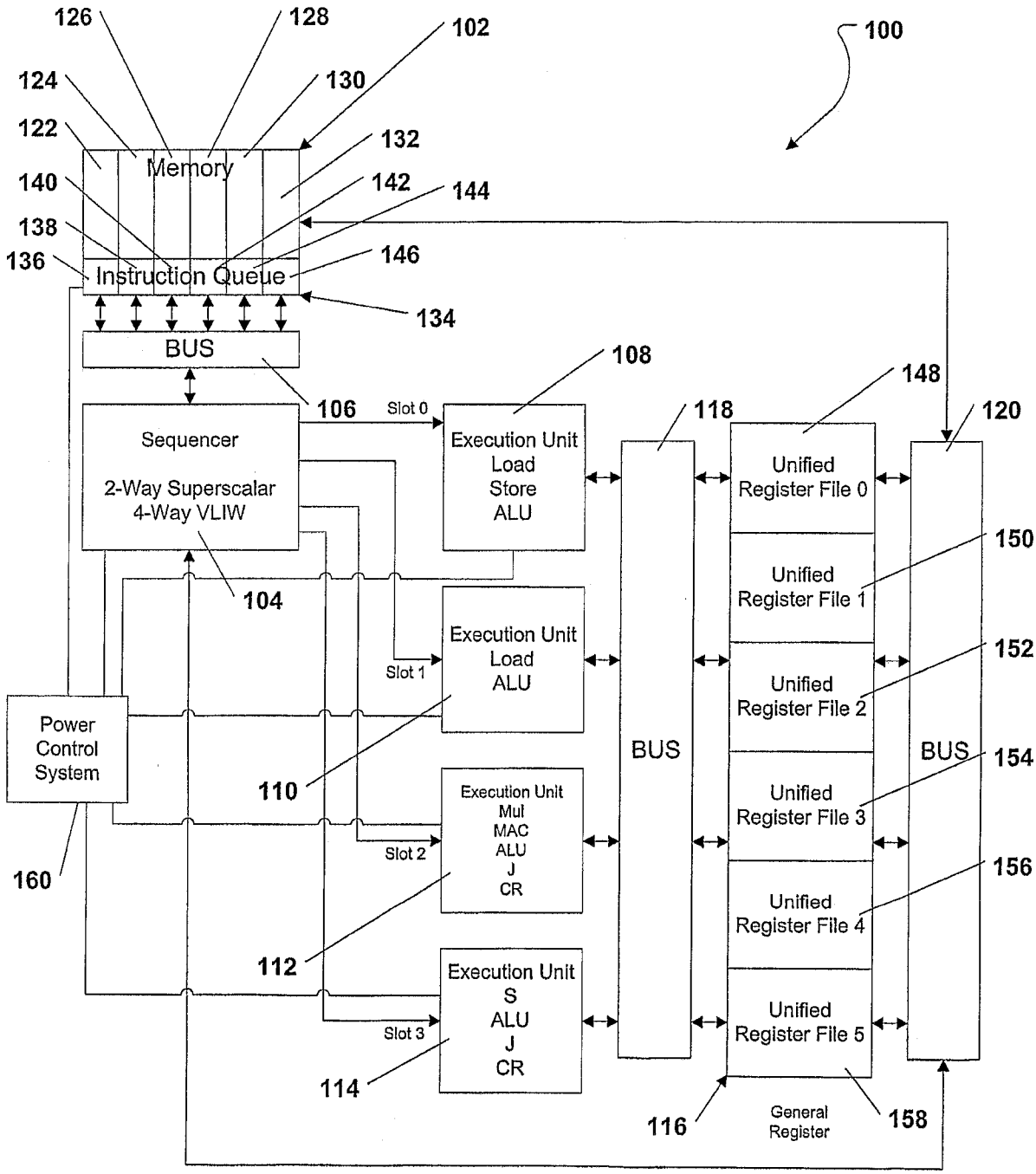

126
128
102
100
124
130
122
132
Memory
140
142
144
138
146
136
Instruction Queue
134
BUS
108
148
106
Slot 0
118
120
Sequencer
2-Way Superscalar
4-Way VLIW
Execution Unit
Load
Store
ALU
Unified
Register File 0
150
Unified
Register File 1
104
Execution Unit
Load
ALU
152
Slot 1
Unified
Register File 2
Power
Control
System
BUS
BUS
154
110
Execution Unit
Mul
MAC
ALU
J
CR
Unified
Register File 3
Slot 2
156
160
Unified
Register File 4
112
Execution Unit
S
ALU
J
CR
Unified
Register File 5
Slot 3
114
116
General
Register
158

FIG. 1

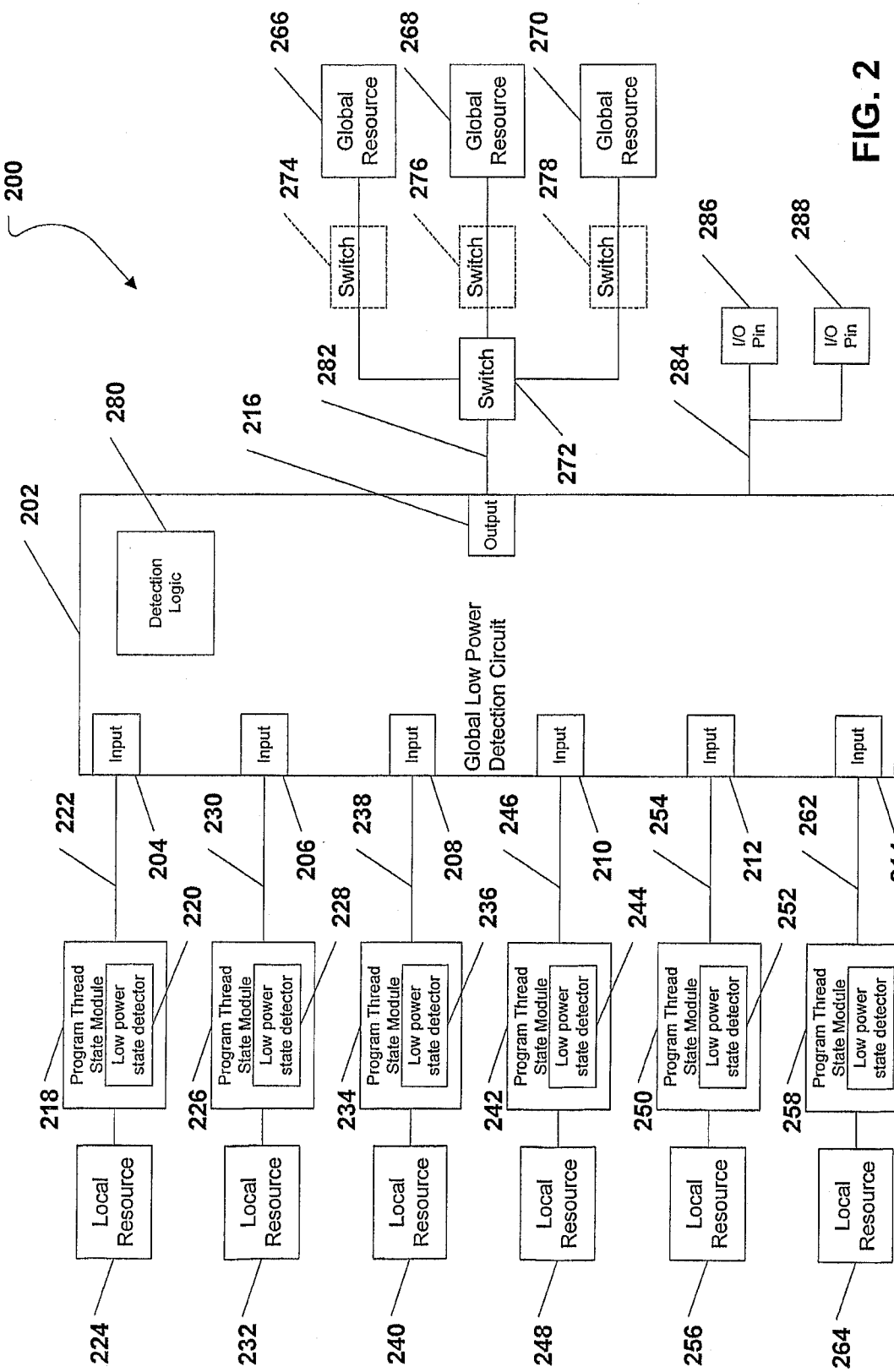

200
202
Global Low Power Detection Circuit
Detection Logic
280
Input
Output
216
272
Switch
282
284
I/O Pin
286
288
Switch
274
276
278
Global Resource
266
268
270
Program Thread State Module
Low power state detector
218
220
222
204
226
228
230
206
234
236
238
208
242
244
246
210
250
252
254
212
258
260
262
214
Local Resource
224
232
240
248
256
264

FIG. 2

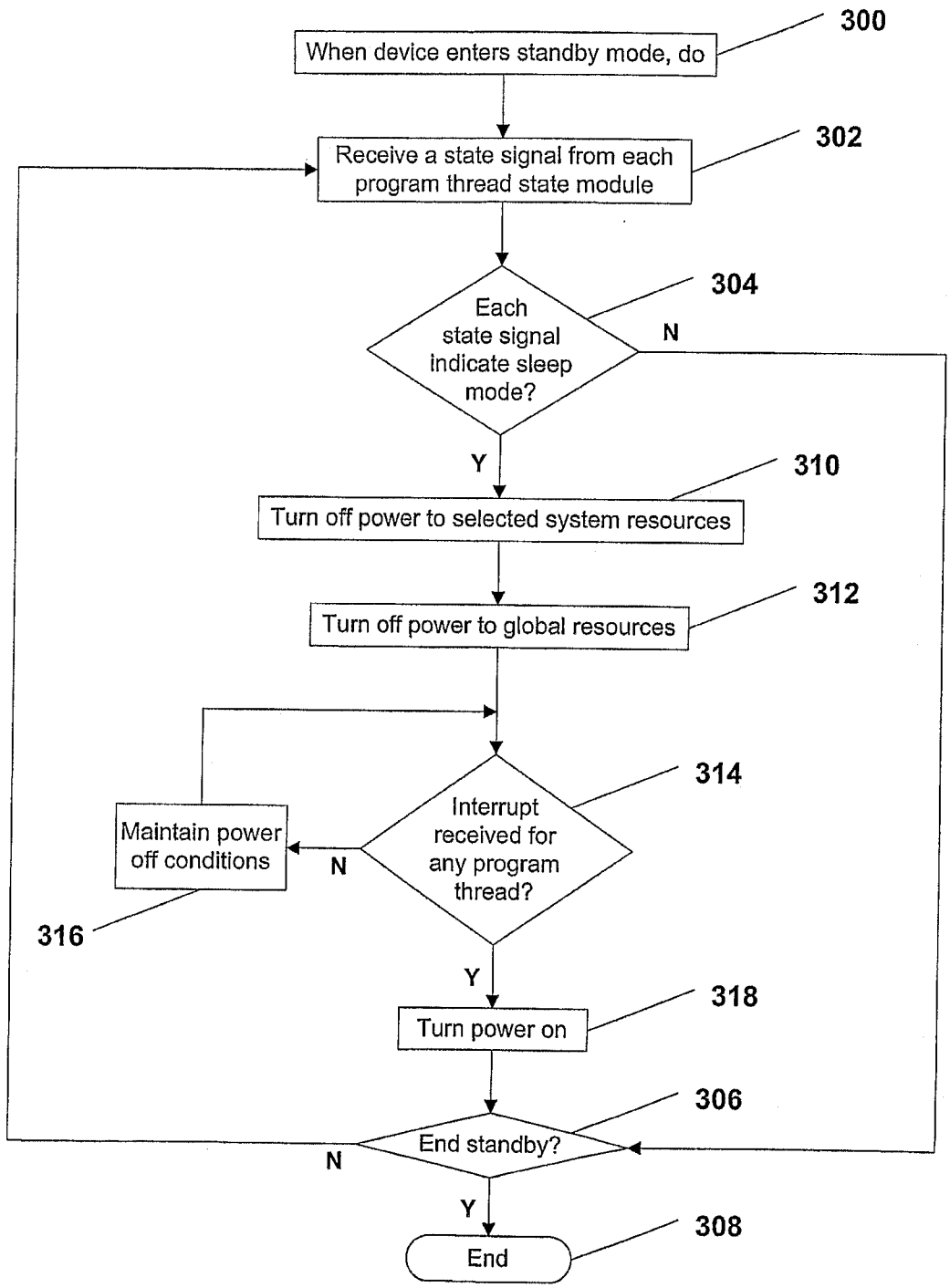

When device enters standby mode, do
300
Receive a state signal from each program thread state module
302
Each state signal indicate sleep mode?
304
N
Y
Turn off power to selected system resources
310
Turn off power to global resources
312
Interrupt received for any program thread?
314
Maintain power off conditions
N
316
Y
Turn power on
318
End standby?
306
N
Y
End
308

FIG. 3

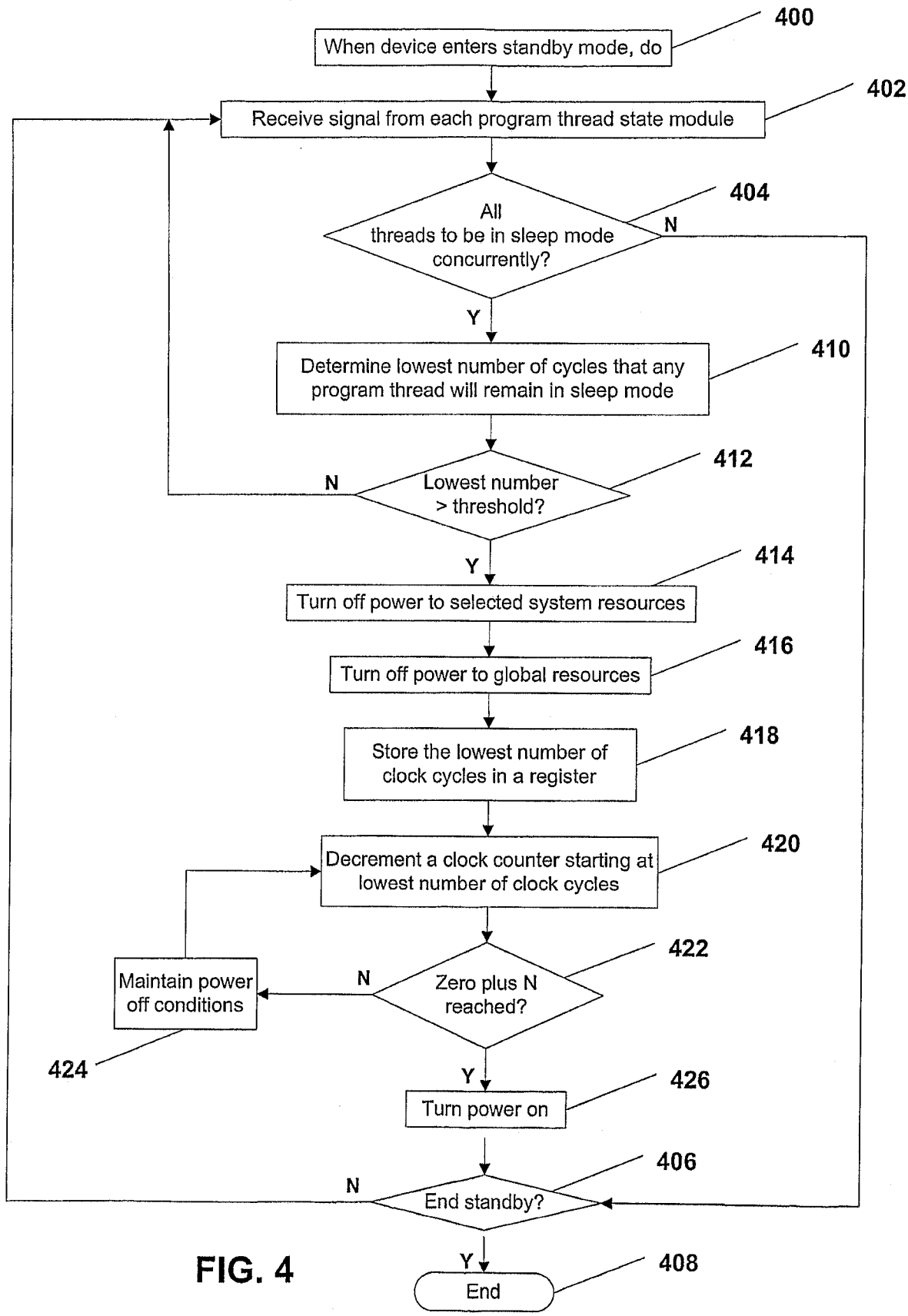

400
When device enters standby mode, do
402
Receive signal from each program thread state module
404
All threads to be in sleep mode concurrently?
N
Y
410
Determine lowest number of cycles that any program thread will remain in sleep mode
412
Lowest number > threshold?
N
Y
414
Turn off power to selected system resources
416
Turn off power to global resources
418
Store the lowest number of clock cycles in a register
420
Decrement a clock counter starting at lowest number of clock cycles
422
Zero plus N reached?
N
Maintain power off conditions
424
Y
426
Turn power on
406
End standby?
N
Y
408
End

FIG. 4

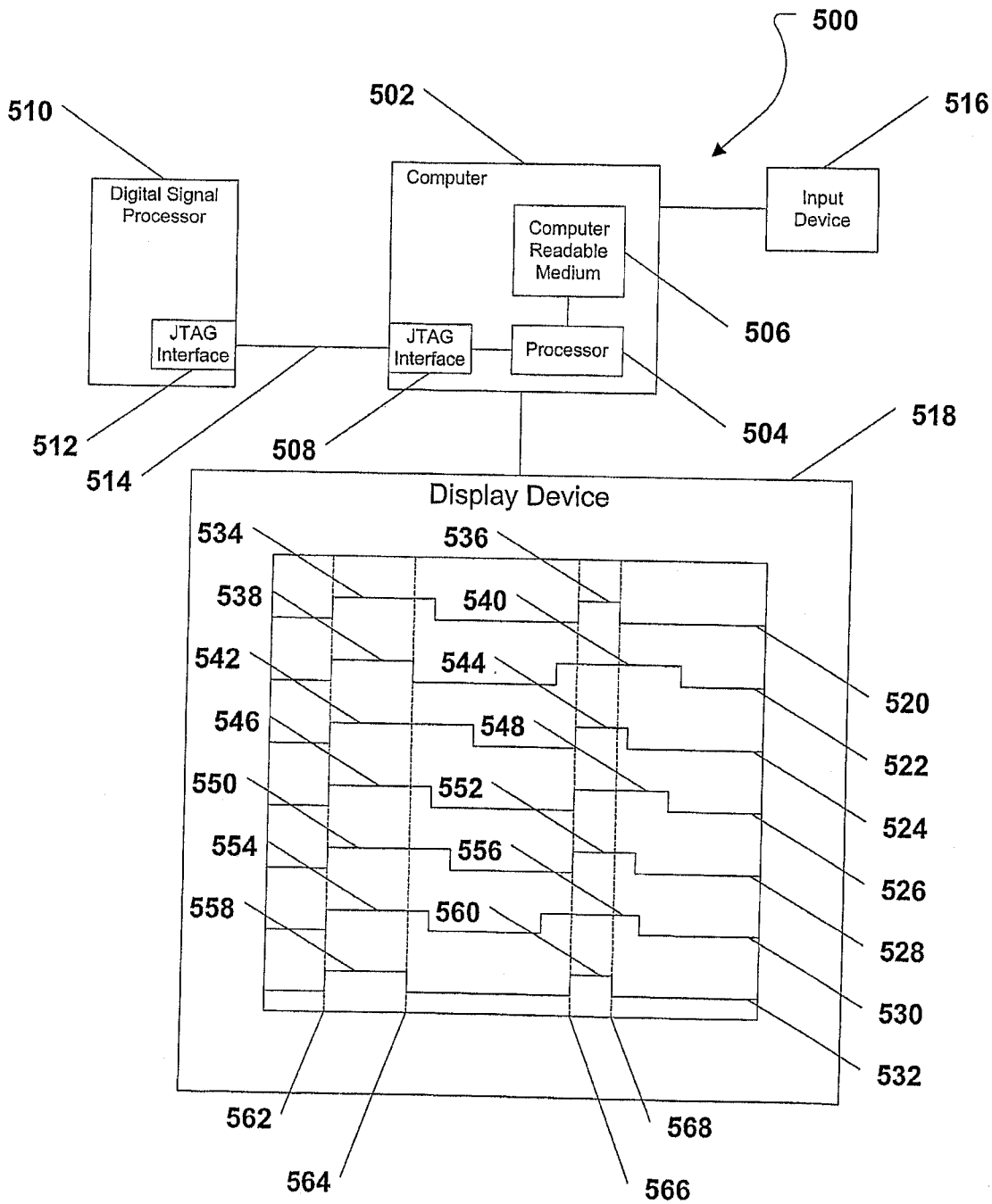

500
502
510
516
Digital Signal Processor
Computer
Input Device
Computer Readable Medium
506
JTAG Interface
JTAG Interface
Processor
504
512
514
508
518
Display Device
534
536
538
540
542
544
520
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568
564
566

FIG. 5

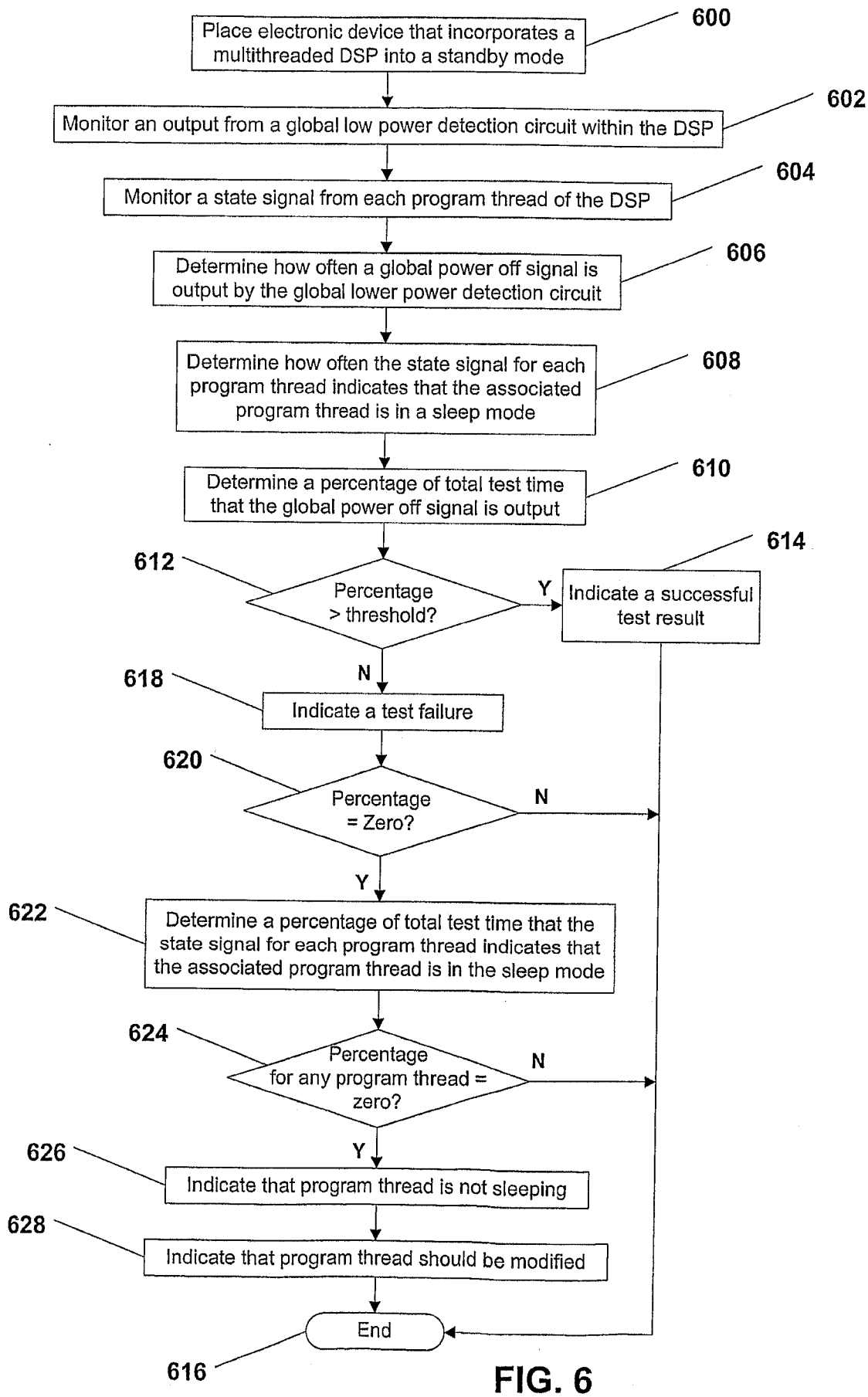

Place electronic device that incorporates a multithreaded DSP into a standby mode
600
Monitor an output from a global low power detection circuit within the DSP
602
Monitor a state signal from each program thread of the DSP
604
Determine how often a global power off signal is output by the global lower power detection circuit
606
Determine how often the state signal for each program thread indicates that the associated program thread is in a sleep mode
608
Determine a percentage of total test time that the global power off signal is output
610
612
Percentage > threshold?
Y
614
Indicate a successful test result
N
618
Indicate a test failure
620
Percentage = Zero?
N
Y
622
Determine a percentage of total test time that the state signal for each program thread indicates that the associated program thread is in the sleep mode
624
Percentage for any program thread = zero?
N
Y
626
Indicate that program thread is not sleeping
628
Indicate that program thread should be modified
End
616

FIG. 6

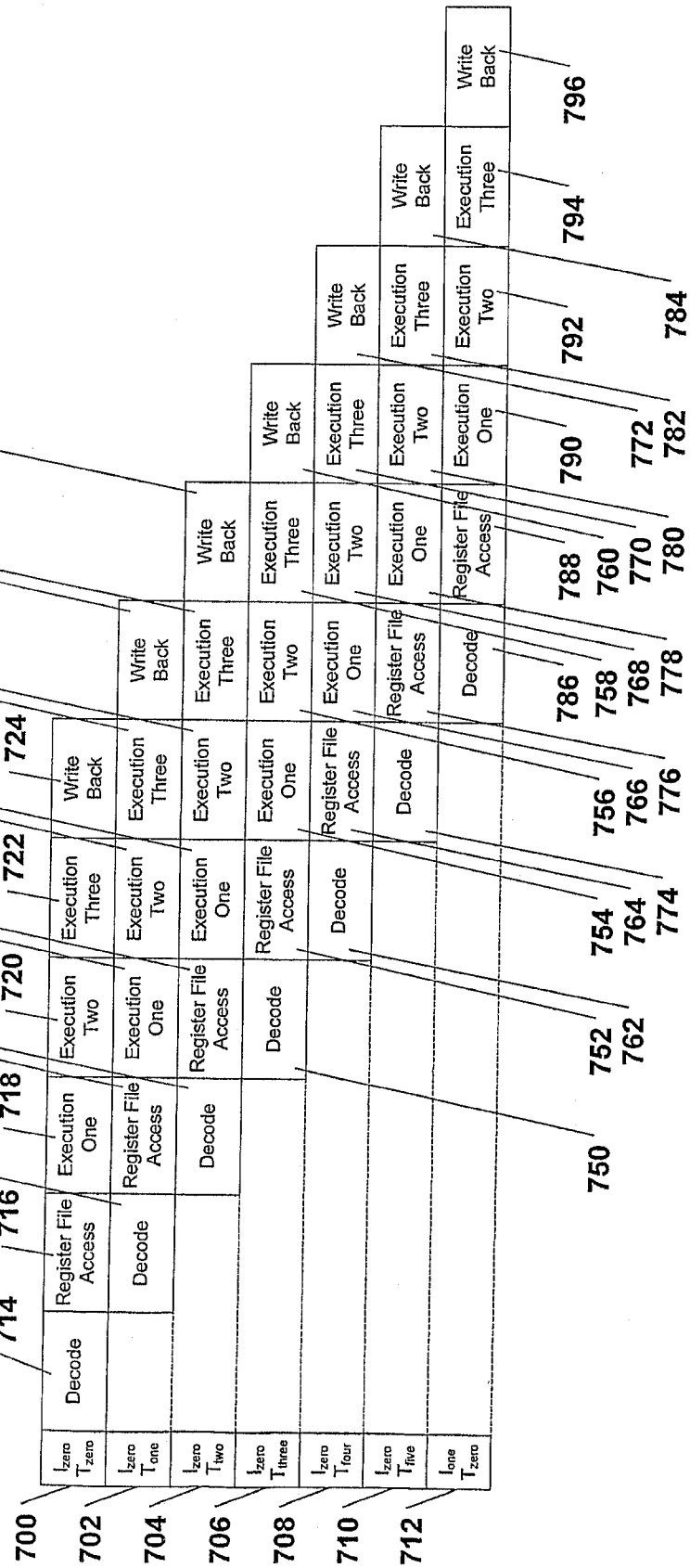

700
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740
742
744
746
748
750
752
754
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758
760
762
764
766
768
770
772
774
776
778
780
782
784
786
788
790
792
794
796
Decode
Register File Access
Execution One
Execution Two
Execution Three
Write Back

FIG. 7

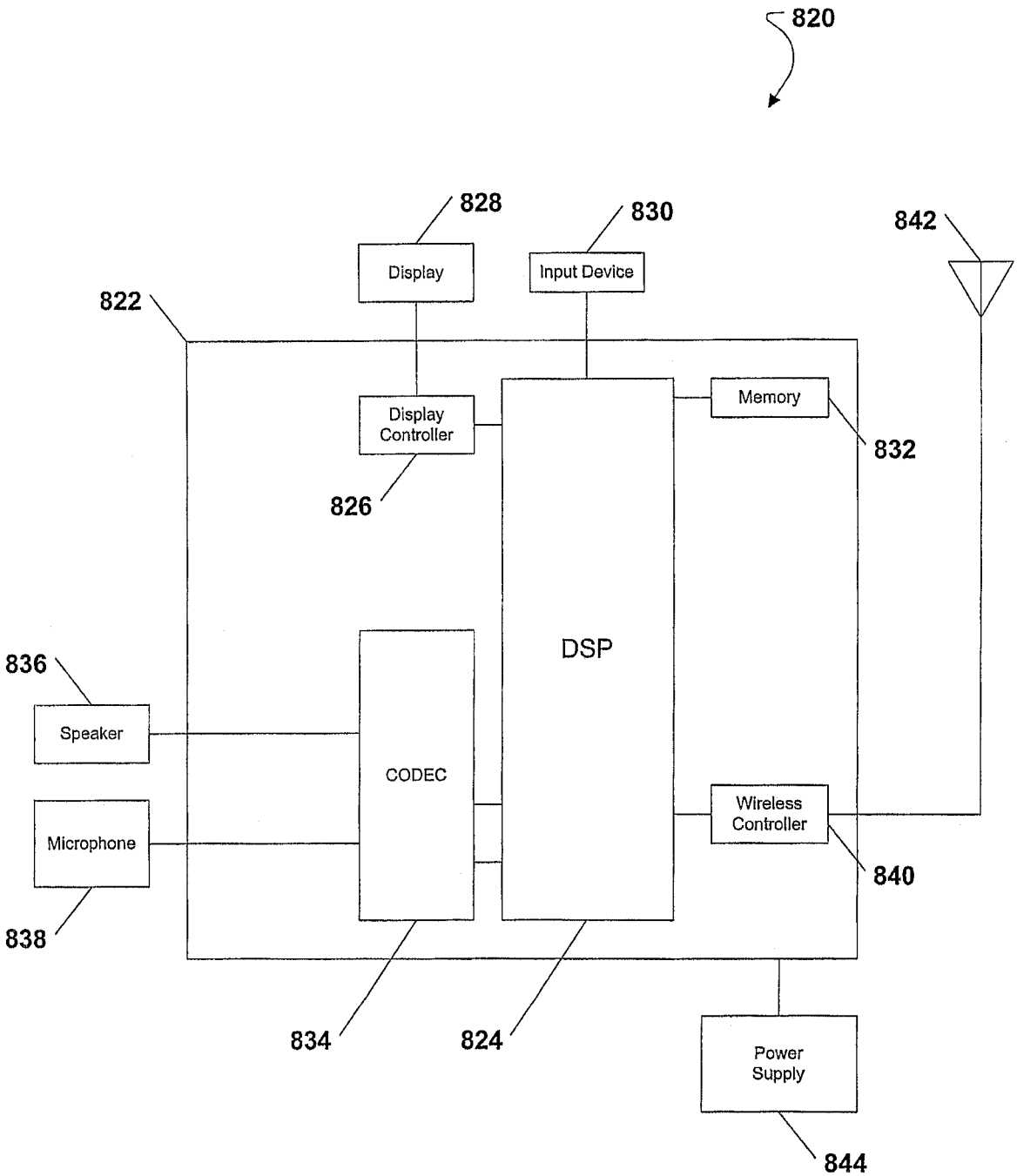

820
828
Display
830
Input Device
842
822
Display Controller
826
Memory
832
DSP
836
Speaker
CODEC
Microphone
838
Wireless Controller
840
834
824
Power Supply
844

FIG. 8

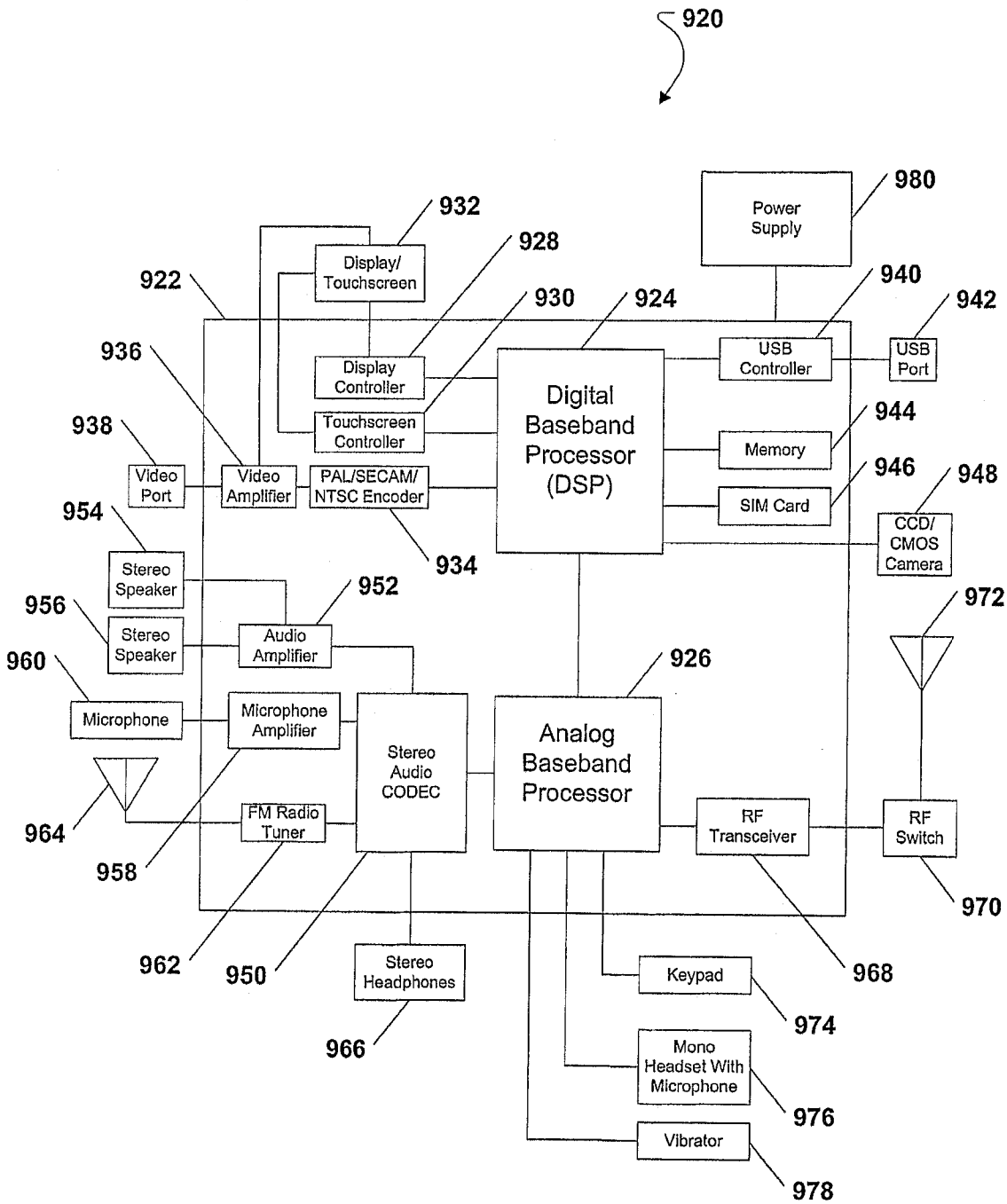

920
Power Supply
980
932
928
Display/ Touchscreen
922
930
924
940
942
936
Display Controller
USB Controller
USB Port
Digital Baseband Processor (DSP)
938
Touchscreen Controller
944
Memory
946
948
Video Port
Video Amplifier
PAL/SECAM/ NTSC Encoder
SIM Card
954
CCD/ CMOS Camera
934
Stereo Speaker
952
956
Stereo Speaker
Audio Amplifier
972
960
926
Microphone
Microphone Amplifier
Stereo Audio CODEC
Analog Baseband Processor
964
FM Radio Tuner
RF Transceiver
RF Switch
958
970
962
950
968
Stereo Headphones
Keypad
974
966
Mono Headset With Microphone
976
Vibrator
978

FIG. 9

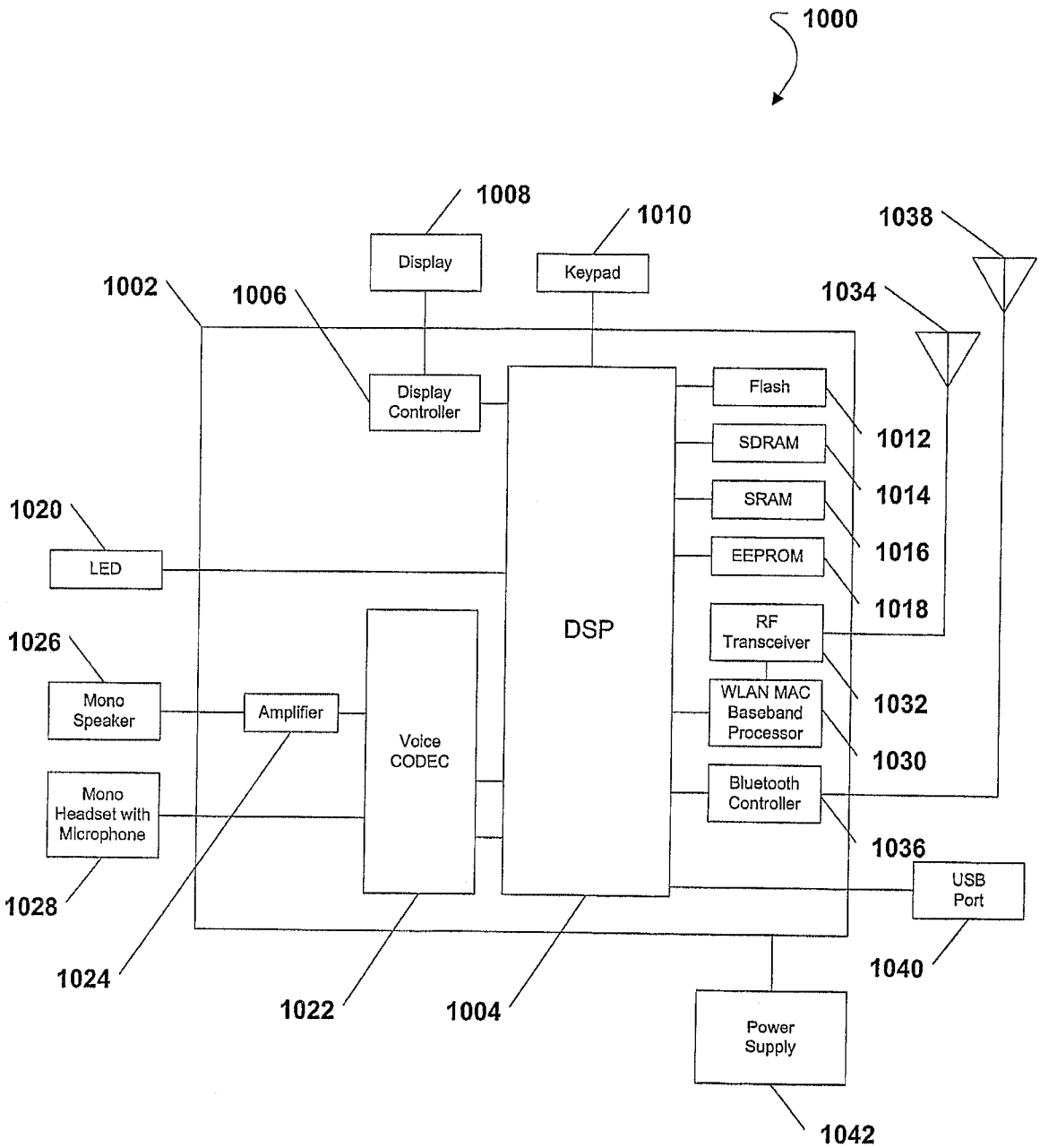

1000
1008
1010
1038
Display
Keypad
1002
1006
1034
Display Controller
Flash
SDRAM
SRAM
EEPROM
RF Transceiver
WLAN MAC Baseband Processor
Bluetooth Controller
1012
1014
1016
1018
1032
1030
1036
1020
LED
1026
Mono Speaker
Amplifier
Voice CODEC
DSP
Mono Headset with Microphone
1028
1024
1022
1004
USB Port
1040
Power Supply
1042

FIG. 10

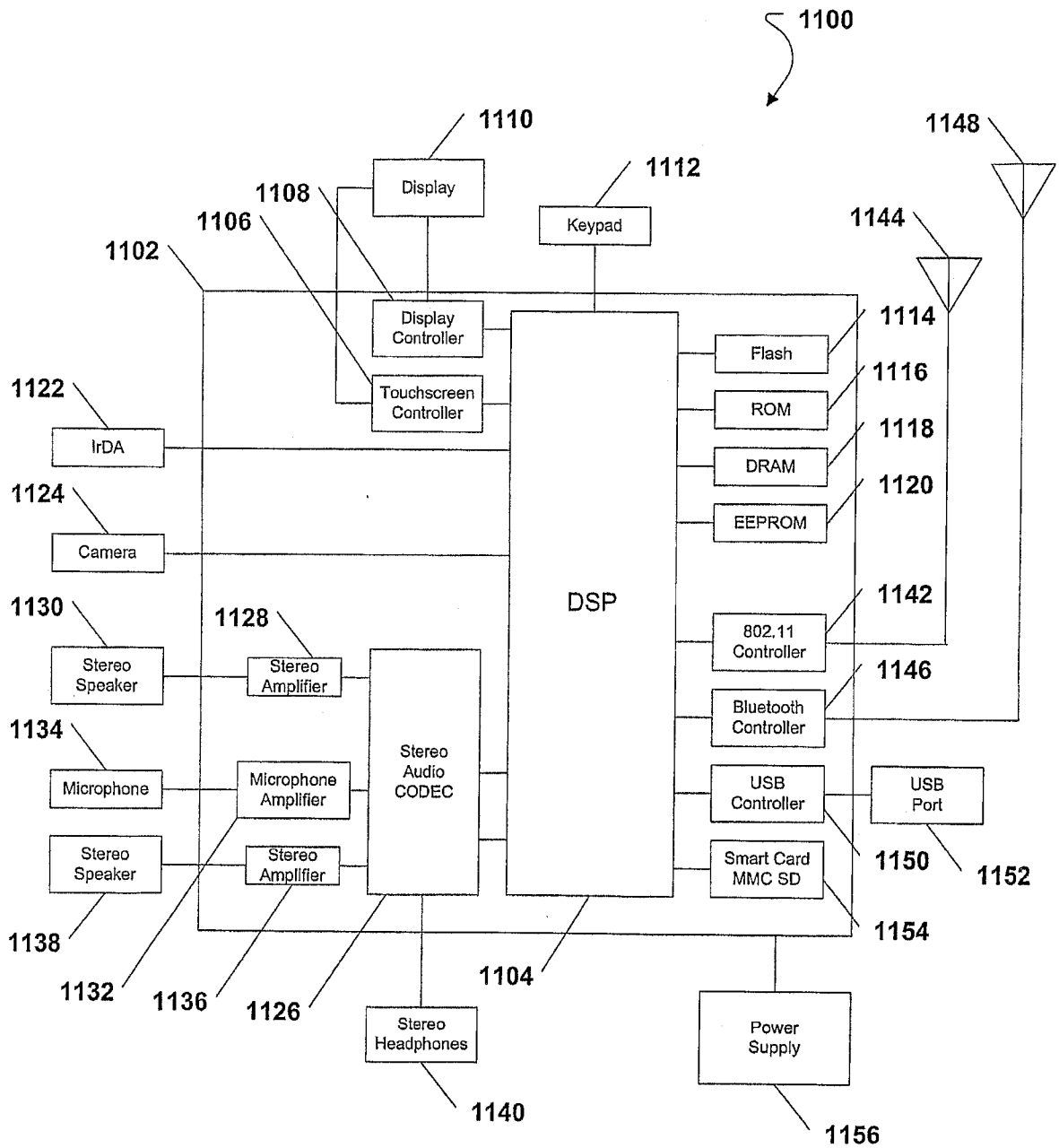

1100
1110
Display
1112
Keypad
1148
1108
1106
1102
1144
Display Controller
Touchscreen Controller
1114
Flash
1116
ROM
1118
DRAM
1120
EEPROM
1122
IrDA
1124
Camera
DSP
1142
802.11 Controller
1146
Bluetooth Controller
1130
Stereo Speaker
1128
Stereo Amplifier
1134
Microphone
Microphone Amplifier
Stereo Audio CODEC
USB Controller
USB Port
1150
1152
Stereo Speaker
Stereo Amplifier
Smart Card MMC SD
1154
1138
1132
1136
1126
1104
Stereo Headphones
Power Supply
1140
1156

FIG. 11

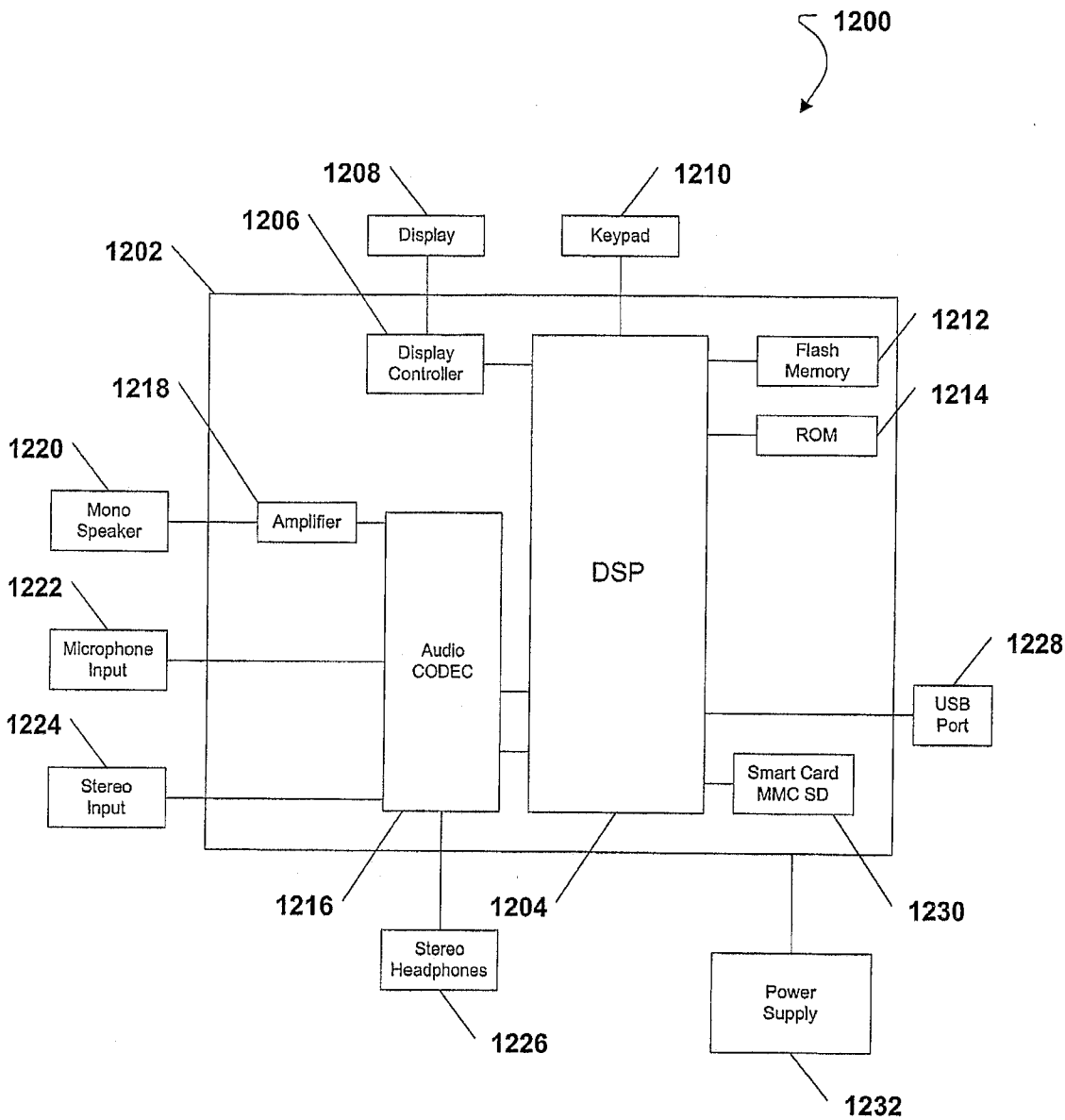

1200
1208
1210
1206
Display
Keypad
1202
1212
Display Controller
Flash Memory
1218
1214
ROM
1220
Mono Speaker
Amplifier
DSP
1222
Microphone Input
Audio CODEC
1228
USB Port
1224
Stereo Input
Smart Card MMC SD
1216
1204
1230
Stereo Headphones
Power Supply
1226
1232

FIG. 12