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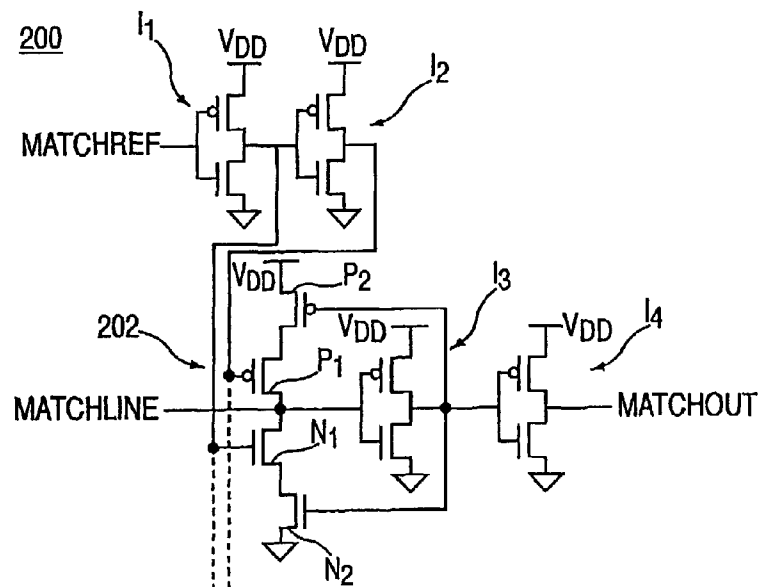
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(54) Title: CONTENT ADDRESSABLE MEMORY (CAM) WITH ERROR CHECKING AND CORRECTION



(57) Abstract: A content addressable memory (CAM) (100) capable of ignoring and correcting bit errors contained therein is disclosed. In an exemplary embodiment, the CAM includes a plurality of individual CAM cells (102) for storing a codeword having a number of bits associated therewith. A match line (MATCHLINE) is coupled to each of the plurality of individual CAM cells, and is used to indicate a match status of a comparand word (104) that is compared to the stored codeword. The match status is reflective of either a match state or a mismatch state. A sensing apparatus (200) is used for latching the match line to the match state whenever the comparand word (104) mismatches the stored codeword by a number of N or fewer bits, wherein N is defined a maximum number of correctable bits for a given error checking and correction (ECC) algorithm used.

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