specifically shown in FIG. 9, the memory device 300 may further include a memory bank having a plurality of bank arrays. In addition, in FIG. 9, only one PIM circuit 350 is illustrated. However, a plurality of PIM circuits may be provided in the memory device 300 to correspond to the plurality of bank arrays.

[0083] According to the above-described embodiments, the instruction memory 330 may include a plurality of instruction queue segments for storing instructions based on the circular queue technique. In addition, the instruction memory 330 may include a plurality of rows and a plurality of columns, and an instruction storage position may be directed by a queue address including a row address RA and a column address CA. For example, when it is assumed that each of the instruction queue segments of the instruction memory 330 stores one instruction, one row of the instruction memory 330 may include a plurality of instruction queue segments.

[0084] The memory device 300 may receive the command and address from the host HOST through the command address bus CA BUS and may receive the queue address in relation to the instruction loading or updating operation. In addition, the memory device 300 may receive the instructions Inst from the host HOST. For example, the memory device 300 may receive the instructions Inst through the data bus DQ BUS. In addition, in the instruction executing and updating mode, based on control of the processing controller 320, an instruction may be read from the instruction memory 330 and executed and, based on control of the control logic 310, the instructions Inst from the host HOST may be updated to the instruction memory 330.

[0085] The control logic 310 may include an index manager 311 and the index manager 311 may generate indices Index corresponding to the instructions Inst. According to exemplary embodiments, the indices Index may be assigned to entries of the instruction queue segments of the instruction memory 330, in which the instructions are stored, and an operation of directing executed instructions may be performed based on the indices Index. For example, the index manager 311 may calculate the indices Index corresponding to the instructions by using at least some of the bits included in the row address RA and the column address CA and, when the instructions are stored in the instruction memory 330, may store a corresponding indices Index together with the instructions. Alternatively, according to the embodiment illustrated in FIG. 9, an index memory 331 is further provided in the memory device 300 and the indices Index may be stored in the index memory 331.

[0086] The index order storage circuit 360 may store index order information provided by the host HOST. For example, after the plurality of instructions are loaded into the instruction memory 330 and the instruction loading operation is completed, in order to set the execution order of the instructions loaded on the instruction memory 330, the index order information may be provided from the host HOST to the memory device 300.

[0087] Then, the memory device 300 may read and execute the instructions in the index order stored in the index order storage circuit 360 in performing the operation logic processing operation. For example, whenever the operation logic processing operation is performed, an index Index stored in the index order storage circuit 360 is read and the control logic 310 may provide the read index Index to the processing controller 320. An indices Index corresponding to a plurality of instructions to be serially processed may be included in the index order information.

[0088] According to an exemplary embodiment, the indices Index may be set to have various values. For example, to correspond to m instructions stored in m instruction queue segments included in the instruction memory 330, the indices Index having one or more bits are generated and indices Index having different bit values may be stored in the instruction memory 330 to correspond to the instructions. The processing controller 320 may compare the index Index read from the index order storage circuit 360 with the indices Index stored with the instruction memory 330, may read an instruction corresponding to the received index Index, and may control the operation logic processing operation.

[0089] According to the above-described embodiment, a plurality of instructions for directing the same kind of operations need not be repeatedly stored in the instruction memory 330. For example, multiple indices may be used for a single stored instruction within the circular queue to execute that instruction repeatedly prior to overwriting. Therefore, a size of the instruction memory 330 may be reduced. In addition, without executing the instructions in the order stored in the instruction memory 330, based on the information stored in the index order storage circuit 360, an instruction stored in an arbitrary position may be executed as needed.

[0090] In the operation logic processing operation according to the above-described embodiment, an access operation of the instruction memory 330 based on a counting operation of the program counter 340 may be selectively performed. For example, some of the plurality of operations of the neural network function may be performed based on the

WHAT IS CLAIMED IS:

1. A memory device comprising:

a memory bank including at least one bank array of memory cells;

a processor in memory (PIM) circuit connected to the memory bank and configured to perform an operation logic processing operation by using at least one of data provided by a host or data read from the memory bank; and

an instruction memory connected to the PIM circuit and including a circular instruction memory queue having a plurality of first to m^{th} instruction queue segments configured in a circle to store instructions provided by the host,

wherein instructions stored in the first to m^{th} instruction queue segments are executed in response to an operation request from the host, and a new instruction provided by the host is updated over a completely executed instruction at a segment in the circular instruction memory queue.

2. The memory device of claim 1,

wherein some of a plurality of instructions are stored in the first to m^{th} instruction queue segments in relation to one neural network function, and

wherein others of the plurality of instructions are sequentially updated over completely executed instructions among the first to m^{th} instruction queue segments.

3. The memory device of claim 1 or claim 2, further comprising control logic configured to decode a command or address received from the host, to control a memory bank operation on the memory bank based on the decoded command or address, or to perform a control operation controlling the PIM circuit to perform the operation logic processing operation.

4. The memory device of any one of claims 1 to 3,

wherein the memory bank comprises a plurality of first to N^{th} bank arrays and the PIM circuit comprises a plurality of first to N^{th} PIM circuits arranged to correspond to the first to N^{th} bank arrays, and

wherein the instruction memory is arranged to correspond to each of the first to N^{th} PIM circuits and an instruction read from the instruction memory is provided to a

corresponding PIM circuit.

5. The memory device of any one of claims 1 to 4,

wherein the memory device operates in a loading mode, an executing mode, and an executing and updating mode,

wherein, in the loading mode, first to m^{th} instructions are stored in the first to m^{th} instruction queue segments,

wherein, in the executing mode, in response to the operation request from the host, at least some of the first to m^{th} instructions are sequentially executed, and

wherein, in the executing and updating mode, in response to the operation request from the host, while executing instructions stored in the instruction memory, a new instruction is updated over a previously executed instruction in the circular instruction queue.

6. The memory device of any one of claims 1 to 4,

wherein first to m^{th} instructions are stored in the first to m^{th} instruction queue segments, and

wherein, after the first instruction that is executed, while a second instruction is executing, an $(m+1)^{th}$ instruction is updated over the first instruction in the circular instruction queue.

7. The memory device of any one of claims 1 to 4,

wherein first to m^{th} instructions are stored in the first to m^{th} instruction queue segments, and

wherein, after a plurality of first to k^{th} instructions are sequentially executed, an operation of updating a new instruction starts from the first executed instruction in the circular instruction queue.

8. The memory device of any one of claims 1 to 7, further comprising:

an index memory configured to store indices corresponding to instructions stored in the instruction memory; and

an index order storage circuit configured to store index order information representing an execution order of the instructions from the host,

wherein, as the operation request is provided from the host, instructions stored in the

instruction memory are executed in an order in accordance with the index order information.

9. The memory device of claim 8, wherein, as a plurality of indices directing the same instruction are included in the index order information, an instruction stored in one instruction queue segment is executed a plurality of times.

10. The memory device of any one of claims 1 to 9, wherein each of the first to m^{th} instruction queue segments comprises at least one of a flip-flop or a latch.

11. A memory device comprising:

a memory bank including at least one bank array of memory cells;

a processor in memory (PIM) circuit connected to the memory bank and configured to perform an operation logic processing operation by using at least one of data provided by a host or data read from the memory bank;

an instruction memory connected to the PIM circuit and including a circular instruction memory queue having a plurality of first to m^{th} instruction queue segments configured to store instructions provided by the host;

an index manager configured to generate indices corresponding to the instructions stored in the instruction memory; and

an index order storage circuit configured to store index order information representing an execution order of the instructions from the host,

wherein, as an operation request is provided by the host, instructions stored in the instruction memory are executed in the execution order in accordance with the stored index order information.

12. The memory device of claim 11, wherein, as a plurality of indices directing the same instruction are included in the index order information, an instruction stored in one instruction queue segment is executed the same plurality of times.

13. The memory device of claim 11 or claim 12, wherein the index manager receives a row address and a column address representing a storage position of the instruction memory, and generates the index by using at least some of a plurality of bits of the row address and the column address.

14. The memory device of any one of claims 11 to 13, further comprising an index memory configured to store indices corresponding to instructions stored in the instruction memory,

wherein the index manager stores the indices generated to correspond to the instructions in the index memory.

15. An operating method of a memory device having instruction memory configured to store instructions related to operation processing and a processor in memory (PIM) circuit configured to perform operation logic processing operations corresponding to the instructions, the method comprising:

loading some of a plurality of instructions for a neural network function into a plurality of instruction queue segments of a circular instruction queue of the instruction memory;

the PIM circuit performing the operation logic processing operations by sequentially executing the loaded instructions;

overwriting, with others of the plurality of instructions for the neural network function, instruction queue segments having previously executed instructions; and

the PIM circuit performing operation logic processing operations by sequentially executing the others of the plurality of instructions.

16. The method of claim 15,

wherein the memory device operates in a loading mode, an executing mode, and an executing and updating mode,

wherein, in the loading mode, the instructions are stored in the instruction memory,

wherein, in the executing mode, in response to an operation request from a host, instructions stored in the instruction memory are sequentially executed, and

wherein, in the executing and updating mode, in response to the operation request from the host, while executing instructions stored in the instruction memory, a new instruction is updated over a previously executed instruction in an instruction queue segment.

17. The method of claim 15 or claim 16,

wherein the instruction memory comprises a plurality of first to m^{th} instruction queue

segments, and the same plurality of first to m^{th} instructions are stored in the first to m^{th} instruction queue segments, and

wherein, after the first instruction is executed, while the second instruction is executing, an $(m+1)^{th}$ instruction is updated over the first instruction in the circular instruction queue.

18. The method of claim 15 or claim 16,

wherein the instruction memory comprises a plurality of first to m^{th} instruction queue segments, and the same plurality of first to m^{th} instructions are stored in the first to m^{th} instruction queue segments, and

wherein, after a plurality of first to k^{th} instructions are sequentially executed, where k is less than m, an operation of updating a new instruction starts from the first instruction queue segment.

19. The method of any one of claims 15 to 18, wherein an operation of performing operation processing by executing one or more instructions, and an operation of overwriting instruction queue segments containing previously executed instructions with one or more new instructions, are alternately performed.

20. The method of any one of claims 16 to 19, further comprising:

storing indices corresponding to the instructions; and

receiving index order information representing an execution order of the instructions from a host,

wherein, as the operation request is provided by the host, instructions stored in the instruction memory are executed in an order in accordance with the received index order information.