

ABSTRACT

A system for executing a plurality of software threads, comprising: a plurality of processing circuitries; a plurality of memory areas connected to the processing circuitries, each memory area associated with at least one of the processing circuitries; and at least one hardware processor, connected to the processing circuitries and configured for: in each of a plurality of iterations: while the processing circuitries execute the software threads, collecting for each thread a plurality of thread statistical values indicative of a plurality of memory accesses to at least some of the memory areas performed when executing the thread; for at least one thread, performing an analysis comprising the thread statistical values thereof to identify a preferred memory area of the plurality of memory areas; and configuring one of the at least one processing circuitry associated with the preferred memory area to execute the at least one thread.

FIG. 2